International
IOR Rectifier

PD – 95937

IRF7805/IRF7805APbF

HEXFET® Chip-Set for DC-DC Converters

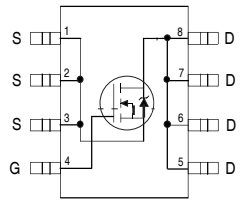
- N Channel Application Specific MOSFETs
- Ideal for Mobile DC-DC Converters
- Low Conduction Losses
- Low Switching Losses
- Lead-Free

Description

These new devices employ advanced HEXFET Power MOSFET technology to achieve an unprecedented balance of on-resistance and gate charge. The reduced conduction and switching losses make them ideal for high efficiency DC-DC Converters that power the latest generation of mobile microprocessors.

The IRF7805/IRF7805A offers maximum efficiency for mobile CPU core DC-DC converters.

SO-8



Top View

Device Features

	IRF7805	IRF7805A
Vds	30V	30V
Rds(on)	11mΩ	11mΩ
Qg	31nC	31nC
Qsw	11.5nC	
Qoss	36nC	36nC

Absolute Maximum Ratings

Parameter		Symbol	IRF7805	IRF7805A	Units
Drain-Source Voltage		V_{DS}	30		V
Gate-Source Voltage		V_{GS}	±12		
Continuous Drain or Source	25°C	I_D	13	13	A
Current ($V_{GS} \geq 4.5V$)	70°C		10	10	
Pulsed Drain Current①		I_{DM}	100	100	
Power Dissipation	25°C	P_D	2.5		W
	70°C		1.6		
Junction & Storage Temperature Range		T_J, T_{STG}	–55 to 150		°C
Continuous Source Current (Body Diode)①		I_S	2.5	2.5	A
Pulsed source Current		I_{SM}	106	106	

Thermal Resistance

Parameter		Max.	Units
Maximum Junction-to-Ambient③	$R_{\theta JA}$	50	°C/W

11/9/04

Electrical Characteristics

Parameter		IRF7805			IRF7805A			Units	Conditions
		Min	Typ	Max	Min	Typ	Max		
Drain-to-Source Breakdown Voltage*	$V_{(BR)DSS}$	30	–	–	30	–	–	V	V_{GS} = 0V, I_D = 250µA
Static Drain-Source on Resistance*	R_{DS}(on)		9.2	11		9.2	11	mΩ	V_{GS} = 4.5V, I_D = 7A②
Gate Threshold Voltage*	V_{GS}(th)	1.0			1.0			V	V_{DS} = V_{GS}, I_D = 250µA
Drain-Source Leakage Current*	I_{DSS}			30			30	µA	V_{DS} = 24V, V_{GS} = 0
				150			150		V_{DS} = 24V, V_{GS} = 0, Tj = 100°C
Gate-Source Leakage Current*	I_{GSS}			±100			±100	nA	V_{GS} = ±12V
Total Gate Charge*	Q_g		22④	31④		22④	31④	nC	V_{GS} = 5V, I_D = 7A
Pre-Vth Gate-Source Charge	Q_{gs1}		3.7			3.7			V_{DS} = 16V, I_D = 7A
Post-Vth Gate-Source Charge	Q_{gs2}		1.4			1.4			
Gate to Drain Charge	Q_{gd}		6.8			6.8			
Switch Charge* (Q_{gs2} + Q_{gd})	Q_{SW}		8.2	11.5		8.2			
Output Charge*	Q_{oss}		30	36		30	36		V_{DS} = 16V, V_{GS} = 0
Gate Resistance	R_g		1.7			1.7		Ω	
Turn-on Delay Time	t_d(on)		16			16		ns	V_{DD} = 16V
Rise Time	t_r		20			20			I_D = 7A
Turn-off Delay Time	t_d (off)		38			38			R_g = 2Ω
Fall Time	t_f		16			16			V_{GS} = 4.5V Resistive Load

Source-Drain Rating & Characteristics

Parameter		Min	Typ	Max	Min	Typ	Max	Units	Conditions
Diode Forward Voltage*	V_{SD}			1.2			1.2	V	I_S = 7A②, V_{GS} = 0V
Reverse Recovery Charge⑤	Q_{rr}		88			88		nC	di/dt = 700A/µs V_{DS} = 16V, V_{GS} = 0V, I_S = 7A
Reverse Recovery Charge (with Parallel Schotkky)⑤	$Q_{rr(s)}$		55			55			di/dt = 700A/µs (with 10BQ040) V_{DS} = 16V, V_{GS} = 0V, I_S = 7A

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.
② Pulse width ≤ 300 µs; duty cycle ≤ 2%.
③ When mounted on 1 inch square copper board, t < 10 sec.
④ Measured at V_{DS} < 100mV. This approximates actual operation of a synchronous rectifier.
⑤ Typ = measured - Q_{oss}
* Devices are 100% tested to these parameters.

Power MOSFET Selection for DC/DC Converters

Control FET

Special attention has been given to the power losses in the switching elements of the circuit - Q1 and Q2. Power losses in the high side switch Q1, also called the Control FET, are impacted by the $R_{ds(on)}$ of the MOSFET, but these conduction losses are only about one half of the total losses.

Power losses in the control switch Q1 are given by;

$$P_{loss} = P_{conduction} + P_{switching} + P_{drive} + P_{output}$$

This can be expanded and approximated by;

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(I \times \frac{Q_{gd}}{i_g} \times V_{in} \times f\right) + \left(I \times \frac{Q_{gs2}}{i_g} \times V_{in} \times f\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right)$$

This simplified loss equation includes the terms Q_{gs2} and Q_{oss} which are new to Power MOSFET data sheets.

Q_{gs2} is a sub element of traditional gate-source charge that is included in all MOSFET data sheets. The importance of splitting this gate-source charge into two sub elements, Q_{gs1} and Q_{gs2}, can be seen from Fig 1.

Q_{gs2} indicates the charge that must be supplied by the gate driver between the time that the threshold voltage has been reached (t1) and the time the drain current rises to I_{dmax} (t2) at which time the drain voltage begins to change. Minimizing Q_{gs2} is a critical factor in reducing switching losses in Q1.

Q_{oss} is the charge that must be supplied to the output capacitance of the MOSFET during every switching cycle. Figure 2 shows how Q_{oss} is formed by the parallel combination of the voltage dependant (non-linear) capacitance's C_{ds} and C_{dg} when multiplied by the power supply input buss voltage.

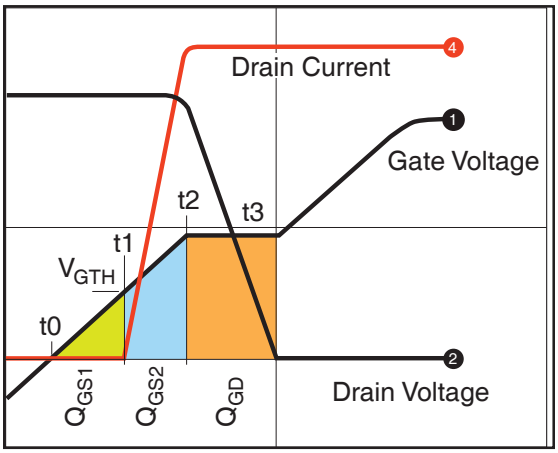


Figure 1: Typical MOSFET switching waveform

Synchronous FET

The power loss equation for Q2 is approximated by;

$$P_{loss} = P_{conduction} + P_{drive} + P_{output}^{*}$$

$$P_{loss} = \left(I_{rms}^{\ 2} \times R_{ds(on)}\right) + \left(Q_g \times V_g \times f\right) + \left(\frac{Q_{oss}}{2} \times V_{in} \times f\right) + \left(Q_{rr} \times V_{in} \times f\right)$$

*dissipated primarily in Q1.

For the synchronous MOSFET Q2, $R_{ds(on)}$ is an important characteristic; however, once again the importance of gate charge must not be overlooked since it impacts three critical areas. Under light load the MOSFET must still be turned on and off by the control IC so the gate drive losses become much more significant. Secondly, the output charge Q_{oss} and reverse recovery charge Q_{rr} both generate losses that are transfered to Q1 and increase the dissipation in that device. Thirdly, gate charge will impact the MOSFETs' susceptibility to Cdv/dt turn on.

The drain of Q2 is connected to the switching node of the converter and therefore sees transitions between ground and V_{in}. As Q1 turns on and off there is a rate of change of drain voltage dV/dt which is capacitively coupled to the gate of Q2 and can induce a voltage spike on the gate that is sufficient to turn the MOSFET on, resulting in shoot-through current . The ratio of Q_{gd}/Q_{gs1} must be minimized to reduce the potential for Cdv/dt turn on.

Spice model for IRF7805 can be downloaded in machine readable format at www.irf.com.

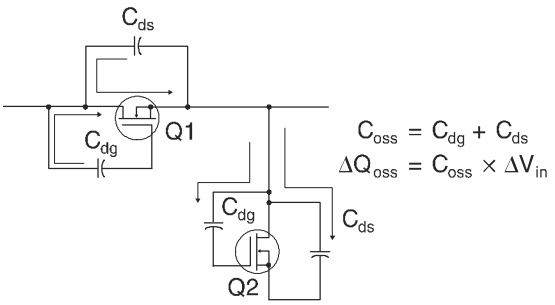


Figure 2: Q_{oss} Characteristic

Typical Characteristics

IRF7805

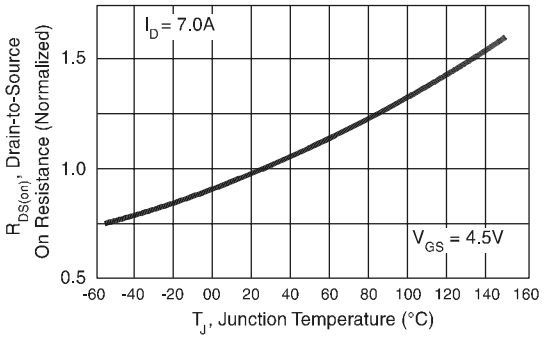


Figure 3. Normalized On-Resistance vs. Temperature

IRF7805A

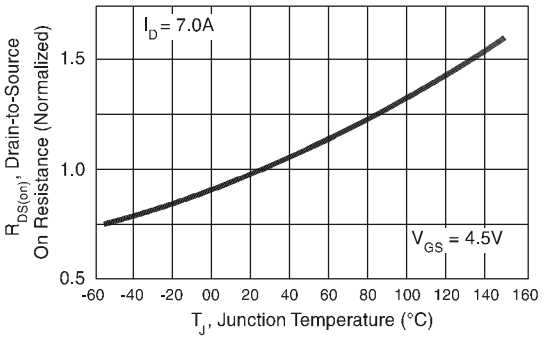


Figure 4. Normalized On-Resistance vs. Temperature

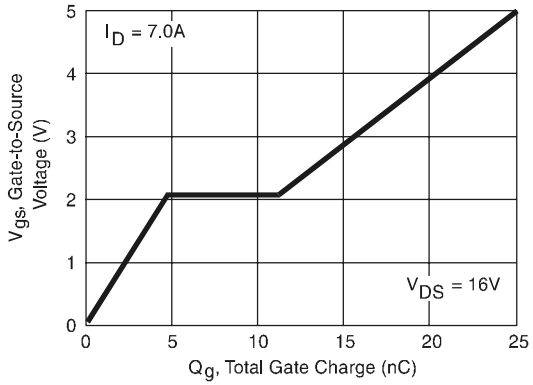


Figure 5. Typical Gate Charge vs. Gate-to-Source Voltage

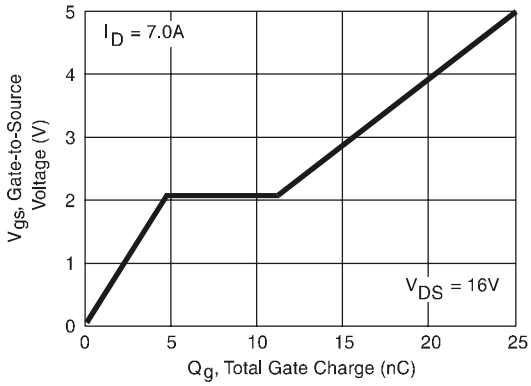


Figure 6. Typical Gate Charge vs. Gate-to-Source Voltage

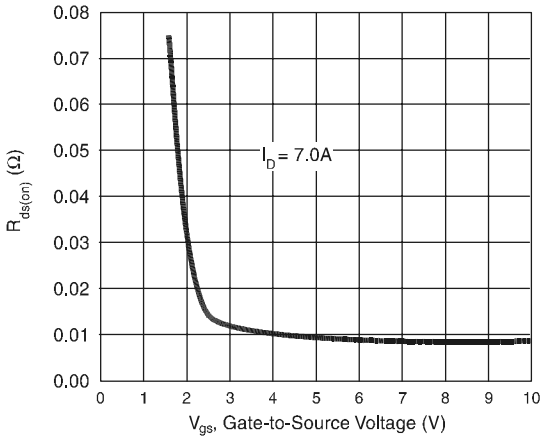


Figure 7. Typical Rds(on) vs. Gate-to-Source Voltage

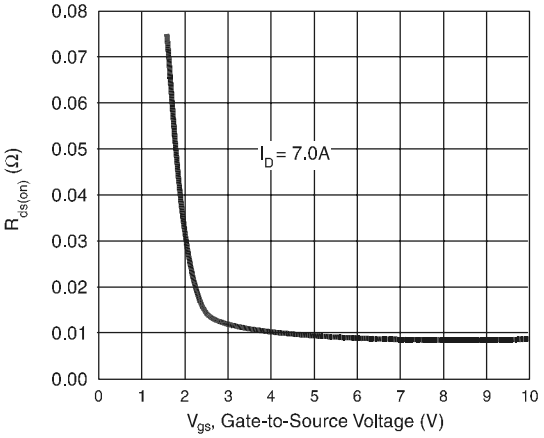


Figure 8. Typical Rds(on) vs. Gate-to-Source Voltage

IRF7805

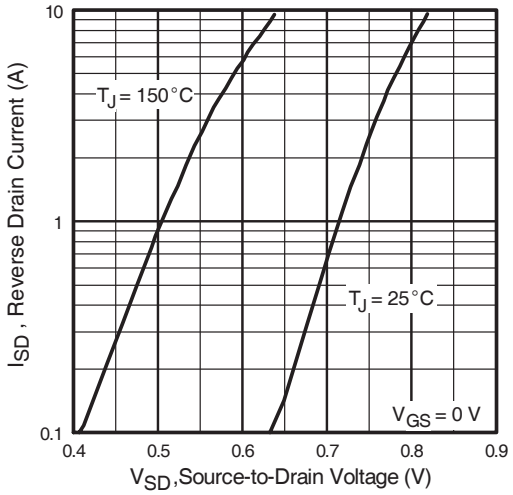


Figure 9. Typical Source-Drain Diode Forward Voltage

IRF7805A

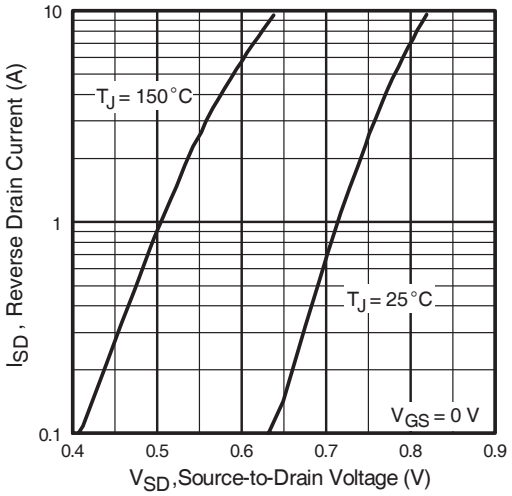


Figure 10. Typical Source-Drain Diode Forward Voltage

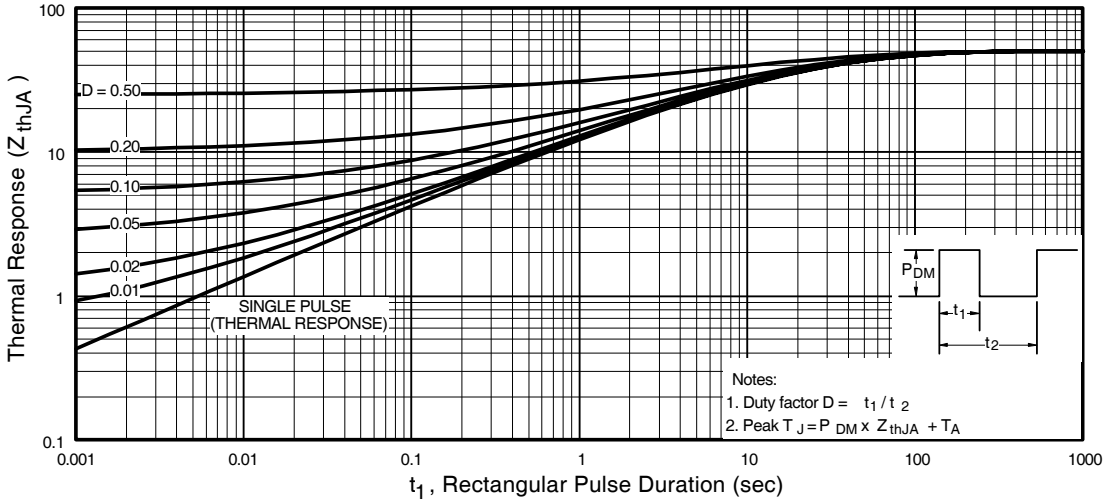
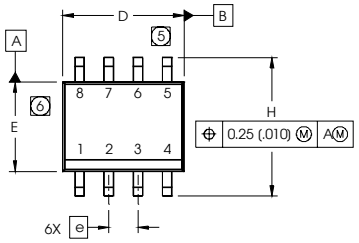
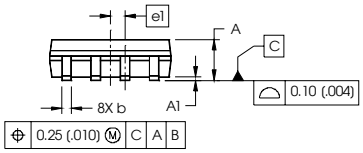


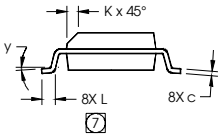
Figure 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

SO-8 Package Outline

Dimensions are shown in milimeters (inches)







DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

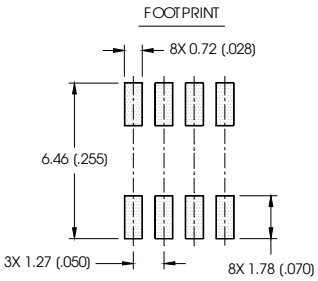
NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
2. CONTROLLING DIMENSION: MILLIMETER
3. DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

5 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).

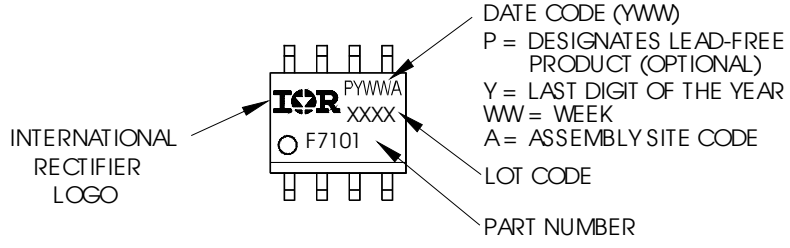
6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).

7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



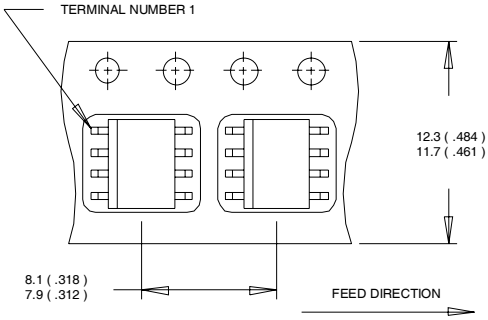
SO-8 Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

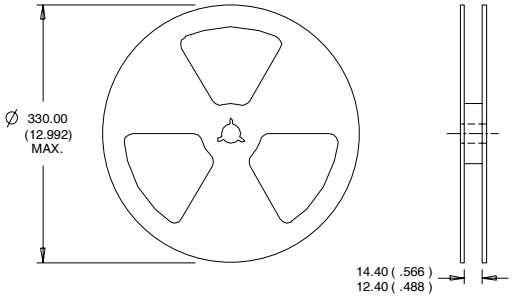


SO-8 Tape and Reel

Dimensions are shown in milimeters (inches)



NOTES:
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Consumer market.
Qualifications Standards can be found on IR's Web site.

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