DATA SHEET

MARCH, 1999
Revision 1.4

LXT980/980A Dual-Speed, 5-Port Fast Ethernet Repeater

with Integrated Management Support

General Description

The LXT980 is a 5-port 10/100 Class II Repeater that is fully compliant with IEEE 802.3 standards. Four ports directly support either 100BASE-TX/10BASE-T copper media or 100BASE-FX fiber media via pseudo-ECL (PECL) interfaces. The fifth port, a 10 or 100 Mbps Media Independent Interface (MII), connects to Media Access Controllers (MACs) for bridge/switch applications. At 100 Mbps, the MII can also be configured to interface to another PHY device, such as the LXT970. This data sheet applies to all LXT980 products (LXT980, LXT980A, and any subsequent variants), except as specifically noted.

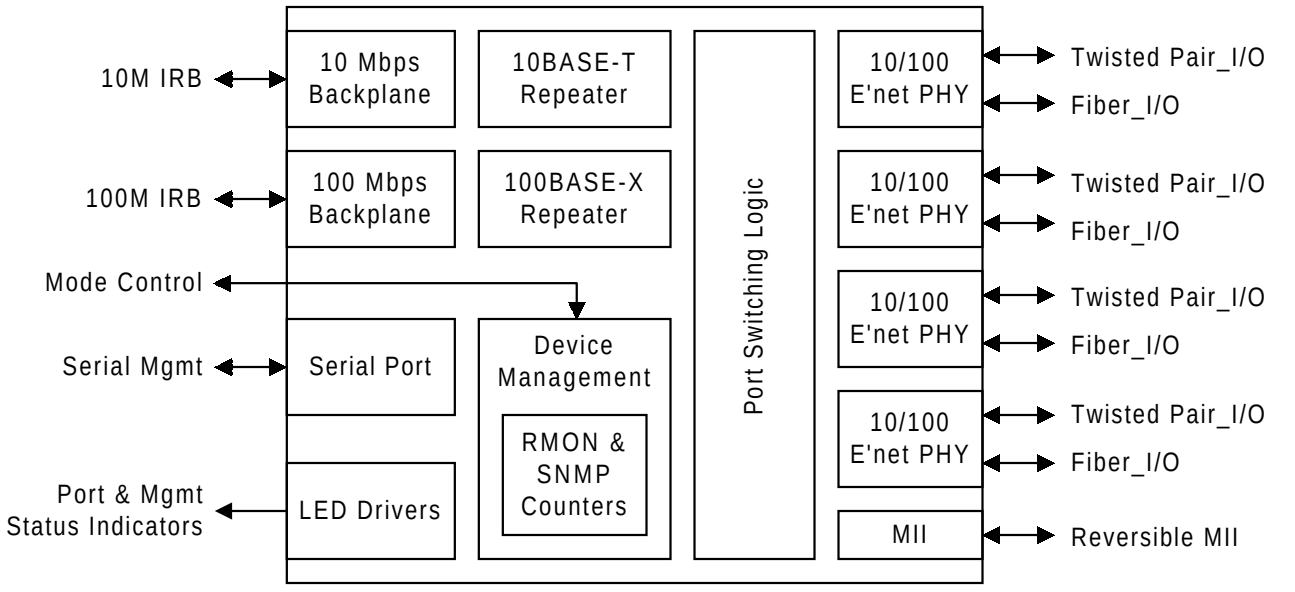
The LXT980 provides auto-negotiation with parallel detection for the four PHY ports. These ports can also be manually configured, either by hardware or software. The LXT980 provides two internal repeater state machines—one operating at 10 Mbps and one at 100 Mbps. Once configured, the LXT980 automatically connects each port to the appropriate repeater.

The LXT980 also provides two Inter-Repeater Backplanes (IRBs) for expansion — one operating at 10 Mbps and one at 100 Mbps. Up to 240 ports can logically be combined into one repeater using these buses. The LXT980 supports SNMP and RMON management via on-chip 32- and 64-bit counters. The counters and control information are accessible via a high-speed Serial Management Interface (SMI). The device supports two Source Address Tracking registers per port and a Source Address Matching Function.

Features

- Four 10/100 ports with complete twisted-pair PHYs including integrated filters and 100BASE-FX PECL interfaces.
- 10/100 MII port connection to either MAC or PHY.
- Independent segments for 10 and 100 Mbps operation.
- Cascadable Inter-Repeater Backplanes (IRBs).
- Hardware assist for RMON and the Repeater MIB.
- High-speed Serial Management Interface (SMI).
- Two address-tracking registers per port.
- Source Address matching function.
- Integrated LED drivers with user-selectable modes.
- Available in 208-pin QFP package.
- Case temperature range: 0-115°C.

LXT980/980A Block Diagram



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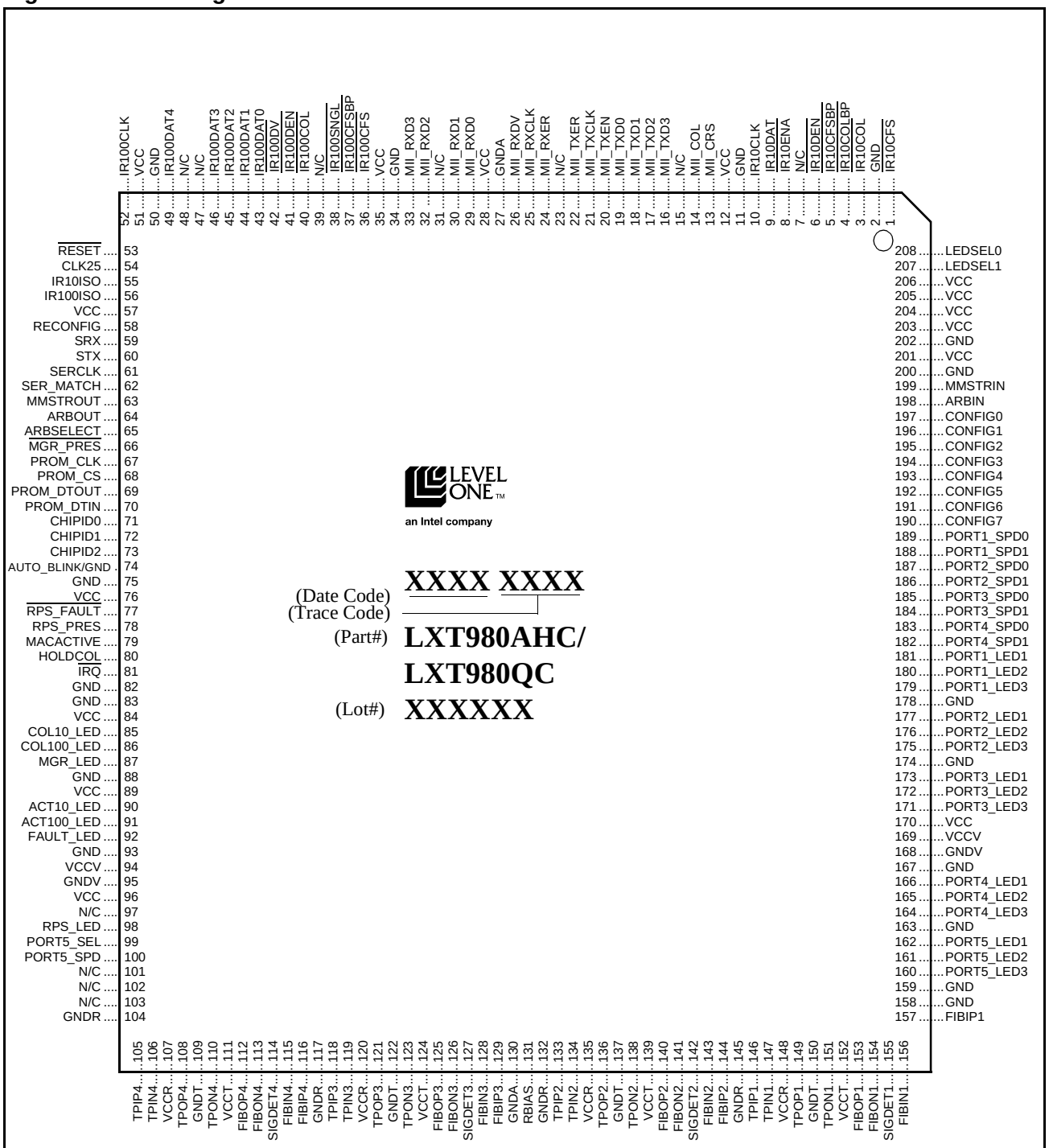
PIN ASSIGNMENTS AND SIGNAL DESCRIPTIONS

Figure 1: Pin Assignments



Note: For Pin 74 Signal Description, see Table 9 on page 13 (**LXT980**) and Table 11 on page 14 (**LXT980A**).

Table 1: Mode Control Signal Descriptions

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type[1]</th><th colspan="3">Description</th></tr>
<tr><td>189
188</td><td>PORT1_SPD0
PORT1_SPD1</td><td rowspan="8">TTL Input, PU, Latched on reset</td><td colspan="3">Speed Select - Ports 1 through 4. These pins set the default value of the Port Speed Control Register for the associated port as follows:</td></tr>
<tr><td>187
186</td><td>PORT2_SPD0
PORT2_SPD1</td><td>SPD1
0
0
1
1</td><td>SPD0
0
1
0
1</td><td>Mode
Allow 10/100 auto-negotiation/parallel detection.
Force 10BASE-T.
Force 100BASE-FX.
Force 100BASE-TX.</td></tr>
<tr><td>185
184</td><td>PORT3_SPD0
PORT3_SPD1</td></tr>
<tr><td>183
182</td><td>PORT4_SPD0
PORT4_SPD1</td></tr>
<tr><td>100</td><td>PORT5_SPD</td><td>TTL Input, PU</td><td colspan="3">Speed Select - Port 5. Selects operating speed of the MII (MAC) interface. Also selects the segment on which statistics are kept.
High = 100 Mbps. Low = 10 Mbps.
(Port 5 speed of 10 Mbps is available when PHY mode is selected.)</td></tr>
<tr><td>99</td><td>PORT5_SEL</td><td>TTL Input, PU</td><td colspan="3">Mode Select - Port 5. Selects operating mode of the MII interface. Pin is monitored at power-up and reset. Subsequent changes have no effect.
High = PHY Mode (LXT980 acts as PHY side of the MII.)
Low = MAC Mode (LXT980 acts as MAC side of the MII.)</td></tr>
<tr><td>197
196
195
194
193
192
191
190</td><td>CONFIG0
CONFIG1
CONFIG2
CONFIG3
CONFIG4
CONFIG5
CONFIG6
CONFIG7</td><td>TTL Input, PD</td><td colspan="3">Configuration Register Inputs. These inputs allow the user to store system-specific information (board type, plug-in cards, status, etc.) in the Serial Configuration Register (address AC). This register may be read remotely through the Serial Management Interface (SMI).</td></tr>
</table>

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   TTL = Transistor-Transistor Logic.

Table 2: PHY Mode MII Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	Output TTL	**Receive Data.** The LXT980 transmits received data to the controller on these outputs. Data is driven on the falling edge of MII_RXCLK.
26	MII_RXDV	Output TTL	**Receive Data Valid.** Active High signal, synchronous to MII_RXCLK, indicates valid data on MII_RXD<3:0>.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for PHY mode.

Table 2: PHY Mode MII Interface Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
25	MII_RXCLK	Output TTL	**Receive Clock.** MII receive clock for expansion port. This is a 2.5 or 25 MHz clock derived from the CLK25 input (refer to Table 11).
24	MII_RXER	Output TTL	**Receive Error.** Active High signal, synchronous to MII_RXCLK, indicates invalid data on MII_RXD<3:0>.
22	MII_TXER	Input TTL	**Transmit Error.** MII_TXER is a 100M-only signal. The MAC asserts this input when an error has occurred in the transmit data stream. The LXT980 responds by sending 'Invalid Code Symbols' on the line.
21	MII_TXCLK	Output TTL	**Transmit Clock.** 2.5 or 25 MHz continuous output derived from the 25 MHz input clock.
20	MII_TXEN	Input TTL	**Transmit Enable.** External controllers drive this input High to indicate that data is being transmitted on the MII_TXD<3:0> pins. Tie this input Low if it is unused.
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Input TTL	**Transmit Data.** External controllers use these inputs to transmit data to the LXT980. The LXT980 samples MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Output TTL	**Collision.** The LXT980 drives this signal High to indicate that a collision has occurred.
13	MII_CRS	Output TTL	**Carrier Sense.** Active High signal indicates LXT980 is transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for PHY mode.

Table 3: MAC Mode MII Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
29 30 32 33	MII_RXD0 MII_RXD1 MII_RXD2 MII_RXD3	Input TTL	**Receive Data.** The LXT980 receives data from the PHY on these pins. Data is sampled on the rising edge of MII_RXCLK.
26	MII_RXDV	Input TTL	**Receive Data Valid.** The PHY asserts this active High signal, synchronous to MII_RXCLK, to indicate valid data on MII_RXD<3:0>.
25	MII_RXCLK	Input TTL	**Receive Clock.** MII receive clock for expansion port. This is a 25 MHz clock.
24	MII_RXER	Input TTL	**Receive Error.** The PHY asserts this active High signal, synchronous to MII_RXCLK, to indicate invalid data on MII_RXD<3:0>.
22	MII_TXER	Output TTL	**Transmit Error.** The LXT980 asserts this signal when an error has occurred in the transmit data stream.
21	MII_TXCLK	Input TTL	**Transmit Clock.** 25 MHz continuous input clock. Must be supplied from same source as CLK25 system clock.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for MAC mode.

Table 3: MAC Mode MII Interface Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
20	MII_TXEN	Output TTL	**Transmit Enable.** The LXT980 drives this output High to indicate that data is being transmitted on the MII_TXD<3:0> pins.
19 18 17 16	MII_TXD0 MII_TXD1 MII_TXD2 MII_TXD3	Output TTL	**Transmit Data.** The LXT980 drives these outputs to transmit data to the PHY. The device drives MII_TXD<3:0> on the rising edge of MII_TXCLK, when MII_TXEN is High.
14	MII_COL	Input TTL	**Collision.** The PHY asserts this active High signal to notify the LXT980 that a collision has occurred.
13	MII_CRS	Input TTL	**Carrier Sense.** The PHY asserts this active High signal to notify the LXT980 that the PHY is transmitting or receiving.

1. MII interface pins reverse direction based on PHY/MAC mode. Direction listed is for MAC mode.

Table 4: Inter-Repeater Backplane Signal Descriptions

Pin	Symbol	Type[1]	Description
Common IRB Signals			
199	MMSTRIN	TTL Input PD, NC	**Management Master Input.** The Management Master (MM) daisy chain ensures that collisions are counted correctly in multi-board applications. Attach the MMSTRIN input of each device to the MMSTROUT output of the previous device. Ground MMSTRIN of the first or only device.
63	MMSTROUT	TTL Output	**Management Master Output.** MM daisy chain output. In hot-swap applications, a 1 kΩ - 3 kΩ resistor can be used as a by-pass between MMSTRIN and MMSTROUT.
100 Mbps IRB Signals (Refer to Figure 21)			
36	$\overline{\text{IR100CFS}}$	Analog I/O	**100 Mbps IRB Collision Force Sense.** A three-level signal that determines number of active ports on the “logical” repeater. High level (5V) indicates no ports active; Mid level (approx. 2.8V) indicates one port active; Low level (0V) indicates more than one port active, resulting in a collision. This signal requires a 240Ω pull-up resistor, and connects between chips on the same board.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
   OD = Open Drain
   TTL = Transistor-Transistor Logic
   Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 4: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
37	$\overline{\text{IR100CFSBP}}$	Analog I/O NC	**100 Mbps IRB Collision Force Sense - Backplane.** This three-level signal functions the same as IRCFS; however, it connects between chips with ChipID=0, on different boards. $\overline{\text{IR100CFSBP}}$ requires a single 91Ω pull-up resistor on each stack.
38	$\overline{\text{IR100SNGL}}$	Schmitt CMOS I/O PU	**100 Mbps Single Driver State.** This active Low signal is asserted by the device with ChipID = 000 when a packet is being received from one or more ports. This signal should not be connected between boards.
40	$\overline{\text{IR100COL}}$	Schmitt CMOS I/O PU	**100 Mbps Multiple Driver State.** This active Low signal is asserted by the device with ChipID = 000 when a packet is being received from more than one port (collision). It should not be connected between boards.
41	$\overline{\text{IR100DEN}}$	TTL Output OD	**100 Mbps IRB Driver Enable.** This output provides directional control for an external bidirectional transceiver (‘245) used to buffer the 100 Mbps IRB in multi-board applications. It must be pulled up by a 330Ω resistor. When there are multiple devices on one board, tie all $\overline{\text{IR100DEN}}$ outputs together. If $\overline{\text{IR100DEN}}$ is tied directly to the DIR pin on a ‘245, attach the on-board IR100DAT, IR100CLK, and $\overline{\text{IR100DV}}$ signals to the “B” side of the ‘245, and connect the off-board signals to the “A” side of the ‘245.
42	$\overline{\text{IR100DV}}$	Schmitt CMOS I/O OD, PU	**100 Mbps IRB Data Valid.** This active Low signal indicates port activity on the repeater. IR100DV frames the clock and data of the packet on the backplane. This signal requires a 120Ω pull-up resistor.
43 44 45 46 49	IR100DAT0 IR100DAT1 IR100DAT2 IR100DAT3 IR100DAT4	Tri-state Schmitt CMOS I/O PU	**100 Mbps IRB Data.** These bidirectional signals carry data on the 100 Mbps IRB. Data is driven on the falling edge and sampled on the rising edge of IR100CLK. These signals can be buffered between boards.
52	IR100CLK	Tri-state Schmitt CMOS I/O PD	**100 Mbps IRB Clock.** This bidirectional, non-continuous, 25 MHz clock is recovered from received network traffic. Schmitt triggering is used to increase noise immunity. This signal must be pulled to VCC when idle. One 1 kΩ pull-up resistor on both side of a ‘245 buffer is recommended.
56	IR100ISO	TTL Output	**100 Mbps Stack Backplane Isolate.** This output allows one LXT980 per Board the ability to enable or disable an external bidirectional transceiver (‘245). Attach the output to the Enable input of the ‘245. The output is driven High (disable) to isolate the 100 Mbps IRB.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
   OD = Open Drain
   TTL = Transistor-Transistor Logic
   Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 4: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
10 Mbps IRB Signals (Refer to Figure 22)			
9	IR10DAT	CMOS I/O OD, PD	**10 Mbps IRB Data.** Carries data on the 10 Mbps IRB. Data is driven and sampled on the rising edge of the corresponding IRCLK. This signal must be pulled up by a 330Ω resistor. Between boards, this signal can be buffered.
10	IR10CLK	Tri-state Schmitt CMOS I/O PD	**10 Mbps IRB Clock.** This bidirectional, non-continuous, 10 MHz clock is recovered from received network traffic. During idle periods, the output is high-impedanced. Schmitt triggering is used to increase noise immunity.
6	$\overline{\text{IR10DEN}}$	TTL Output OD	**10 Mbps IRB Driver Enable.** This output provides directional control for an external bidirectional transceiver (‘245) used to buffer the IRBs in multi-board applications. It must be pulled up by a 330Ω resistor. When there are multiple devices on one board, tie all $\overline{\text{IR10DEN}}$ outputs together. If $\overline{\text{IR10DEN}}$ is tied directly to the DIR pin on a ‘245, attach the on-board IR10DAT, IR10CLK and $\overline{\text{IR10ENA}}$ signals to the “B” side of the ‘245, and connect the off-board signals to the “A” side of the ‘245.
8	$\overline{\text{IR10ENA}}$	CMOS I/O OD, PU	**10 Mbps IRB Enable.** This active Low output indicates carrier presence on the IRB. A 330Ω pull-up resistor is required to pull the $\overline{\text{IR10ENA}}$ output High when the IRB is idle. When there are multiple devices, tie all $\overline{\text{IR10ENA}}$ outputs together. This signal may be buffered between boards.
3	$\overline{\text{IR10COL}}$	CMOS I/O OD, PU	**10 Mbps IRB Collision.** This output is driven Low to indicate that a collision has occurred on the 10 Mbps segment. A 330Ω resistor is required in each box to pull this signal High when there is no collision. This signal should not be connected between boards and it may not be buffered.
4	$\overline{\text{IR10COLBP}}$	CMOS I/O OD, NC	**10 Mbps IRB Collision - Backplane.** This active Low output has the same function as $\overline{\text{IR10COL}}$, but is used between boards. Attach this signal only from the device with ChipID = 0 to the backplane or connector, **without buffering**. The output must be pulled up by one 330Ω resistor per system.
1	$\overline{\text{IR10CFS}}$	Analog I/O OD	**10 Mbps IRB Collision Force Sense.** This three-state analog signal indicates transmit collision when driven Low. $\overline{\text{IR10CFS}}$ requires a 680Ω, 1% pull-up resistor. Do not connect this signal between boards and do not buffer.
5	$\overline{\text{IR10CFSBP}}$	Analog I/O OD, NC	**10 Mbps IRB Collision Force Sense - Backplane.** Functions the same as $\overline{\text{IR10CFS}}$, but connects between boards. Attach this signal only from the device with ChipID = 0 to the backplane or connector, **without buffering**. This signal requires one 330Ω, 1% pull-up resistor per system.
79	MACACTIVE	TTL Input PD	**MAC Active.** A TTL-level signal. Active High input allows external ASICs to participate in 10 Mbps IRB. Driving data onto the IRB requires that the external ASIC assert MACACTIVE High for one clock cycle, then assert $\overline{\text{IR10ENA}}$ Low. ASIC monitors $\overline{\text{IR10COL}}$ (active Low) for collision. By using MACACTIVE, the repeater—not the MAC—drives the three-level $\overline{\text{IR10CFS}}$ pin.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down.
   I/O = Input / Output.
   OD = Open Drain
   TTL = Transistor-Transistor Logic
   Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 4: Inter-Repeater Backplane Signal Descriptions – continued

Pin	Symbol	Type[1]	Description
55	IR10 ISO	TTL Output	**10 Mbps IRB Isolate.** By using IR10 IS, one LXT980 per board can enable or disable an external bidirectional transceiver (‘245). Attach the output to the Enable input of the ‘245. Driven High (disable) to isolate the 10 Mbps IRB.
80	HOLDCOL	TTL I/O PD	**Hold Collision for 10 Mbps mode.** This active High signal is driven by the device with ChipID = 0 to extend a non-local transmit collision to other devices on the same board. The HOLDCOL signals from different boards should NOT be attached together.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
PU = Input contains pull-up.
PD = Input contains pull-down.
I/O = Input / Output.
OD = Open Drain
TTL = Transistor-Transistor Logic
Even if the IRB is not used, required pull-up resistors must be installed as listed above.

Table 5: Twisted-Pair Port Signal Descriptions

Pin	Symbol	Type	Description
149, 151	TPOP1, TPON1	Analog Output	**Twisted-Pair Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports’ twisted-pair line drivers. These pins can be left open when not used.
136, 138	TPOP2, TPON2		
121, 123	TPOP3, TPON3		
108, 110	TPOP4, TPON4		
146, 147	TPIP1, TPIN1	Analog Input	**Twisted-Pair Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports’ twisted-pair receivers. These pins can be left open when not used.
133, 134	TPIP2, TPIN2		
118, 119	TPIP3, TPIN3		
105, 106	TPIP4, TPIN4		

Table 6: Fiber Port Signal Descriptions

Pin	Symbol	Type	Description
153, 154	FIBOP1, FIBON1	PECL Output	**Fiber Outputs - Ports 1 through 4.** These pins are the positive and negative outputs from the respective ports’ PECL drivers. These pins can be left open when not used.
140, 141	FIBOP2, FIBON2		
125, 126	FIBOP3, FIBON3		
112, 113	FIBOP4, FIBON4		
157, 156	FIBIP1, FIBIN1	PECL Input	**Fiber Inputs - Ports 1 through 4.** These pins are the positive and negative inputs to the respective ports’ PECL receivers. These pins can be left open when not used.
144, 143	FIBIP2, FIBIN2		
129, 128	FIBIP3, FIBIN3		
116, 115	FIBIP4, FIBIN4		
155	SIGDET1	PECL Input	**Signal Detect - Ports 1 through 4.** Signal detect for the fiber ports. These pins can be left open when not used.
142	SIGDET2		
127	SIGDET3		
114	SIGDET4		

Table 7: Serial Management Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
58	RECONFIG	TTL Input PD, NC	**Reconfigure**. This input controls the driving of the clock signal on the high-speed Serial Management Interface (SERCLK). When this input is High, the LXT980 drives SERCLK with a 625 kHz output. When this input is Low, SERCLK is an input to the LXT980. In addition, a Low-to-High transition on RECONFIG causes the LXT980 to drive 13 continuous 0s on the SMI, causing a re-arbitration to occur.
62	SER_MATCH	TTL Output	**Serial Match.** The LXT980 device with ChipID = 0 asserts this active High output whenever it detects a message on the SMI that matches the local Hub ID. Refer to Figure 10 on page 34.
59	SRX	TTL Input, PD	**Serial Receive.** Receive data input for high-speed serial management interface. Must be tied to STX externally. SRX is sampled on the rising edge of SERCLK.
60	STX	TTL Output OD	**Serial Transmit.** Transmit data output for high-speed serial management interface. Must be tied to SRX externally. Data transmitted on STX is compared with data received on SRX. In the event of a mismatch, STX is put in the high impedance state. STX is driven on the falling edge of SERCLK.
61	SERCLK	Tri-state TTL I/O, PD	**Serial Clock.** Clock for serial management interface. Depending on RECONFIG, this pin is either a 625 kHz output or a 0 to 2 MHz input.
198	ARBIN	TTL Input, PD, NC	**Arbitration In/Out**. Used with Chain Arbitration. If used, tie ARBIN to ARBOUT of the previous device. ARBIN at the top of the daisy chain can be connected to ground or to ARBOUT of the SCC. If unused, tie ARBIN High.
64	ARBOUT	TTL Output NC	
65	ARBSELECT	TTL Input PU	**Arbitration Mode Select.** 0 = EEPROM based, 1 = chain based.
66	$\overline{\text{MGR\_PRES}}$	TTL Input NC, PU	**Manager Present.** This signal is sensed at power up and hardware reset. If the signal is High, it indicates that no local manager is present, and the LXT980 enables all ports and sets all LEDs to operate in “hardware mode”. If it is Low, indicating that a manager is present, the LXT980 disables all ports, pending control of network manager.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
   PU = Input contains pull-up.
   PD = Input contains pull-down
   OD = Open Drain
   TTL = Transistor-Transistor Logic.

Table 8: LED Signal Descriptions

Pin	Symbol	Type[1]	Description
208 207	LEDSEL0 LEDSEL1	TTL Input PD	**LED Mode Select**. Must be static. 00 = Mode 1, 01 = Mode 2, 10 = Mode 3
181 177 173 166 162	PORT1_LED1 PORT2_LED1 PORT3_LED1 PORT4_LED1 PORT5_LED1	TTL Output	**LED Driver 1 - Ports 1 through 5.** Programmable LED driver. Active Low. Refer to “Port LEDs” on page 24.
180 176 172 165 161	PORT1_LED2 PORT2_LED2 PORT3_LED2 PORT4_LED2 PORT5_LED2	TTL Output	**LED Driver 2 - Ports 1 through 5.** Programmable LED driver. Active Low. Refer to “Port LEDs” on page 24.
179 175 171 164 160	PORT1_LED3 PORT2_LED3 PORT3_LED3 PORT4_LED3 PORT5_LED3	TTL Output	**LED Driver 3 - Ports 1 through 5.** Programmable LED driver. Active Low. Refer to “Port LEDs” on page 24.
85	COL10_LED	TTL Output	**10 Mbps Collision LED Driver.** Active Low indicates collision on 10Mbps segment.
86	COL100_LED	TTL Output	**100 Mbps Collision LED Driver.** Active Low indicates collision on 100 Mbps segment.
87	MGR_LED	TTL Output	**Manager Present LED Driver.** Active Low indicates Manager present.
90	ACT10_LED	TTL Output	**10 Mbps Activity LED Driver.** Active Low indicates activity on 10 Mbps segment.
91	ACT100_LED	TTL Output	**100 Mbps Activity LED Driver.** Active Low indicates activity on 100 Mbps segment.
92	FAULT_LED	TTL Output	**Fault LED Driver.** Active Low indicates global fault.
98	RPS_LED	TTL Output	**Redundant Power Supply LED Driver.** Active Low indicates RPS fault.

1. PD = Input contains pull-down.
TTL = Transistor-Transistor Logic

Table 9: Power Supply and Indication Signal Descriptions

Pin	Symbol	Type[1]	Description
12, 28, 35, 51, 57, 76, 84, 89, 96, 170, 201, 203-206	VCC	Digital	**Power Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to digital ground should be supplied for every one of these pins.
2, 11, 34, 50, 75, 82, 83, 88, 93, 158, 159, 163, 167, 174, 178, 200, 202	GND	Digital	**Ground.** Connect each of these pins to digital ground.
74	GND (**LXT980 only**)	Digital	**Ground.** Connect this pin to digital ground. **Note:** For LXT980A, refer to Table 11 on page 14.
94, 169	VCCV	Analog	**VCO Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDV should be supplied for every one of these pins.
95, 168	GNDV	Analog	**VCO Ground**.
111, 124, 139, 152	VCCT	Analog	**Transmitter Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDT should be supplied for every one of these pins.
109, 122, 137, 150	GNDT	Analog	**Transmitter Ground.**
107, 120, 135, 148	VCCR	Analog	**Receiver Supply Inputs.** Each of these pins must be connected to a common +5 VDC power supply. A de-coupling capacitor to GNDR should be supplied for every one of these pins
104, 117, 132, 145,	GNDR	Analog	**Receiver Ground.**
131	RBIAS	Analog	**RBIAS.** Used to provide bias current for internal circuitry. The 100 µA bias current is provided through an external 22.1 kΩ, 1% resistor to GNDA.
27, 130	GNDA	Analog	**Analog Ground.**
78	RPS_PRES	TTL Input PD	**Redundant Power Supply Present.** Active High input indicates presence of redundant power supply. Tie Low if not used.
77	$\overline{\text{RPS\_FAULT}}$	TTL Input PU	**Redundant Power Supply Fault.** Active Low input indicates redundant power supply fault. The state of this input is reflected in the RPS_LED output (refer to Table 8). Tie High if not used.

1. PU = Input contains pull-up.
   PD = Input contains pull-down.
   TTL = Transistor-Transistor Logic.

Table 10: PROM Interface Signal Descriptions

Pin	Symbol	Type[1]	Description
67	PROM_CLK	Tri-State TTL I/O, PD	**PROM Clock.** 1 MHz clock for reading PROM data (ChipID=0). If a PROM is not used, this pin must be tied Low.
68	PROM_CS	Tri-State TTL Output	**PROM Chip Select.** Selects EPROM. Active High signal driven by chip with ID of 0.
69	PROM_DTOUT	Tri-State TTL Output	**PROM Data Output.** Selects read instruction for EPROM. Active High signal driven only by chip with ID of 0.
70	PROM_DTIN	TTL Input, PD	**PROM Data Input.** If PROM not used, input tied Low or High.

1. PD = Input contains pull-down.
TTL = Transistor-Transistor Logic.

Table 11: Miscellaneous Signal Descriptions

Pin	Symbol	Type[1]	Description
53	$\overline{\text{RESET}}$	Schmitt CMOS Input NC	**Reset.** This active Low input causes internal circuits, state machines, and counters to reset (address tracking registers do not reset). On power-up, devices should not be brought out of reset until the power supply has stabilized and reached 4.5V. When there are multiple devices, it is recommended that all be supplied by a common reset that is driven by an ‘LS14 or similar device.
54	CLK25	Schmitt CMOS Input	**25 MHz system clock.** Drive with MOS levels.
71 72 73	CHIPID0 CHIPID1 CHIPID2	TTL Input, PD	**Chip ID.** These pins assign unique ChipIDs to as many as eight devices on a single board. One device on each board must be assigned ChipID = 0.
74	AUTO_BLINK (**LXT980A only**)	TTL Input, PD	**AUTO_BLINK.** Setting this pin High disables the Blink indication that shows a “No Link” condition for Port*n*LED3. **Note:** For LXT980, refer to Table 9 on page 13.
81	$\overline{\text{IRQ}}$	TTL Output OD	**Interrupt request.** Active Low interrupt. Refer to Tables 65 and 71 for criteria and clearing options.
7, 15, 23, 31, 39, 47, 48, 97, 101, 102, 103,	NC	-	**No Connects.** Leave these pins unconnected.

1. NC = No Clamp. Pad will not clamp input in the absence of power.
PD = Input contains pull-down.
TTL = Transistor-Transistor Logic.

FUNCTIONAL DESCRIPTION

Introduction

As a fully integrated IEEE 802.3 repeater capable of 10 Mbps and 100 Mbps functionality, the LXT980 is a very versatile device allowing great flexibility in Ethernet design solutions. Figures 2, 3, and 4 show some typical applications, and Figure 5 shows a more complete I/O circuit. Refer to Application Information (page 38) for specific circuit implementations.

This multi-port repeater provides four 10BASE-T/100BASE-TX/100BASE-FX ports. In addition, there is a bidirectional Media Independent Interface (MII) expansion port that may be connected to either a 10/100 MAC, or to a 100 Mbps PHY.

The LXT980 provides two repeater state machines and two Inter-Repeater Backplanes (IRB) on a single chip—one for 10 Mbps operation and one for 100 Mbps operation. The 100 Mbps repeater fully meets IEEE 802.3 Class II requirements. Each port's operating speed may be selected independent of the other ports. The auto-negotiation capability of the LXT980 allows it to poll connected nodes and configure itself accordingly.

The LXT980 incorporates full RMON support by providing on-chip counters and hardware assistance for a fully managed environment. The segmented backplane simplifies dual-speed operation, and allows multiple devices to be stacked and function as one logical repeater. Up to 240 ports (192 TP ports and 48 MII ports) can be supported in a single cascade.

Figure 2: Typical Managed Repeater Architectures

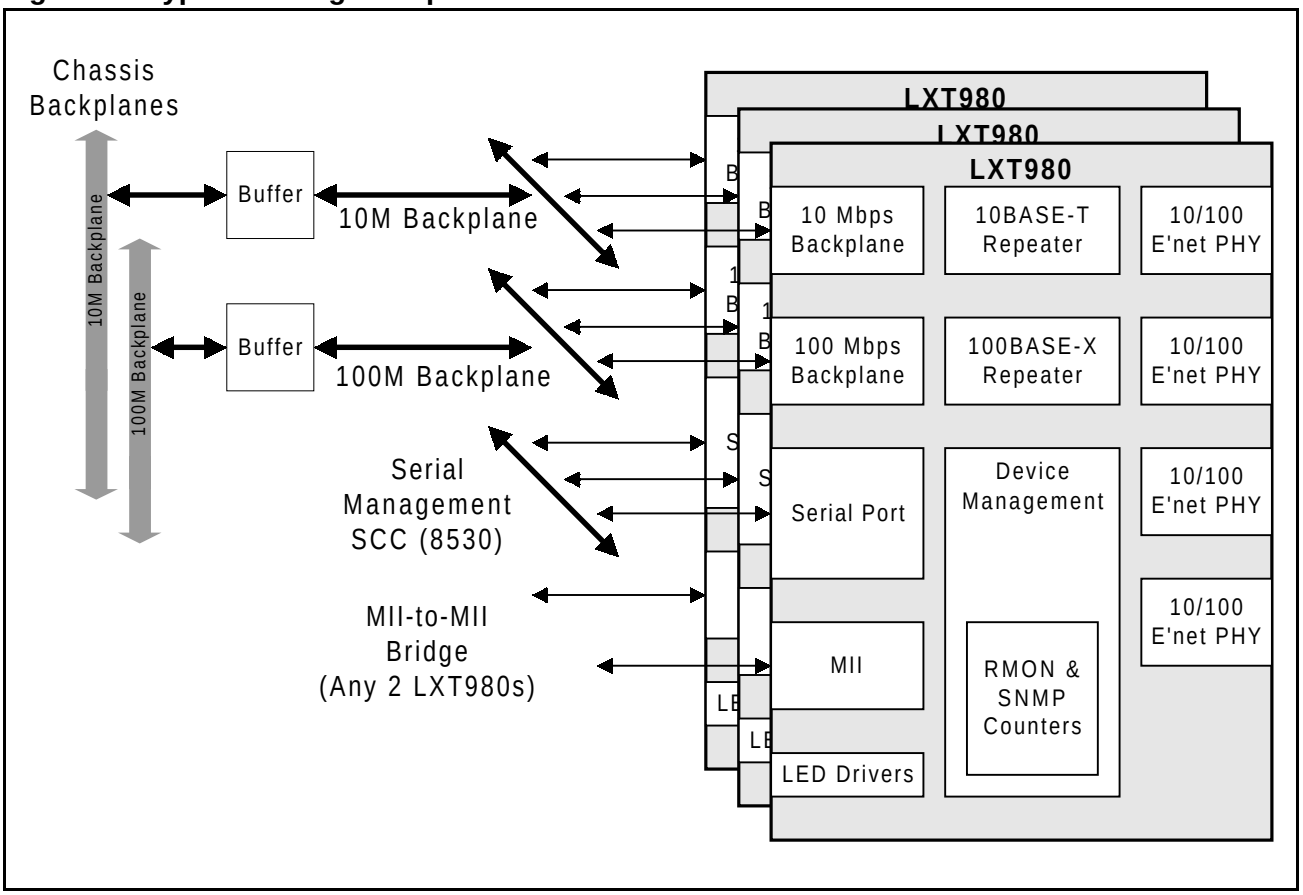


Figure 3: Typical Unmanaged 100 Mbps Repeater Architectures

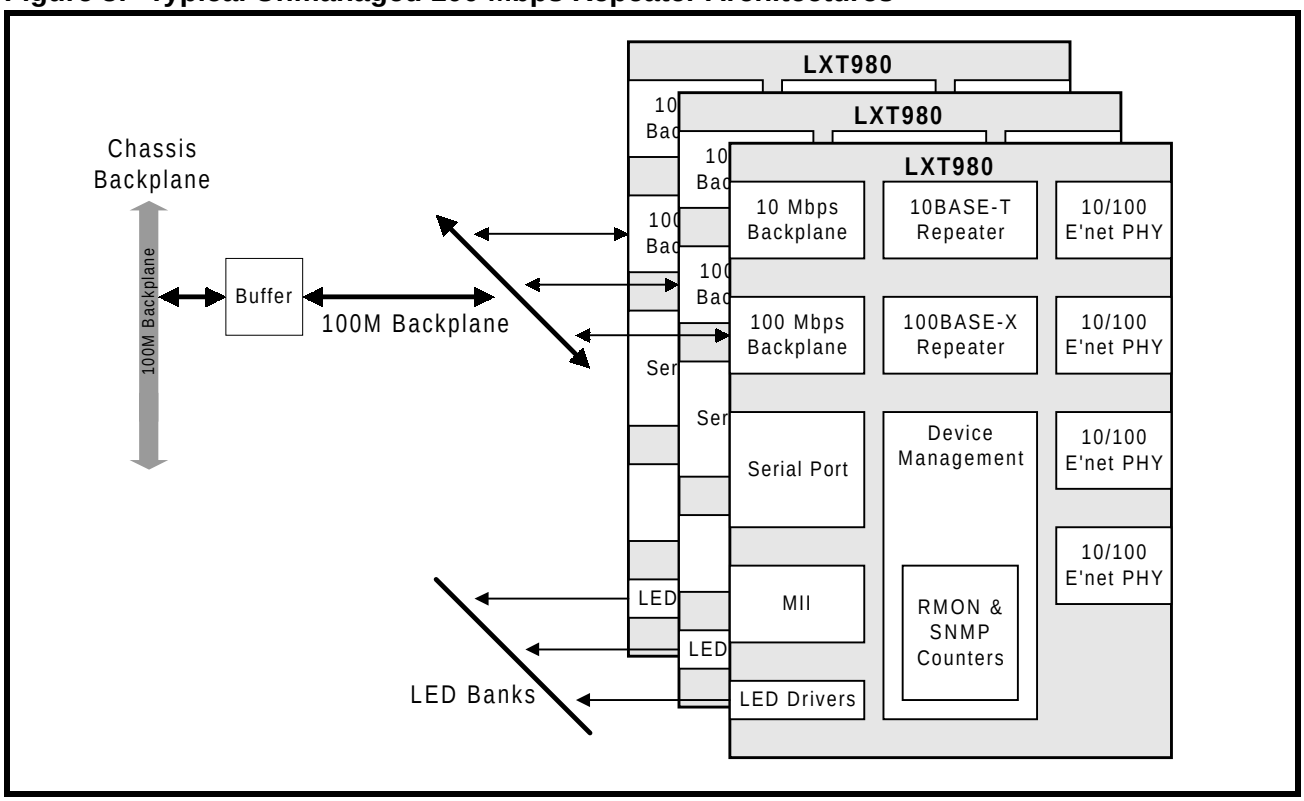


Figure 4: Typical Hybrid Switch/Repeater Application

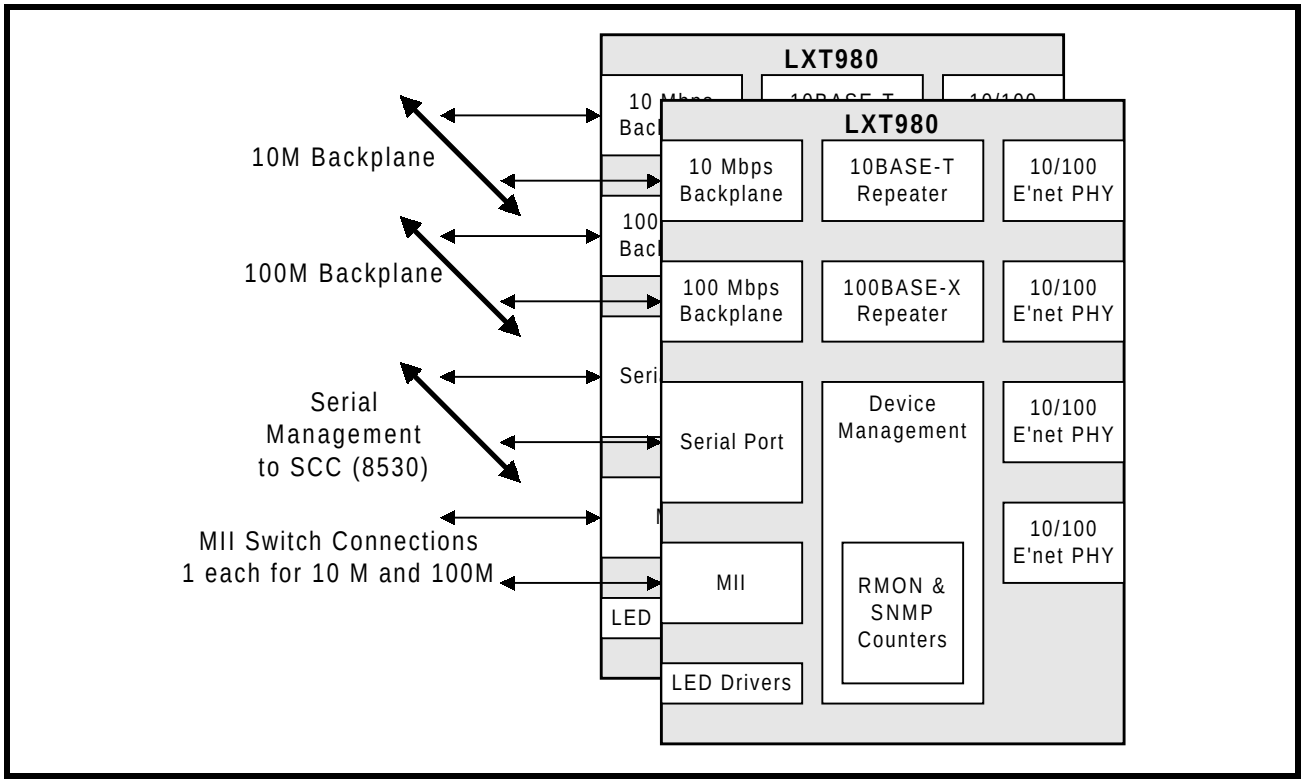
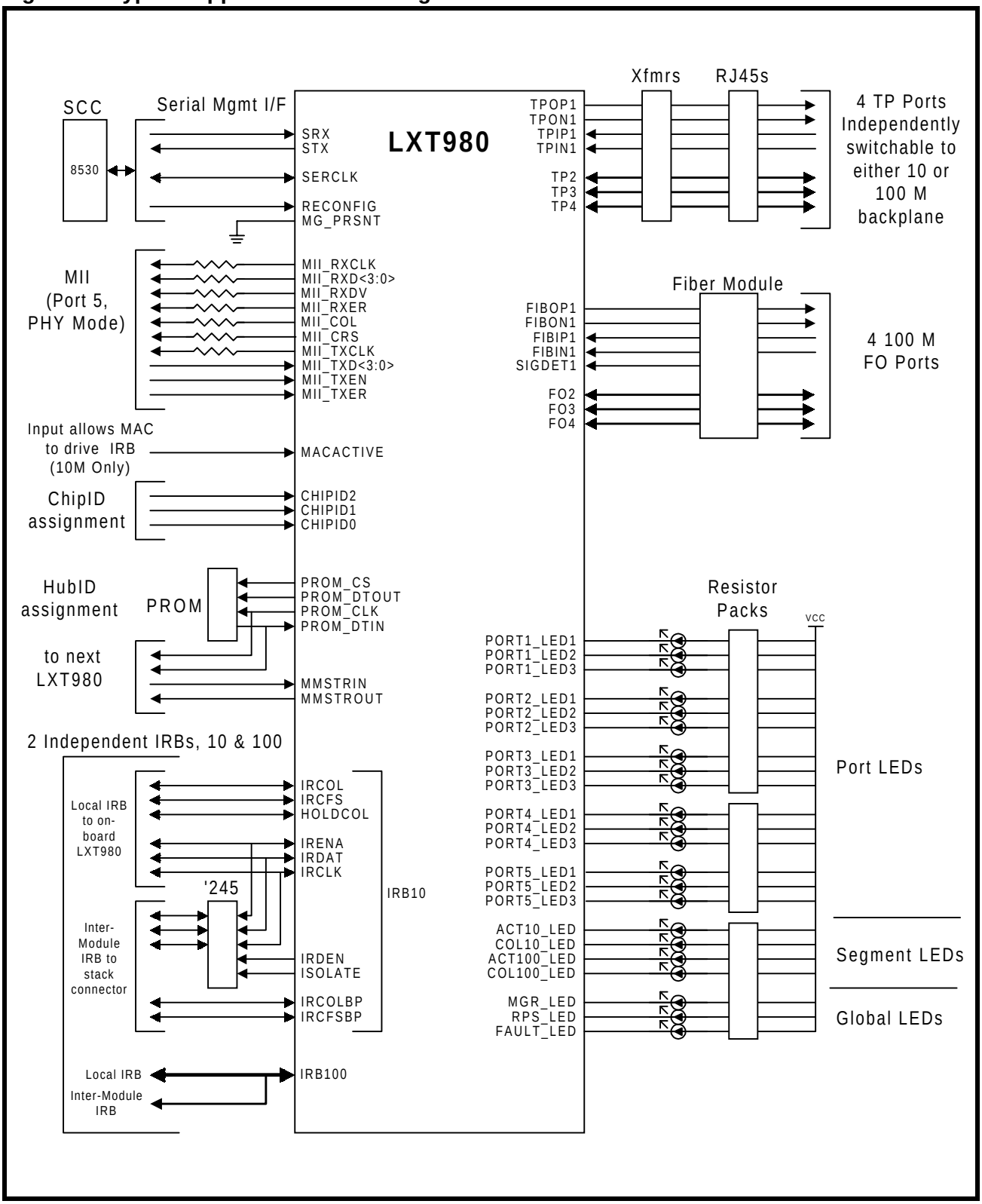


Figure 5: Typical Application Block Diagram



TP/FX Port Configuration

The LXT980 reads the hardware configuration pins at power-up, hardware reset, or software reset (but not at repeater reset), to determine operating conditions for each of its twisted-pair (TP) or fiber (FX) ports. Each port has its own configuration pins so that it can be individually configured. Software can monitor or change the configuration through the Port Speed Control Register (see Table 61 on page 77). The four possible configurations for each port are summarized in Table 12.

Table 12: Manual Speed Selection

SPD1	SPD0	Speed Selection
0	0	Allow 10/100 auto-negotiation/ parallel detection on copper media
0	1	Force port to 10BASE-T mode
1	0	Force port to 100BASE-FX mode
1	1	Force port to 100BASE-TX mode

Forced Operation

A port can be directly configured to operate in one of three modes: 100FX, 100TX, or 10BT. When a port is configured for forced operation via hardware or software, it immediately begins operating in the selected mode. Forced operation is the only way to enable 100FX operation. All links are established as half-duplex only. As a repeater, the LXT980 cannot support full-duplex operation.

Auto-Negotiation

Any port can be configured to establish its link via auto-negotiation. The port and its link partner establish link conditions by exchanging Fast Link Pulse (FLP) bursts. Each FLP burst contains 16 bits of data that advertise the port's capabilities. The FLP bursts sent by the port are maintained in its Auto-negotiation Advertisement Register (Table 81 on page 88). The link partner's abilities are stored in the auto-negotiation link partner register (Table 79 on page 86). Status can be observed in the respective Auto-negotiation Status Register (Table 80 on page 87). Each port has its own advertisement, link partner advertisement, and Auto-negotiation Status Registers.

When auto-negotiation is enabled, the capabilities advertised by the LXT980 are predetermined and cannot be changed; the advertisement register is read only, except for bit 13 (remote fault). The LXT980 always advertises 100 half duplex and 10 half duplex. it never advertises 10 or 100 full-duplex.

If the link partner does not support auto-negotiation, the LXT980 determines link state by listening for 100 Mbps IDLE symbols or 10 Mbps link pulses. If it detects either of these signals, it configures the port and updates the status registers appropriately.

Link Establishment and TP Port Connection

Once a port establishes link, the LXT980 automatically connects it to the appropriate repeater state machine. If link loss is detected and auto-negotiation is enabled, the port returns to the auto-negotiation state.

Changing Port Speed

In order to change port speed while operating, the following sequence is required:

- Disable the port(s) to be changed.
- Set Port Speed Control Register to desired speed.
- Perform a repeater reset (LXT980 will not read hardware configuration pins. Refer to Table 69 on page 81.)
- Re-enable the port(s).

NOTE

The entire repeater must be reset in order to change the port speed on any port.

MII Port Configuration

At power-up or reset, the MII is configured via external pins to one of the three modes of operation:

- 100 Mbps, PHY side of interface—for interfacing to 100 Mbps MAC.
- 10 Mbps, PHY side of interface—for interfacing to 10 Mbps MAC.
- 100 Mbps, MAC side of interface—to drive fifth 100 Mbps port via an LXT970 or other MII-compliant PHY. In this mode, the external PHY must be configured as either a 100-TX or 100-FX connection.

Interface Descriptions

The LXT980 provides four network interface ports. Each port provides both a twisted-pair and a fiber interface. The twisted-pair interface directly supports 100BASE-TX (100TX) and 10BASE-T (10T) Ethernet applications. A common termination circuit is used for both media types. The fiber interface indirectly supports 100BASE-FX (100FX) media through a PECL connection to an external fiber-optic transceiver. Both interfaces fully comply with IEEE 802.3 standards.

Twisted-Pair Interface

The twisted-pair interface for each port consists of two differential signal pairs — one for transmit and one for receive. The transmit signal pair is TPOP/TPON, the receive signal pair is TPIP/TPIN. The twisted-pair interface for a given port is enabled when the port configuration is set to auto-negotiate, forced 10T or forced 100TX operation. The twisted-pair interface is disabled when 100FX is selected.

The transmitter is current driven and requires magnetics with 2:1 turns ratio. A 400 Ω resistive load should be placed across the TPOP/N pair, in parallel with the magnetics. The centertap of the primary side of the transmit winding must be tied to a quiet VCC for proper operation. When the twisted-pair interface is disabled, the transmitter outputs are tri-stated.

The receiver requires magnetics with a 1:1 turns ratio, and a load of 100 Ω. When the twisted-pair port is enabled, the receiver actively biases its inputs to approximately 2.8V. When the twisted-pair interface is disabled, no biasing is provided. A 4 kΩ load is always present across the TPIP/TPIN pair.

When used in 100TX applications, the LXT980 sends and receives a continuous, scrambled 125 Mbaud MLT-3 waveform on this interface. In the absence of data, IDLE symbols are sent and received in order to keep the link up.

When used in 10T applications, the LXT980 sends and receives a non-continuous, 10 Mbaud Manchester-encoded waveform. To maintain link during idle periods, the LXT980 sends link pulses every 16 ms, and expects to receive them every 10 to 20 ms. Each 10BASE-T port automatically detects and sends link pulses, and disables its transmitter if link pulses are not detected. Each receiver can also be configured to ignore link pulses, and leave its transmitter enabled all the time (link pulse transmission cannot be disabled). Each 10BASE-T port can detect and automatically correct for polarity reversal on the TPIP/N inputs. The 10BASE-T interface provides integrated filters using Level One's patented filter technology. These filters facilitate low-cost system designs which meet EMI requirements.

In applications where the twisted-pair interface is not used, the inputs and outputs may be left unconnected.

Fiber Interface

Each fiber interface consists of the FIBOP/FIBON (transmit) and FIBIP/FIBIN (receive) signal pair. Each interface also provides a “Signal Detect” input which can be tied to the corresponding output on the fiber transceiver for determining signal quality.

The transmit pair is biased to approximately 1.5V and generally must be AC-coupled to the transceiver. The receive pair will accommodate an input bias in the 2V-5V range, and can be DC-coupled to the transceiver. Refer to Figure 18 for a typical interface circuit.

The fiber interface for each port is enabled when the speed select is set to 100FX, and is disabled in all other cases. When a fiber port is disabled, its outputs are pulled to ground, and its inputs are tri-stated. The input and output pins on unused fiber ports may be left unconnected.

Each fiber port transmits and receives a continuous, 1V peak-to-peak, non-scrambled, NRZI waveform. The LXT980 does not support scrambling or auto-negotiation on the fiber interface.

Remote Fault Reporting

The SD pin detects signal quality and reports a remote fault if the signal quality starts to degrade. Loss of signal quality also blocks any further data from being received and causes loss of the link. The remote fault code consists of 84 consecutive 1s followed by a single ‘0’, and is transmitted at least three times. The LXT980 transmits the remote fault code and sets the associated interrupts when both of the following conditions are true:

- Fiber mode is selected.
- Signal Detect indicates no signal, or the receive PLL cannot lock.

Media Independent Interface

The LXT980 supports a standard Media Independent Interface (MII). This interface can be programmed to operate as either the PHY or the MAC side of the interface.

When the MII is operating as the MAC side of the interface (MAC mode), it always operates at 100 Mbps. When the MII is operating as the PHY side of the interface (PHY mode), it can be programmed to operate either at 10 Mbps or at 100 Mbps. Once the MII is configured, the LXT980 automatically connects it to the corresponding internal repeater.

NOTE

The MII does not support auto-negotiation, auto-speed, auto-link, or partition functions.

On the LXT980, the MII always operates as a nibble-wide (4B) interface. Symbol mode (5B interface) is not supported on the LXT980 MII.

Serial Management Interface

The Serial Management Interface (SMI) provides system access to the status, control and statistic gathering abilities of the LXT980. This interface is designed to allow multiple devices to be managed from a single multi-drop (daisy-chain) connection, and to use the minimum number of signals (2) for ease of system design.

The interface itself consists of two digital NRZ signals — clock and data. Refer to Table 7 on page 11 for serial management I/F pin assignments and signal descriptions. Data is framed into HDLC-like packets, with a start/stop flag, header and CRC field for error checking. Zero-bit insertion/removal is used. The interface can operate at any speed from 0 to 2 Mbps.

Address assignment is provided via one of two arbitration mechanisms which are activated whenever the device is powered up or reset/reconfigured. Refer to the section on the SMI (page 32).

Repeater Operation

The LXT980 contains two internal repeater state machines — one operating at 10 Mbps and the other at 100 Mbps. The LXT980 automatically switches each port to the correct repeater, once the operational state of that port has been determined. Each repeater connects all ports configured to the same speed (including the MII), and the corresponding Inter-Repeater Backplane. Both repeaters perform the standard jabber, partition, and isolate functions as required.

100 Mbps Repeater Operation

The LXT980 contains a complete 100 Mbps Repeater State Machine (100RSM) that is fully IEEE 802.3 Class II compliant. Any port configured for 100 Mbps operation is automatically connected to the 100 Mbps Repeater. This includes any of the four media ports if they are configured for 100TX or 100FX operation, and the MII port if it is configured for 100 Mbps operation.

The 100 Mbps RSM has its own Inter-Repeater Backplane (100IRB). Multiple LXT980s can be cascaded on the 100IRB and operate as one repeater segment. Data from any port will be forwarded to any other port in the cascade. The 100IRB is a 5-bit symbol-mode interface. It is designed to be stackable.

The LXT980 maintains a complete set of statistics for its local repeater segment as long as the MII port is configured for 100 Mbps operation. These are accessible through the high-speed management interface.

The LXT980 performs the following 100 Mbps repeater functions:

- Signal amplification, wave-shape restoration, and data-frame forwarding.
- Handling of received code violations. The LXT980 will substitute the “H” symbol for all invalid received codes.
- SOP, SOJ, EOP, EOJ delay < 46BT; class II compliant (see Figure 25).
- Collision Enforcement. During a 100 Mbps collision, the LXT980 drives a 1010 jam signal (encoded as Data 5 on TX links) to all ports until the collision ends. There is no minimum enforcement time.
- Partition. The LXT980 partitions any port participating in excess of 60 consecutive collisions or one long collision approximately 575.2 µs long. Once partitioned, the LXT980 continues monitoring and transmitting to the port, but does not repeat data received from the port until it properly un-partitions.
- Un-partition. The LXT980 supports two un-partition algorithms. The default algorithm, which complies with the IEEE 802.3 specification, un-partitions a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.
- The alternate un-partition algorithm is available through the management interface. The alternate algorithm will un-partition a port on *either* transmit or receive of at least 450-560 bits without collision on the partitioned port.
- Isolate. The LXT980 isolates any port transmitting more than two successive false carrier events. A false carrier event is defined as a packet not starting with a /J/K symbol pair. Note: this is not the same as “100IRB isolate,” which involves segmenting the backplane.
- Un-isolate. The LXT980 will un-isolate a port that remains in the IDLE state for 33000 +/- 25% BT or that receives a valid frame at least 450-500 BT in length.
- /T/R generation. The LXT980 can insert a /T/R symbol pair (End of Stream Delimiter) on any incoming packet that does not include one. This feature is optional, and is enabled through the management interface.
- Jabber. The LXT980 ignores any receiver remaining active more than 57,500 bit times. The LXT980 exits this state when all jabbering receivers return to the idle condition.

The isolate and symbol error functions do not apply to the MII port.

10 Mbps Repeater Operation

The LXT980 contains a complete 10 Mbps Repeater State Machine (10RSM) that is fully IEEE 802.3 compliant. Any port configured for 10 Mbps operation is automatically connected to the 10 Mbps Repeater. This includes any of the four media ports if they are configured for 10BT operation, and the MII port if it is configured for 10 Mbps operation.

The 10RSM has its own Inter-Repeater Backplane (10IRB). Multiple LXT980s can be cascaded on the

10IRB and operate as one repeater segment. Data from any port will be forwarded to any other port in the cascade. The 10IRB is 1-bit wide and runs at 10 MHz. It is designed to be stackable.

The LXT980 maintains a complete set of statistics on its repeater segment, as long as the MII port is configured for 10 Mbps operation. These are accessible through the high-speed management interface.

The LXT980 performs the following 10 Mbps repeater functions:

- Signal amplification, wave-shape restoration, and data-frame forwarding.
- Preamble regeneration. All outgoing packets will have a minimum of 56 bits of preamble and 8 bits of SFD.
- SOP, SOJ, EOP, EOJ delays meet requirements of IEEE 802.3 section 9.5.5 and 9.5.6.
- Collision Enforcement. During a 10 Mbps collision, the LXT980 drives a jam signal (“1010”) to all ports for a minimum of 96 bit times and until the collision ends.
- Partition. The LXT980 will partition any port that participates in excess of 32 consecutive collisions. Once partitioned, the LXT980 will continue monitoring and transmitting to the port, but will not repeat data received from the port until it properly un-partitions.
- Un-partition. The LXT980 supports two un-partition algorithms. The default algorithm, which complies with the IEEE 802.3 specification, un-partitions a port when data can be either received or transmitted from the port for 450-560 bit times without a collision on that port.
- The LXT980 also provides an alternate un-partition algorithm, which is available through the management interface. The alternate algorithm will un-partition a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.
- Jabber. The LXT980 will assert a minimum-IFG idle period when any port remains actively transmitting for longer than 40,000 to 75,000 bit times.

Management Support

Configuration and Status

The LXT980 provides management control and visibility of the following functions:

- Reset and Zeroing of counters
- Auto-negotiation (Control, Status, Advertisement, Link Partner)
- Device and Board Configuration
- LED Functions
- Source Address Tracking (per port)
- Source Address Matching (per chip)
- Device/Revision ID

SNMP and RMON Support

The LXT980 provides SNMP and RMON support through its statistics gathering function. Statistics are gathered on all data that flow through the device for each of the ports, including the MII. The LXT980 also maintains statistics for either the entire 10 or 100 Mbps repeater, depending on the speed setting of the MII port. (Two LXT980s are required to maintain statistics on both repeaters. Since cascaded LXT980s operate as a single logical 10/100 repeater, any device in the cascade maintains the same 10 or 100 repeater statistics as any other device). All statistics are stored as 32- or 64-bit quantities. Per-port counters include:

Readable Frames	Readable Octets	FCS Errors
Alignment Errors	FramesTooLong	ShortEvents
Runts	Collisions	LateEvents
VeryLongEvents	DataRateMismatch	AutoPartitions
Broadcast	Multicast	SA Changes
Isolates	Symbol Errors	

Source Address Management

The LXT980 provides two source address management functions for all ports: source address tracking and source address matching. These functions allow a network manager to track source addresses at each port, or to identify any port that sourced a particular source address.

LED Drivers

The LXT980 provides 23 LED drivers:

- 3 mode-selectable port LED drivers (15 total)

- 2 segment LED drivers (4 total)
- 4 global LED drivers

Refer to Table 8 on page 12 for LED Interface pin assignments and signal descriptions.

Requirements

Power

The LXT980 has four types of +5V power supply input pins (VCC, VCCV, VCCR, and VCCT). These inputs may be supplied from a single power supply, although ferrites should be used to filter the power going to the analog and digital power planes. As a matter of good practice, these supplies should be as clean as possible. Specific operating recommendations are shown in the Test Specifications section, Table 25 on page 48.

Each supply input should be decoupled to its respective ground. Refer to Table 6 for power and ground pin assignments, and to "Design Recommendations" on page 38.

Clock

A stable, external 25 MHz system clock source (CMOS) is required by the LXT980. This is connected to the CLK25 pin. Refer to Test Specifications, Table 26 on page 49, for clock input requirements.

Bias Resistor

The LXT980 requires a 22.1 kΩ, 1% resistor connecting its RBIAS input to ground.

Reset

At power-up, the reset input must be held low until VCC reaches at least 4.5V. An 'LS14 or equivalent should be used to drive reset if there are multiple LXT980 devices (See Figure 24 on page 47).

PROM

An external, auto-incrementing 48-bit PROM can be used for two purposes:

- to assign a unique ID to all LXT980s on a board
- to support the EPROM-based address arbitration mechanism on the Serial Management Interface (refer to page 35)

Multiple devices on the same board can share a single common PROM. The LXT980 with ChipID = 0 actively reads the PROM at power-up; all other LXT980s listen in.

If PROM arbitration is not used, the PROM data input signal must be tied either High or Low. Refer to Table 10 on page 14 for PROM interface pin assignments and signal descriptions.

Chip ID

Each LXT980 on a board requires a unique 3-bit Chip ID value asserted on these pins in order for the Serial Management Interface (SMI) to function correctly. One LXT980 on each board must be assigned ChipID = 0.

When Substituting a LXT983 Device

The LXT983 can be substituted in LXT980 designs for a 10/100Mbps unmanaged solution without changing the LXT980 Chip ID pin states. The LXT980 Chip ID 0, Chip ID 1, and Chip ID 2 pins are renamed $\overline{\text{FPS}}$, GND, and GND respectively for the LXT983. For cascading, the first LXT983 device is addressed 000 and all others 001 as indicated by the pin names. The LXT983 requires one chip to have the LXT980-equivalent address 000 and all other LXT983s a non-000 address.

Management Master I/O Link

In multiple device applications, the Management Master daisy chain (MMSTRIN/MMSTROUT) ensures that collisions are counted correctly. Connect the MMSTRIN input to the MMSTROUT output of the previous device, even across board boundaries. Ground the MMSTRIN input of the first or only device in the system. In hot-swap applications, resistive bypassing can be used with a value between 1 and 3 kΩ.

IRB Bus Pull-ups

Even when the LXT980 is used in a stand-alone configuration, pull-up resistors are required on the IRB signals listed below. See Figures 21 and 22 on page 46 for sample circuits.

100 Mbps IRB	10Mbps IRB
IR100CFS	IR10DAT
IR100CFSBP	IR10ENA
IR100DV	IR10COL
IR100CLK	IR10CFS
	IR10COLBP
	IR10CFSBP

LED Operation

The LXT980 provides three types of LED indicators: port, segment, and global (refer to Table 8 on page 12). Three user-selectable LED modes determine pin conditions and how particular conditions are indicated. The LED mode is selected via the LEDSEL<1:0> pins and reflected in an internal register. The LEDs generally operate under hardware control although some limited software overrides are available. In addition to On and Off states, some LED drivers provide a blink state output.

Blink Rates

Two programmable blink rates are provided. The default period for the slow blink rate is 1.6s. The default period is 0.4s for the fast blink rate. These rates may be changed via the LED Timer Register. The slow blink rate is defined by the upper 8 bits and the fast blink rate is defined by the lower 8 bits of the LED Timer Register. Refer to Tables 73-75 on page 84 for details.

Power-Up and Reset Conditions

During reset or power-up, all LED drivers turn on steady and remain on for approximately 2 seconds after reset is cleared. After reset, the Collision, Activity, and Redundant Power Supply LEDs revert to hardware control. The Global Fault and Port LEDs revert to hardware control unless a manager is present in the system.

Port LEDs

Port LEDs provide status for the four twisted-pair ports and the MII port. The LXT980 has 3 LED driver pins for each port as described in Table 8. These pins drive standard LEDs. Three user-selectable modes are provided for the port LEDs. Port LED states are also affected by port speed and auto-negotiation status, see Tables 13 through 15.

Link Loss

During link loss, the Speed LED indicates10M, and the Partition LED indicates “No partition,” regardless of actual partition status.

Software Overrides of Port LEDs

The Port LED Control Register allows limited software overrides of the Port LEDs. Two bits per port provide independent control of each port. However, all three LEDs for the respective port receive the same override (all Port *n* LEDs will be simultaneously set to On, Off, or Blink). Refer to Tables 69 and 74 for coding and bit assignments.

Segment LEDs

These outputs can directly drive LEDs to indicate activity and collision status on a per segment basis. No software overrides are provided for these LED drivers, and they are not affected by LED mode selection. Pulse stretchers are used to extend the on-time for these LEDs.

Collision LEDs

The collision LEDs turn on for approximately 120 µs when the LXT980 detects a collision on the respective 10 Mbps or 100 Mbps segment. During the time that the collision LED is on, any additional collisions are ignored by the collision LED logic.

Activity LEDs

The activity LEDs turn on for approximately 4 ms when the LXT980 detects any activity on the respective 10 Mbps or 100 Mbps segment. During the time that the activity LED is on, any additional activity is ignored by the activity LED logic.

Global LEDs

These LED driver outputs indicate global status conditions.

Manager Present LED

When active, this LED indicates the presence of a manager in the system. It is not affected by LED mode selection and does not allow software overrides.

Global Fault LED

The global fault LED indicates one or more of the following conditions: any port partitioned, any port isolated or RPS fault. How the condition is indicated depends on the LED mode as shown in Tables 13 through 15.

Software Overrides of the Global Fault LED

Two bits in the global LED Control Register allow software overrides to control the global Fault LED. Refer to Tables 69 and 73 on pages 81 and 84 for coding and bit assignments.

Redundant Power Supply LED

The redundant power supply LED is controlled by the RPS_FLT and RPS_PRES pins. The LED state reflects the states of these two inputs, depending on the LED mode selected as listed in Tables 13 through 15.

Table 13: LED Mode 1 Indications

LED	Operating Mode	Hardware Control			Software Control
		On	Blink	Off	
PORT*n*LED1	10 Mbps operation	Link up, not partitioned	N/A	Any other state	Off via Port LED Control Register, address 0B2
	100 Mbps operation	Link up, not partitioned, not isolated	N/A	Any other state	
PORT*n*LED2	10 Mbps operation	Link up, partitioned	N/A	Any other state	
	100 Mbps operation	Link up, partitioned or isolated	N/A	Any other state	
PORT*n*LED3	Auto-neg enabled	100 Mbps link up	No link, (fast blink)[1]	Any other state	
	Auto-neg disabled	100 Mbps link selected, link may be up or down	N/A	Any other state	
RPS	Any	Present, fault	N/A	Any other state	N/A
Global FAULT	Any	Any port partitioned, any port isolated or RPS fault	N/A	Any other state	Off via global LED Control Register, address 0B1

1. Setting AUTO_BLINK (Pin 74) High disables blink (**LXT980A only**).

Table 14: LED Mode 2 Indications

LED	Operating Mode	Hardware Control			Software Control
		On	Blink	Off	
PORT*n*LED1	Any	**10M:** Port enabled, link up, not partitioned **100M:** Port enabled, link up, not partitioned, and not isolated	**10M:** Port enabled, link up, and partitioned **100M:** Port enabled, link (partitioned or isolate) (slow blink)	Any other state	On, Off or fast Blink via Port LED Control Register, Address 0B2
PORT*n*LED2 **(LXT980)**	Any	N/A	N/A	Always off	
PORT*n*LED2 (**LXT980A**)	10 or 100 Mbps ops	Receive activity (20 ms pulse)	N/A	Any other state	
PORT*n*LED3	Auto-neg enabled	100 Mbps link up	No link (fast blink)[1]	10 Mbps link up	
	Auto-neg disabled	100 Mbps selected, link may be up or down	N/A	10 Mbps selected, link may be up or down	
RPS	Any	Present, no fault	Present, fault	Not present	N/A
Global FAULT	Any	N/A	Any port partitioned, any port isolated or RPS fault (slow blink)	Any other state	On, off, or slow blink via global LED Control Register, address 0B1

1. Setting AUTO_BLINK (Pin 74) High disables blink (**LXT980A only**).

Table 15: LED Mode 3 Indications

LED	Operating Mode	Hardware Control			Software Control
		On	Blink	Off	
PORT*n*LED1	10 Mbps operation	Link up, not partitioned	N/A	Any other state	Off via port LED Control Register, address 0B2
	100 Mbps operation	Link up, not partitioned, not isolated	N/A	Any other state	
PORT*n*LED2	10 or 100 Mbps ops	Receive activity (20 ms pulse)	N/A	Any other state	
PORT*n*LED3	Auto-neg enabled	100 Mbps link up	No link (fast blink)[1]	10 Mbps link up	
	Auto-neg disabled	100 Mbps link selected, link may be up or down	N/A	10 Mbps link selected, link may be up or down	
RPS	Any	Present, fault	N/A	Any other state	N/A
Global FAULT	Any	Any port partitioned, any port isolated or RPS fault	N/A	Any other state	Off via global LED Control Register, address 0B1

1. Setting AUTO_BLINK (Pin 74) High disables blink (**LXT980A only**).

IRB Operation

The Inter Repeater Backplane (IRB) allows multiple devices to operate as a single logical repeater, exchanging data collision status information. Each segment on the LXT980 has its own complete, independent IRB. The backplanes use a combination of digital and analog signals as shown in Figure 6. IRB signals can be characterized by connection type as Local (connected between devices on the same board), Stack (connected between boards) or Full (connected between devices on the same board *and* between different boards). Refer to Tables 16 and 17 for details on buffering and pull-up requirements, and to Figures 21 and Figure 22 on page 46 for application circuitry.

MAC IRB Access

The MACACTIVE TTL-level pin allows an external MAC or other digital ASIC to interface directly to the 10 Mbps IRB. When the MACACTIVE pin is asserted, the LXT980 will drive the $\overline{\text{IR10CFS}}$ and $\overline{\text{IR10CFSBP}}$ signals on behalf of the external device, allowing it to participate in collision detection functions.

IRB Isolation

The ISOLATE outputs (IR10ISO and IR100ISO) are provided to control the enable pins of external bidirectional transceivers. In multi-board applications, they can be used to isolate one board from the rest of the system. Only one device can control these signals. The output states of these pins are controlled by the Isolate bits in the Master Configuration Register.

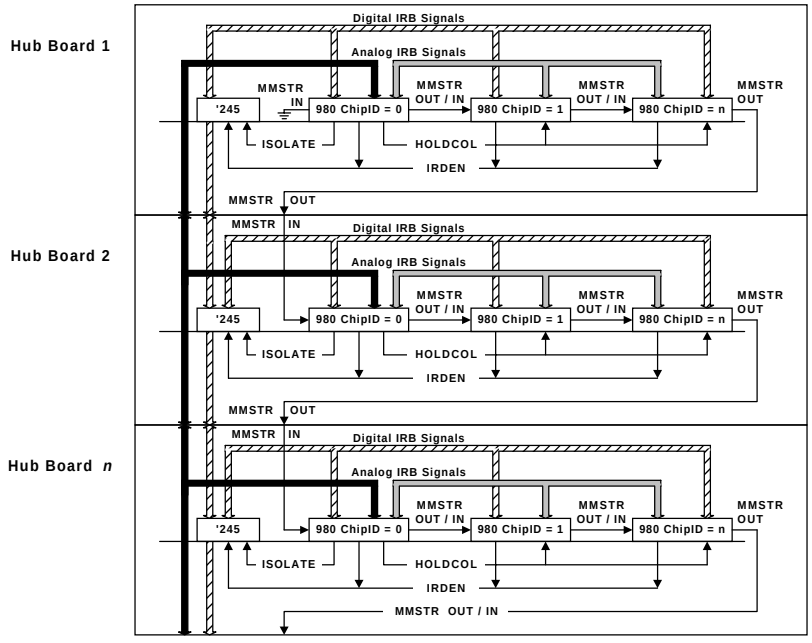
NOTE

Inter-board analog signals will be isolated internally by the device.

MMSTRIN, MMSTROUT

This daisy chain is provided for correct gathering of statistics in multiple-device configurations. In multiple-board applications, this daisy chain must be maintained across boards. In stand-alone applications, or for the first device in a chain, the MMSTRIN input must be pulled Low in order for the management counters to work correctly.

Figure 6: IRB Block Diagram



This diagram shows a single IRB. The LXT980 actually has two independent IRBs, one per speed/segment.

- Digital IRB signals include IRnDAT, IRnENA and IRnCLK.
- Local Analog IRB signals include IRnCOL and IRnCFS.
- Inter-Board Analog IRB signals include IRnCOLBP and IRnCFSBP.

HOLDCOL is used on the 10Mbps IRB Only.

Table 16: IRB Signal Types

Connection Type	Connections Between Devices (same board)	Connections Between Boards
Full	Connect all.	Connect using buffers.
Local	Connect all.	*Do not connect.*
Stack	For devices with ChipID ≠ 0, pull-up at each device and *do not interconnect.*	Connect devices with ChipID = 0 between boards. Use one pull-up resistor per stack.
Special (xxISO)	For devices with ChipID ≠ 0, leave open. For device with ChipID = 0, connect to buffer enable.	*Do not connect.*

Table 17: IRB Signal Details

Name	Pad Type	Buffer	Pull-up	Connection Type
100 Mbps IRB Signals				
IR100DAT<4:0>	Digital	Yes	No	Full
IR100CLK	Digital	Yes	1 kΩ	Full
$\overline{\text{IR100DV}}$	Digital, Open Drain	Yes	120Ω	Full
$\overline{\text{IR100CFS}}$	Analog	No	240Ω, 1%	Local
$\overline{\text{IR100CFSBP}}$	Analog	No	91Ω, 1%[2]	Stack
$\overline{\text{IR100COL}}$	Digital	No	No	Local
$\overline{\text{IR100SNGL}}$	Digital	No	No	Local
$\overline{\text{IR100DEN}}$	Digital, Open Drain	N/A[1]	330Ω	Local
IR100ISO	Digital	N/A[1]	No	Special
10 Mbps IRB Signals				
IR10DAT	Digital, Open Drain	Yes	330Ω	Full
IR10CLK	Digital	Yes	No	Full
$\overline{\text{IR10ENA}}$	Digital, Open Drain	Yes	330Ω	Full
$\overline{\text{IR10CFS}}$	Analog	No	680Ω, 1%	Local
$\overline{\text{IR10CFSBP}}$	Analog	No	330Ω, 1%	Stack
$\overline{\text{IR10COL}}$	Analog	No	330Ω, 1%	Local
$\overline{\text{IR10COLBP}}$	Analog	No	330Ω, 1%	Stack
$\overline{\text{IR10DEN}}$	Digital, Open Drain	N/A[1]	330Ω	Local
IR10ISO	Digital	N/A[1]	No	Special

1. Isolate and Driver Enable signals are provided to control an external bidirectional transceiver.
2. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

MII Port Operation

The LXT980 MII allows a MAC or PHY to directly connect into the repeater environment. The MII port (Port 5) can operate at either 10 or 100 Mbps. The LXT980 maintains the same statistics for this 'Port' as it does for the other 10/100 ports (except for illegal symbols). Utilizing two LXT980s allows the user to have a MAC interface to both the 10 and 100 Mbps segments, in addition to providing segment statistics for both. The LXT980 does *not* provide MDIO/MDC capability, as this is provided via the serial controller interface.

Mode and speed control is provided via PORT5_SPD and PORT5_SEL pins as listed in Table 18.

PHY Mode Operation

PHY Mode is available at both 10 and 100 Mbps. It allows the LXT980 to interface to a 10 or 100 Mbps MAC. When operating at 100 Mbps, the LXT980 passes the full 56 bits of preamble through before sending the SFD. When operating at 10 Mbps, the LXT980 sends data across the MII starting with the 8-bit SFD (no preamble bits).

MAC Mode Operation

MAC Mode (available at 100 Mbps only) allows the user to attach an additional PHY to the LXT980. In this mode the PHY provides both MII_TXCLK and MII_RXCLK. The MII_TXCLK must be frequency-locked to the 25 MHz oscillator used by the LXT980. The LXT980 does not provide an elasticity buffer to compensate for frequency differences. When operating in MAC mode, the LXT980 generates the full 56 bits of preamble before sending the SFD across the MII.

Table 18: MII (Port 5) Mode & Speed Control

PORT5_SPD	PORT5_SEL	Speed & Statistics	Mode
High	Low	100 Mbps	MAC
Low	High	10 Mbps	PHY
High	High	100 Mbps	PHY

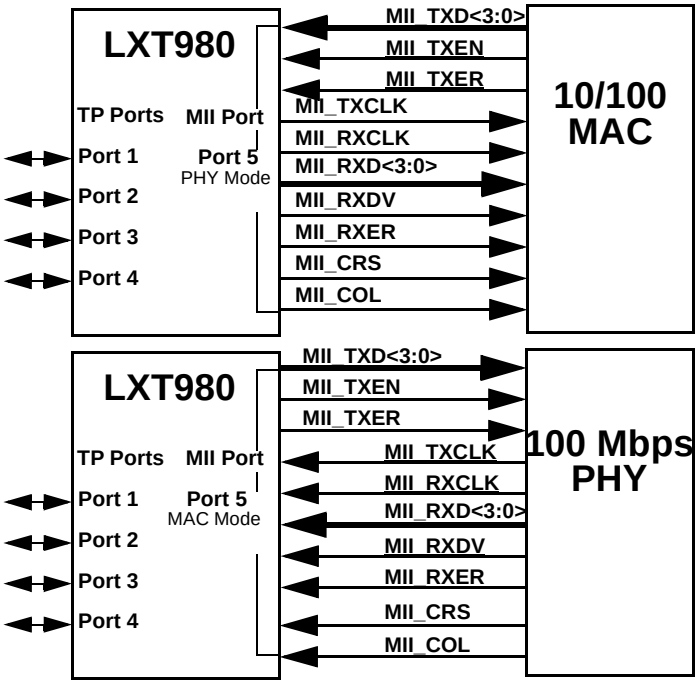
Figure 7: MII (Port 5) Operation

The LXT980 MII port is reversible.

When PHY mode is selected, the LXT980 acts as the PHY side of the MII. In this mode an external MAC sends TX Data to the LXT980 to be repeated to the network. The LXT980 repeats network data to the MAC via the RX Data lines.

When MAC mode is selected, the LXT980 acts as the MAC side of the MII. In this mode the LXT980 repeats network data to the PHY via the TX Data lines.

The external PHY sends data to the LXT980 to be repeated to the network via the RX Data lines.



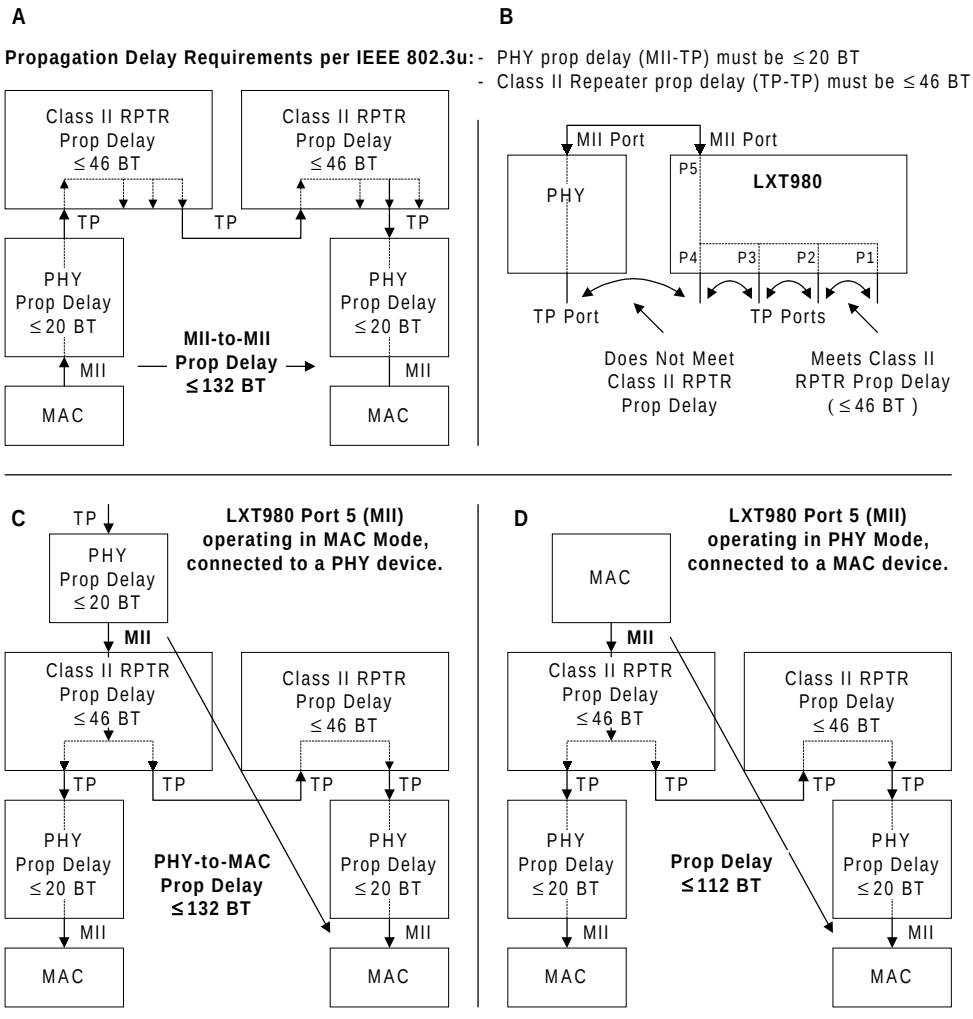
MII Port Timing Considerations

The IEEE 802.3u specification provides propagation delay constraints for standard PHY devices in Section 24.6, and for repeater devices in Section 27. The LXT980 MII port is a hybrid that does not fit either of these categories. The critical consideration that applies to the LXT980 MII port is the overall end-to-end system propagation delay (132 bit times maximum). The LXT980 supports the intent of the Class II repeater application. Figure 8 summarizes the propagation delay issues relevant to the LXT980 MII port.

The LXT980 architecture treats the MII port as a fifth repeater port. The timing delay (latency) from the MII port to any other port meets the requirements for a Class II repeater (≤ 46 BT). It does not meet the requirements for a standard MII-PHY interface (20 - 24 BT). When operating in MAC mode with a PHY connected to the LXT980 MII port (Figure 8B), the fifth TP port does not have the latency characteristics of a Class II repeater with respect to the other ports.

With a MAC connected to the LXT980 MII port (Figure 8D), the maximum latency to any other MAC is 112 BT (not including cable delay). The MAC connected to the LXT980 has an advantage relative to other MACs because it has one less transceiver delay.

Figure 8: MII Timing Issues

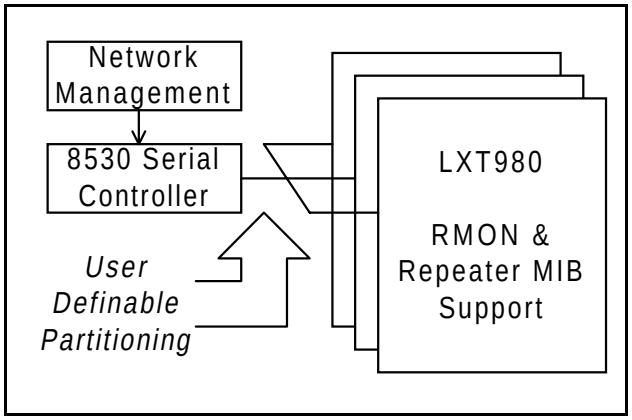


Serial Management I/F

The high-speed Serial Management Interface (SMI) provides access to repeater MIB variables, RMON Statistics attributes and status and control information. A network manager can access the interface through a simple serial communications controller. The interface is designed to be used in a multi-drop configuration, allowing multiple LXT980 devices to be managed from one common line.

The interface consists of a data input line (SRX), data output line (STX), and a clock (SERCLK). It can operate at up to 2 Mbps. The interface operates on a simple command response model, with the network manager as the master and the LXT980 devices as slaves. Figure 9 is a simplified view of typical serial management interface architecture. Refer to Figure 23 on page 47 for circuit details.

Figure 9: Typical Serial Bus Architecture



Serial Clock

SERCLK is a bidirectional pin; direction control is provided by the RECONFIG input. If RECONFIG is High, the LXT980 will drive SERCLK at 625 kHz. If RECONFIG is Low, SERCLK is an input, between 0 and 2 MHz. There is no lower bound to how slow the interface can operate. The clock can be stopped after each operation, as long as an idle (16 ones in a row) is transmitted first.

Serial Data I/O

The serial data pins, SRX and STX, should be tied together. The SRX input is compared with the STX output. If a mismatch occurs, STX goes to a high impedance. STX is driven on the falling edge of SERCLK. SRX is sampled on the rising edge. Refer to Test Specifications (Figure 39 on page 67) for timing information.

Read and Write Operations

Normally the network manager directs read and write operations to a specific LXT980 device using a two-part address consisting of HubID and ChipID. The interface allows up to 127 32-bit registers to be read at one time. Up to two registers can be written at a time.

Some registers may be automatically cleared when subsequent write operations are performed on other registers. Refer to the “Auto-Clearing Registers” section, which follows.

Management Frame Format

The SMI uses a simple frame format, which is shown in Figure 10. Table 19 describes the individual fields. Table 20 shows how the bits for the header field would be stored in memory, assuming that they are transmitted LSB to MSB, low address to high address. Table 21 lists the command set and Table 22 provides a variety of typical packets.

All frames begin and end with a flag of consisting of “01111110”. All fields are transmitted LSB first. Zero-bit stuffing is required if more than five 1s in a row appear in the header, data or CRC fields. In addition, all operations directed to the device must be followed by an idle (ten 1s in a row), and the first operation must be preceded with an idle.

NOTE

The LXT980 uses the CCITT method of CRC (X16 + X12 + X5 +1).

Auto-Clearing Registers

Two registers, the Interrupt Status Register, see Table 64 on page 79 and the Search Port Match Register, see Table 55 on page 74, exhibit an “Auto Clearing” feature.

How Auto Clearing Works

Before executing any write command, the device first reads the most recently accessed register. If the accessed register was an auto-clearing register and set to Auto-Clear Mode, it will be read and cleared.

Example: A read or write command is performed on the Interrupt Status Register. Next, a write command is performed on Port Status Register. The write command to the Port Status Register causes an internal read of the Interrupt Status Register. If the Interrupt Status Register was set to Auto-Clear Mode, it will be

read and cleared—as a result of the write command to the Port Status Register. Because the read and clear is internal (and automatic), the user may not be aware that all data in register 1 is now lost.

NOTE

The Auto-Clear behavior of the Interrupt Status Register and the Search Port Match Register is determined by the auto-clear bit in the Repeater Configuration Register (see Table 70 on page 83).

Preserving Auto-Clearing Register Data

To preserve auto-clearing data in either the interrupt status register or the Search Port Match Register, always follow any read or write command to these registers with a read command to a register that does not auto clear. In other words, do not leave the read pointer on an auto-clearing register.

Example: If you read the interrupt status register (address: 0AE), immediately follow with a "dummy" read of the port link status register (address: 098). This dummy read moves the pointer, ensuring that the information in the interrupt status register is not inadvertently lost through auto clearing. After the "dummy" read, you are now free to go perform any read or write operation without fear of losing data in the auto clearing registers.

NOTE:

There is nothing inherently special about using one particular register for the "dummy" read instead of another. Using the port link status register (in the preceding example) is only a suggestion; a read command to any other register that is not auto-clearing is also acceptable.

Table 19: Serial Management Interface Message Fields

Message	Description
Start or Stop Flag	"01111110". Protocol requires zero insertion after any five consecutive "1"s in the data stream.
Hub ID	Identifies board or sub-system. Assigned by one of two arbitration mechanisms at power-up.
Chip ID	Identifies one of eight LXT980 devices on a board or sub-system. Assigned by 3 external pins on each device.
Command	Identifies the particular operation being performed (see Table 21)
Length	Specifies number of registers to be transferred (1 to 127). Maximum is 2 per write, 127 per read.
Address	Specifies address of register or register block to be transferred.

Figure 10: Serial Management Frame Format

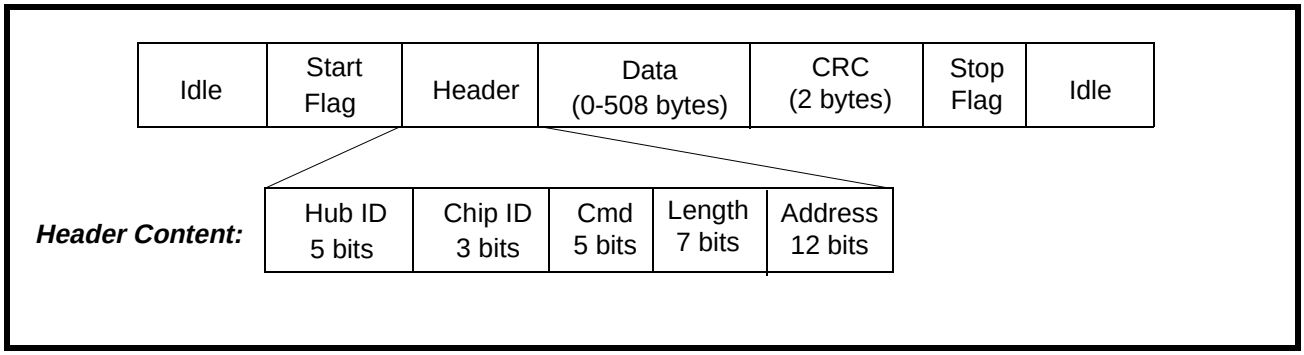


Table 20: Serial Management Header Storage

	MSB							LSB
Increasing Address ↑	Addr 11	Addr 10	Addr 9	Addr 8	Addr 7	Addr 6	Addr 5	Addr 4
	Addr 3	Addr 2	Addr 1	Addr 0	Length 6	Length 5	Length 4	Length 3
	Length 2	Length 1	Length 0	CMD 4	Cmd 3	Cmd 2	Cmd 1	Cmd 0
	ChipID 2	ChipID 1	ChipID 0	HubID 4	HubID 3	HubID 2	HubID 1	HubID 0

Table 21: Serial Management Interface Command Set

Command Value	Name	Usage	Normally Sent By	Description
18 (Hex)	Write	Normal Ops	Network Mgr	Used to write up to 2 registers (8 bytes) at a time.
04 (Hex)	Read	Normal Ops	Network Mgr	Used to read up to 127 registers at a time.
08 (Hex)	Request ID	Arbitration	LXT980	Requests Hub ID. Repeated periodically.
00 (Hex)	ConfigChg	Arbitration	LXT980	Notifies system of configuration change (hot swap). Requests new arbitration phase.
10 (Hex)	Re-arbitrate	Arbitration	Network Mgr	Re-starts arbitration.
14 (Hex)	Assign HubID	Arbitration Mech. 2	Network Mgr	Assigns Hub ID to device with ARBIN=0 and ARBOUT = 1 (top of chain).
0C (Hex)	Set Arbout to 1	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 1.
1C (Hex)	Set Arbout to 0	Arbitration Mech. 2	Network Mgr	Commands specific device to set ARBOUT to 0.
02 (Hex)	DevID	Config	Network Mgr	Asks device to send contents of device revision register.

Interrupt Functions

The LXT980 provides a single open-collector pin for external interrupt signalling. Seven different interrupt conditions may be reported. The Interrupt Status Register identifies the specific interrupt condition (refer to Table 65 on page 79). The Interrupt Mask Register allows specific interrupts to be masked. Interrupts may be cleared in two ways, depending on the status of bit 11 in the Repeater Configuration Register (refer to Table 71 on page 83).

Table 22: Typical Serial Management Packets

Message	Contents of Fields in Serial Management Packet					
	Hub ID	Chip ID	Command	Length	Address	Data
Write [1, 2]	User defined	User defined	18 Hex	01 or 02 Hex	User defined	User defined
Read Request [1, 3]	User defined	User defined	04 Hex	01 to 7F Hex	User defined	Null
Read Response [3]	00000	000	04 Hex	01 to 7F Hex	User defined	Data values
Assign Hub ID (Arb Method 1)	11111	111	18 Hex	02 Hex	188 Hex	Formatted per Table 76
Assign Hub ID (Arb Method 2)	11111	111	14 Hex	01 Hex	000 Hex	Hub ID (LSB) and 27 0s0s
Set Arbout to 0	User defined	User defined	1C Hex	00 Hex	000 Hex	Null
Set Arbout to 1	User defined	User defined	0C Hex	00 Hex	000 Hex	Null
Arb Request	00000	000	08 Hex	02 Hex	190 Hex	PROM ID
Resend Arbitration	11111	111	10 Hex	00 Hex	000 Hex	Null
Resend Arbitration Response	00000	000	08 Hex	02 Hex	190 Hex	EEPROM ID
Device type/ Revision code	User defined	User defined	02 Hex	01 Hex	000 Hex	Null
Device/Revision Response	00000	000	02 Hex	01 Hex	0AD Hex	Device type/ revision

1. Other than checking that the top 3 bits of the address equals 000, the LXT980 does not check if the user writes or reads past the highest location in the data sheet. There are no adverse effects for writing or reading locations above the specified range.
2. If the user performs a write operation of length 1 or 2 and does not send a data field, the LXT980 will write junk into the specified registers. This constitutes an invalid command.
3. If the user reads past the highest location of the LXT980, all those locations will read back 0s. If a read operation is performed with a length of 0, the LXT980 will not respond.

Address Arbitration

Each device has a two part address, consisting of a HubID and a ChipID. The ChipID is assigned by the input pins CHIPID<2:0>. The manager assigns the HubID, and each LXT980 within a particular box will have the same HubID. The Hub ID is assigned through one of two arbitration mechanisms as shown in Figure 11.

EEPROM Arbitration Mechanism

This mechanism requires one serial EEPROM with a unique 48-bit ID on each board. This ID can consist of serial number, date/week/year of manufacture, etc. The ARBSELECT pin must be pulled Low. At power-up, the device with ChipID = 0 reads a 48-bit ID from the PROM. All other devices on the board listen in and record this ID. The device with ChipID = 0 then transmits Arbitration Request messages on the Serial Management Interface (SMI) every 2-3 ms. The request messages from the two boards may collide. If this happens, a resolution scheme ensures that only one message will be transmitted.

The network manager must respond to each request with a message that includes the 48-bit ID and the HubID. All devices hear this message, but only those that match the 48-bit ID receive the HubID as their own. Once a HubID has been assigned to a hub, that hub will cease requesting a HubID. This process continues until all hubs have been assigned an ID. Should a board power off and back on, the hub will re-request an ID, which the manager provides. The command types are assigned so an address arbitration packet will be selected over normal requests.

Chain Arbitration Mechanism

When constructing the stack, the designer should create a daisy chain by tying the ARBOUT pin of each LXT980 to the ARBIN pin of the following LXT980. The manager is at the top of the stack and has control of the ARBIN for the first LXT980. The manager progressively assigns hub IDs using the "Assign Address" and "Set ARBOUT to ZERO" commands. The manager will initially set its ARBOUT (first LXT980's ARBIN) to zero. Since the assign address command only works on the LXT980 that has an ARBIN of 0 and an ARBOUT of 1, the first LXT980 can be assigned an address. After the first LXT980 has been assigned an address, it can uniquely be told to switch its ARBOUT to zero. This creates the (01) condition on the next LXT980 in the line. This LXT980 is then assigned an address and the process continues until all chips have been assigned a unique address. The manager can verify that a hub is still present by performing DEVICE ID commands. If a change of configuration is detected, the manager can perform a broadcast write to return each hub's ARBOUT to 1, and then re-perform the address assignment process.

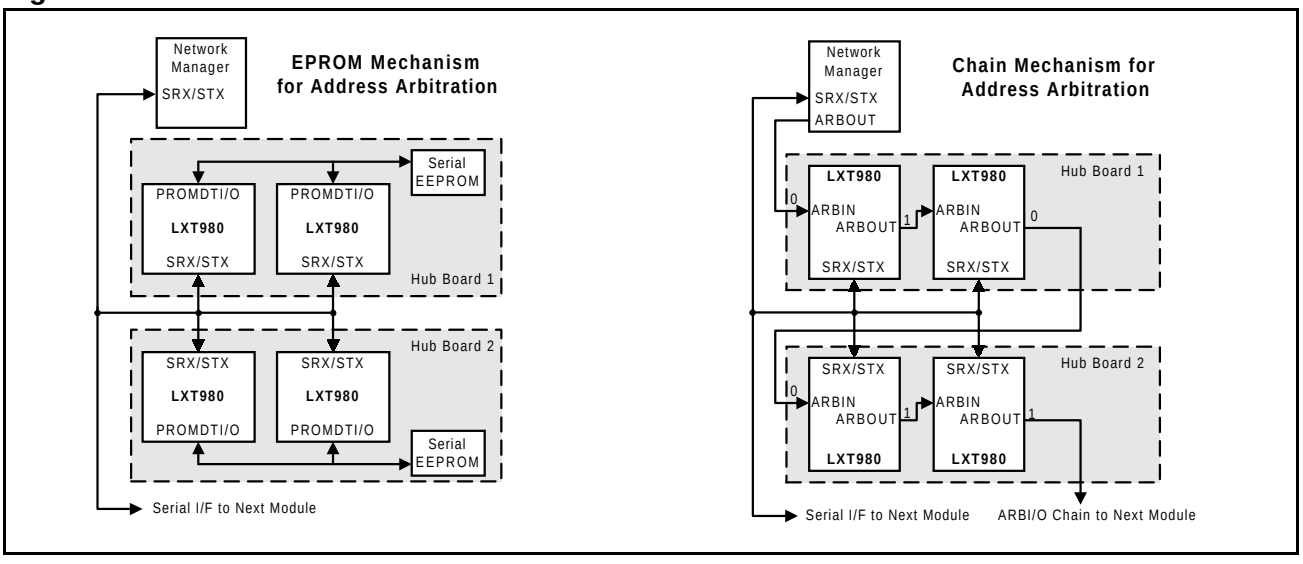
When using the chain arbitration method, set up the daisy chain so that the device with ChipID = 0 is the first device on the board that the chain passes through. Tie to ARBOUT of the SCC or to previous hub in the daisy chain. The first hub ARBIN can also be grounded. When assigning IDs, the first chain bit, located in the Device Revision Register (refer to Table 72 on page 84) can then be used to determine when a new board has been encountered.

Address Re-Arbitration

Two mechanisms for address re-arbitration following a configuration change, such as a hot-swap of a board:

- Manual Re-arbitration. If the LXT980 detects a Low-to-High transition on RECONFIG, or if RECONFIG is High at power-up, it sends out a "Configuration Change" message (all 0s) on the bus, the network manager can use to detect that re-arbitration is required. This message will be sent regardless of arbitration method; however, with "Chain" arbitration mechanism, it will be sent once. The message can be ignored.
- Network Manager. The network manager detects or re-starts arbitration by sending the "Re-arbitrate" command.

Figure 11: Address Arbitration Mechanisms



Serial EEPROM Interface

The serial EEPROM interface has been designed to allow the vendor to load in optional information unique to each board. Items such as serial number or date of manufacture can be placed in the serial EEPROM which is also used in the address arbitration process. Each board must contain a unique set of information. Additionally, only 1 serial EEPROM is required per board, they are not required per chip. The LXT980 reads in the first 48 bits (three 16-bit words) out of the EEPROM and stores them in a register. This read occurs only on power-up as this information is static. Only the LXT980 with a ChipID of 000 will drive the serial EEPROM control lines; all other LXT980s will listen in on the data and clock lines. The first bit to be shifted into the LXT980 from this interface would correspond to bit 47, while the last would be 0. The serial EEPROM shifts out the most significant bit (15) of the word first (the EEPROM must be auto-incrementing).

Figure 12: Serial EEPROM Interface

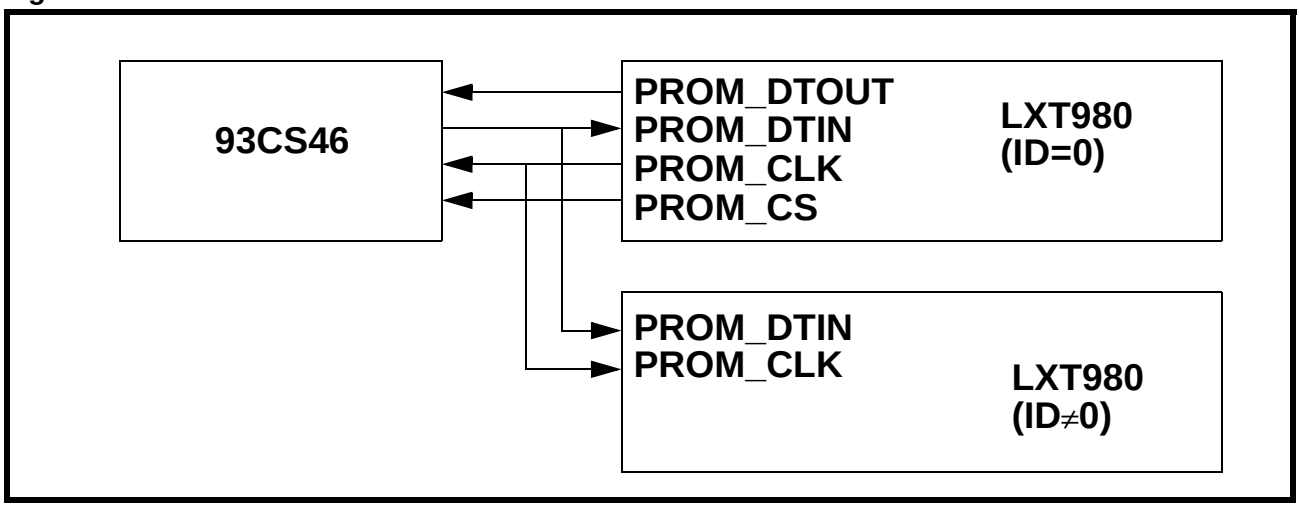
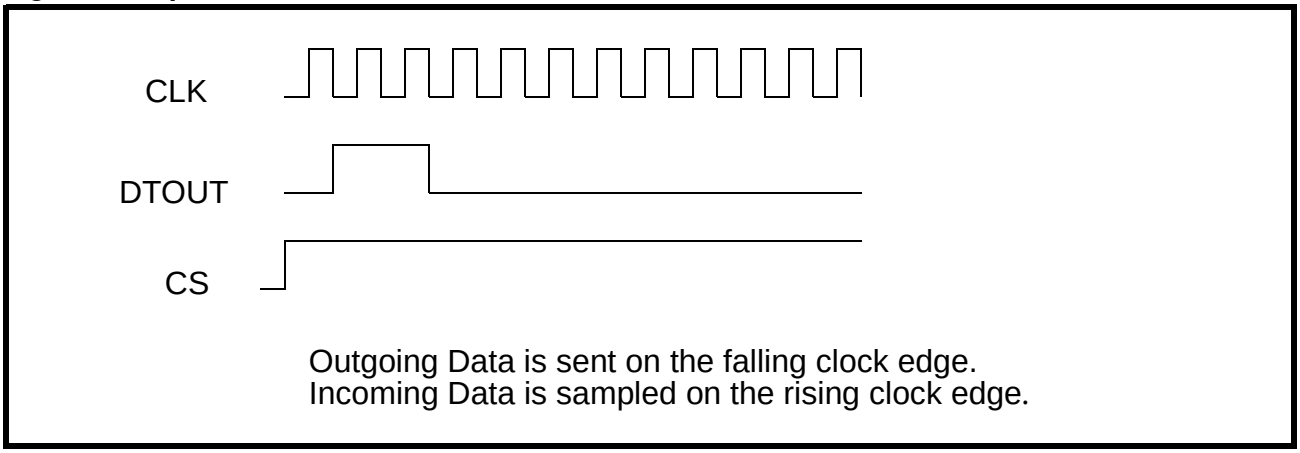


Figure 13: Optional R/W Serial EEPROM Interface



APPLICATION INFORMATION

Design Recommendations

The LXT980 has been designed to comply with IEEE requirements and to provide outstanding receive BER and long-line-length performance. Lab testing has shown that the LXT980 can perform well beyond the required distance of 100m. As with any finely crafted device, reaping the full benefits of the LXT980 requires attention to detail and good design practice.

General Design Guidelines

Adherence to generally accepted design practices is essential to minimize noise levels on power and ground planes. Up to 50 mV of noise is considered acceptable. 50 to 80 mV of noise is considered marginal. High-frequency switching noise can be reduced, and its effects can be eliminated, by following these simple guidelines throughout the design:

- Fill in unused areas of the signal planes with solid copper and attach them with vias to a VCC or ground plane that is not located adjacent to the signal layer.
- Use ample bulk and decoupling capacitors throughout the design (a value of .01 µF is recommended for decoupling caps).
- Provide ample power and ground planes.
- Provide termination on all high-speed switching signals and clock lines.
- Provide impedance matching on long traces to prevent reflections.
- Route high-speed signals next to a continuous, unbroken ground plane.
- Filter and shield DC-DC converters, oscillators, etc.
- Do not route any digital signals between the LXT980 and the RJ45 connectors at the edge of the board.
- Do not extend any circuit power or ground plane past the center of the magnetics or to the edge of the board. Use this area for chassis ground, or leave it void.

Power Supply Filtering

Power supply ripple and digital switching noise on the VCC plane can cause EMI problems and degrade line performance. It is generally difficult to predict in advance the performance of any design, although certain factors greatly increase the risk of having these problems:

- Poorly-regulated or over-burdened power supplies.
- Wide data busses (>32-bits) running at a high clock rate.
- DC-to-DC converters.

Many of these issues can be improved just by following good general design guidelines. In addition, Level One also recommends filtering between the power supply and the analog VCC pins of the LXT980. Filtering has two benefits. First, it keeps digital switching noise out of the analog circuitry inside the LXT980, which helps line performance. Second, if the VCC planes are laid out correctly, it keeps digital switching noise away from external connectors, reducing EMI problems.

The recommended implementation is to divide the VCC plane into two sections. The digital section supplies power to the digital VCC pin, and to the external components. The analog section supplies power to VCCH, VCCT, and VCCR pins of the LXT980. The break between the two planes should run under the device. In designs with more than one LXT980, a single continuous analog VCC plane can be used to supply them all.

The digital and analog VCC planes should be joined at one or more points by ferrite beads. The beads should produce at least a 100Ω impedance at 100 MHz. The beads should be placed so that current flow is evenly distributed. The maximum current rating of the beads should be at least 150% of the current that is actually expected to flow through them. Each LXT980 draws a maximum of 500 mA from the analog supply so beads rated at 750 mA should be used. A bulk cap (2.2 -10 µF) should be placed on each side of each ferrite bead to stop switching noise from traveling through the ferrite.

In addition, a high-frequency bypass cap (.01 µf) should be placed near each analog VCC pin.

Ground Noise

The best approach to minimize ground noise is strict use of good general design guidelines and by filtering the VCC plane.

Power and Ground Plane Layout Considerations

Great care needs to be taken when laying out the power and ground planes. The following guidelines are recommended:

- Follow the guidelines in the *LXT980 Design and Layout Guide* for locating the split between the digital and analog VCC planes.
- Keep the digital VCC plane away from the TPOP/N and TPIP/N signals, away from the magnetics, and away from the RJ45 connectors.
- Place the layers so that the TPOP/N and TPIP/N signals can be routed near or next to the ground plane. For EMI reasons, it is more important to shield TPOP and TPIP/N.

Chassis Ground

For ESD reasons, it is a good design practice to create a separate chassis ground that encircles the board and is isolated via moats and keep-out areas from all circuit-ground planes and active signals. Chassis ground should extend from the RJ45 connectors to the magnetics, and can be used to terminate unused signal pairs ('Bob Smith' termination). In single-point grounding applications, provide a single connection between chassis and circuit grounds with a 2kV isolation capacitor. In multi-point grounding schemes (chassis and circuit grounds joined at multiple points), provide 2kV isolation to the Bob Smith termination.

MII Terminations

Series termination resistors are recommended on all MII signals driven by the LXT980. The proper value = nominal trace impedance minus 13Ω. If the nominal trace impedance is not known, use 55Ω.

The RBIAS Pin

The LXT980 requires a 22.1 kΩ, 1% resistor directly connected between the RBIAS pin and ground. Place the RBIAS resistor as close to the RBIAS pin as possible. Run an etch directly from the pin to the resistor, and sink the other side of the resistor to ground. Surround the RBIAS trace with ground; do not run high-speed signals next to RBIAS.

The Twisted-Pair Interface

Because the LXT980 transmitter uses 2:1 magnetics, system designers must take extra precautions to minimize parasitic shunt capacitance in order to meet return loss specifications. These steps include:

- Use compensating inductor in the output stage (see Figure 20).
- Place magnetics as close as possible to the LXT980.
- Keep transmit pair traces short.
- Do not route transmit pair adjacent to a ground plane. If possible, eliminate planes under the transmit traces completely. Otherwise, keep planes 3-4 layers away.
- Some magnetic vendors are producing magnetics with higher than average return loss performance. Use of these improved magnetics increases the return loss budget available to the system designer.
- Improve EMI performance by filtering the output centertap. A single ferrite bead may be used to supply centertap current to all four ports.

In addition, follow all the standard guidelines for a twisted-pair interface:

- Route the signal pairs differentially, close together. Allow nothing to come between them.
- Keep distances as short as possible; both traces should have the same length.
- Avoid vias and layer changes as much as possible.
- Keep the transmit and receive pairs apart to avoid cross-talk.
- If possible, place entire receive termination network on one side and transmit on the other.
- Keep termination circuits close together and on the same side of the board.
- Always put termination circuits close to the source end of any circuit.
- Bypass common-mode noise to ground on the in-board side of the magnetics using 0.01 µF capacitors.

The Fiber Interface

The fiber interface consists of a pseudo-ECL (PECL) transmit and receive pair to an external fiber optic transceiver. The transmit pair should be AC coupled to the transceiver, and biased to 3.7V with a 50Ω equivalent impedance. The receive pair can be DC-coupled, and should be biased to 3.0V with a 50Ω equivalent impedance. Figure 19 on page 44 shows the correct bias networks to achieve these requirements.

Magnetics Information

The LXT980 requires a 1:1 ratio for the receive transformers and a 2:1 ratio for the transmit transformers. The transformer isolation voltage should be rated at 2 kV to protect the circuitry from static voltages across the connectors and cables. Refer to Table 23 for transformer specifications and *Magnetic Manufacturers for Networking Product Applications* (App. Note 73) for a reference list of compatible magnetic components. Before committing to a specific component, designers should test and validate the magnetics in the specific application to verify that system requirements are met.

Table 23: Magnetics Specifications

Parameter	Min	Nom	Max	Units	Test Condition
Rx turns ratio	–	1 : 1	–	–	
Tx turns ratio	–	2 : 1	–	–	
Insertion loss	0.0	–	1.1	dB	80 MHz
Primary inductance	350	–	–	µH	
Transformer isolation	–	2	–	kV	
Differential to common mode rejection	–	–	-40	dB	.1 to 60 MHz
	–	–	-35	dB	60 to 100 MHz
Return Loss - standard	–	–	-16	dB	30 MHz
	–	–	-10	dB	80 MHz
Return Loss - improved	–	–	-20	dB	30 MHz
	–	–	-15	dB	80 MHz

Typical Application Circuitry

Figures 14 through 17 are simplified block diagrams showing typical applications. Figures 18 through 24 show application circuitry details.

Figure 14: Managed 10/100 Repeater Stack

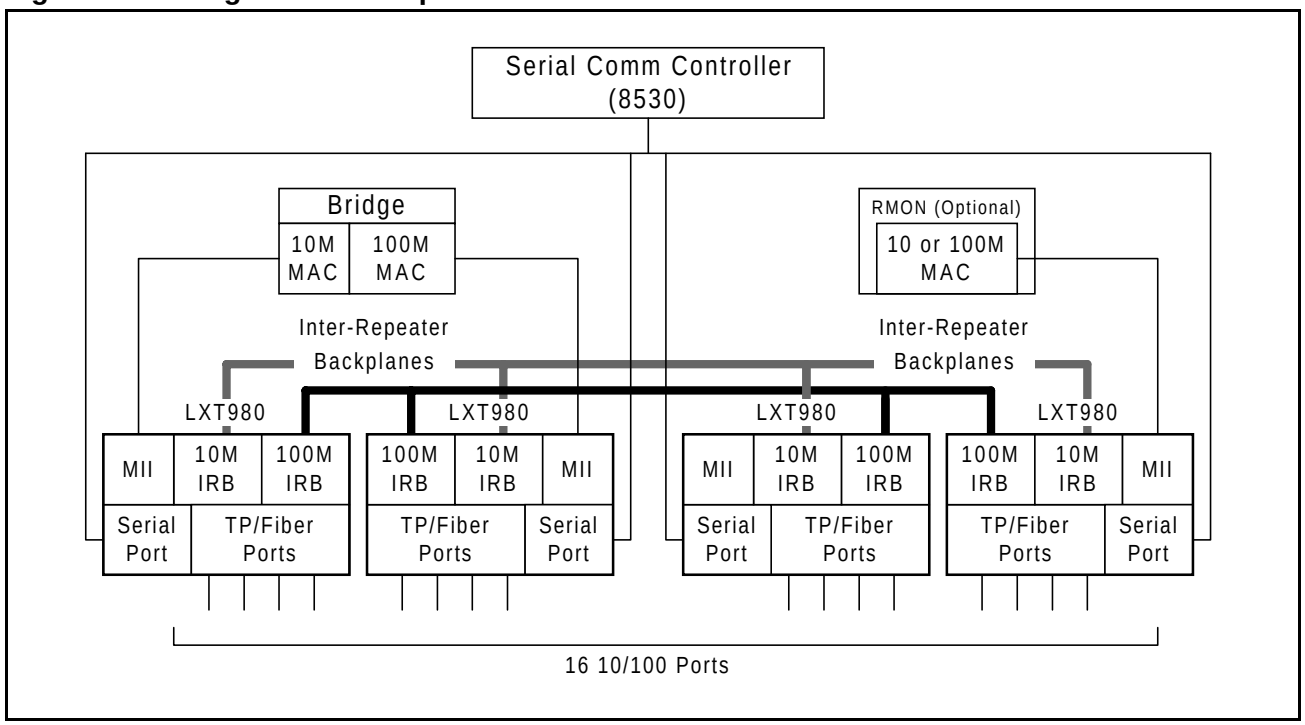


Figure 15: Hybrid Switch/Repeater Application - for Balanced 10/100 Performance

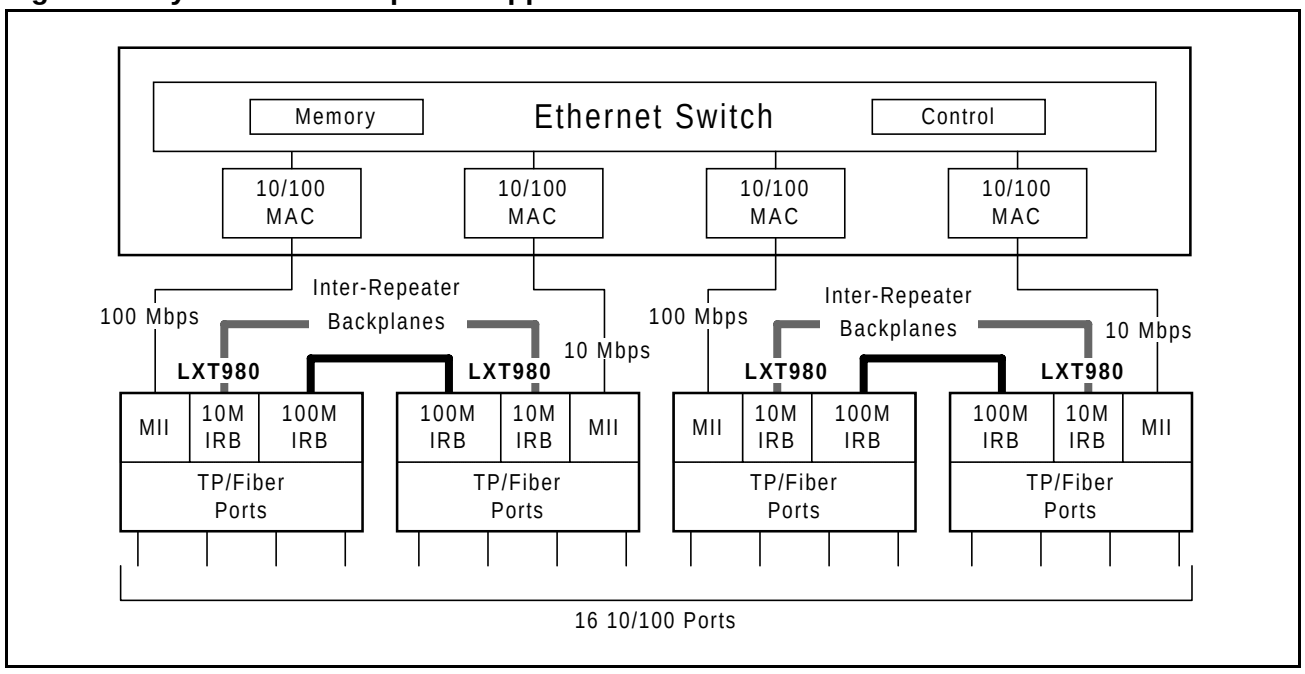


Figure 16: Hybrid Switch/Repeater Application - Weighted Toward 100 Mbps Performance

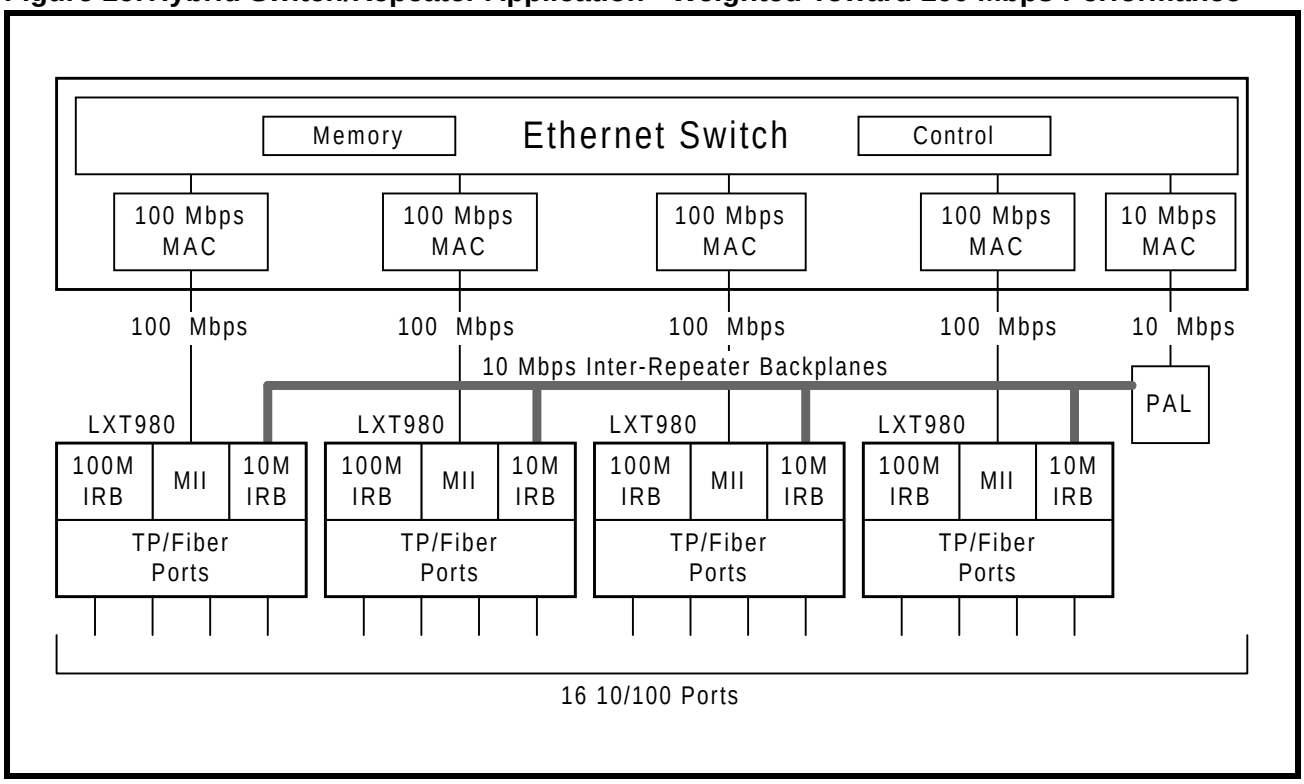


Figure 17: Unmanaged 100-Only Repeater Stack

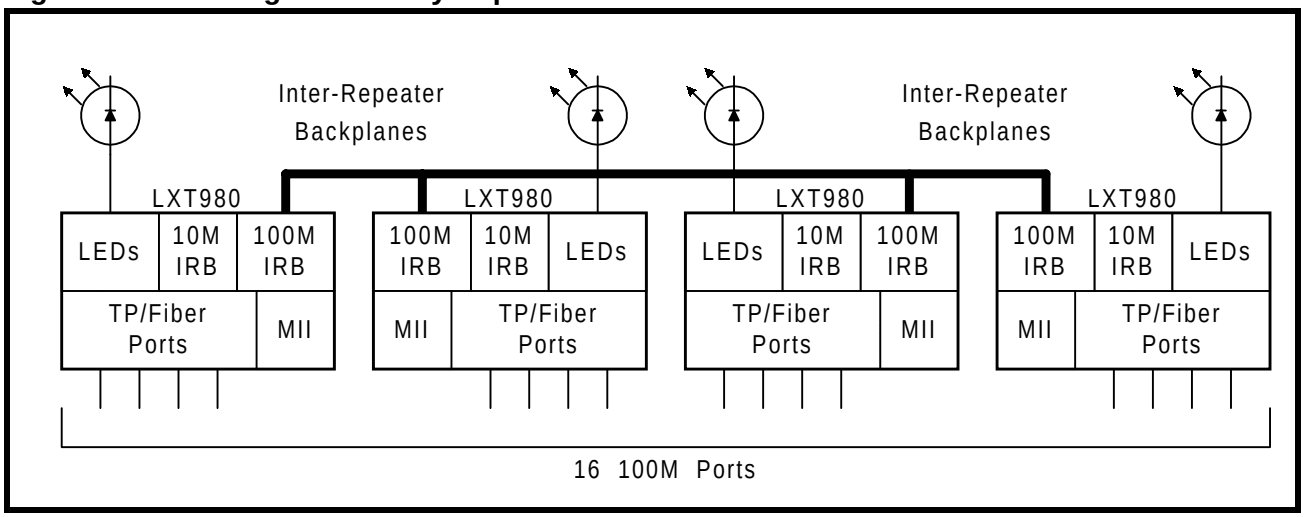


Figure 18: Power and Ground Connections

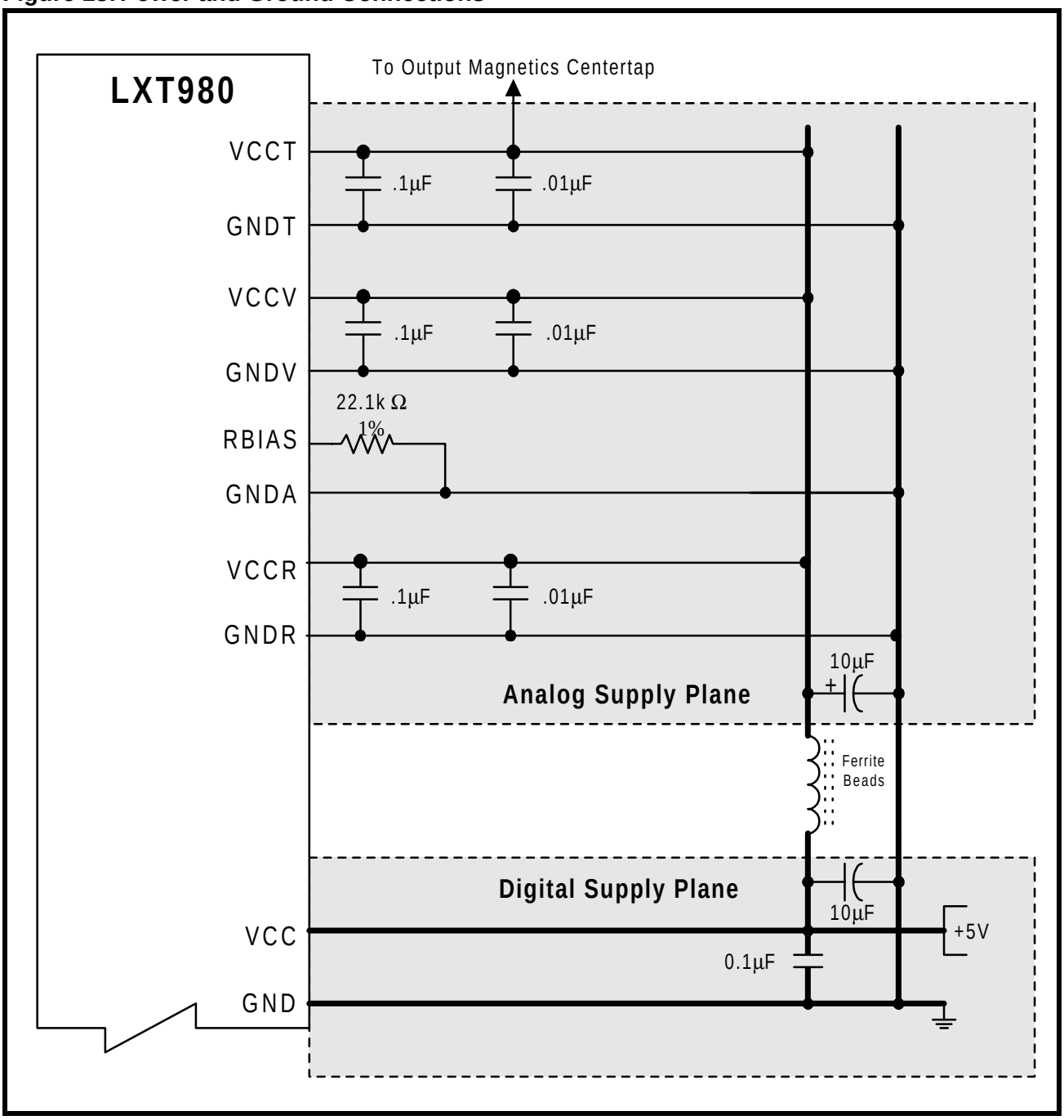
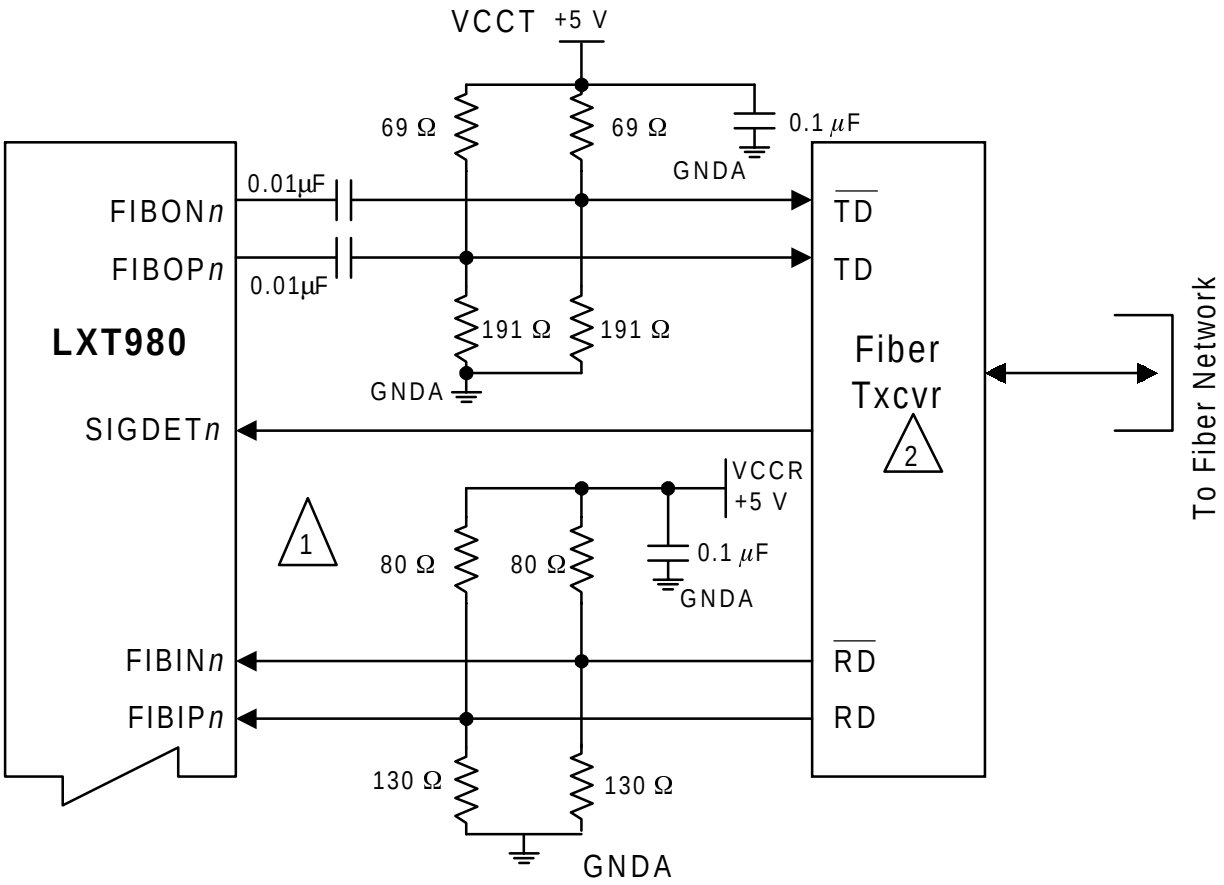


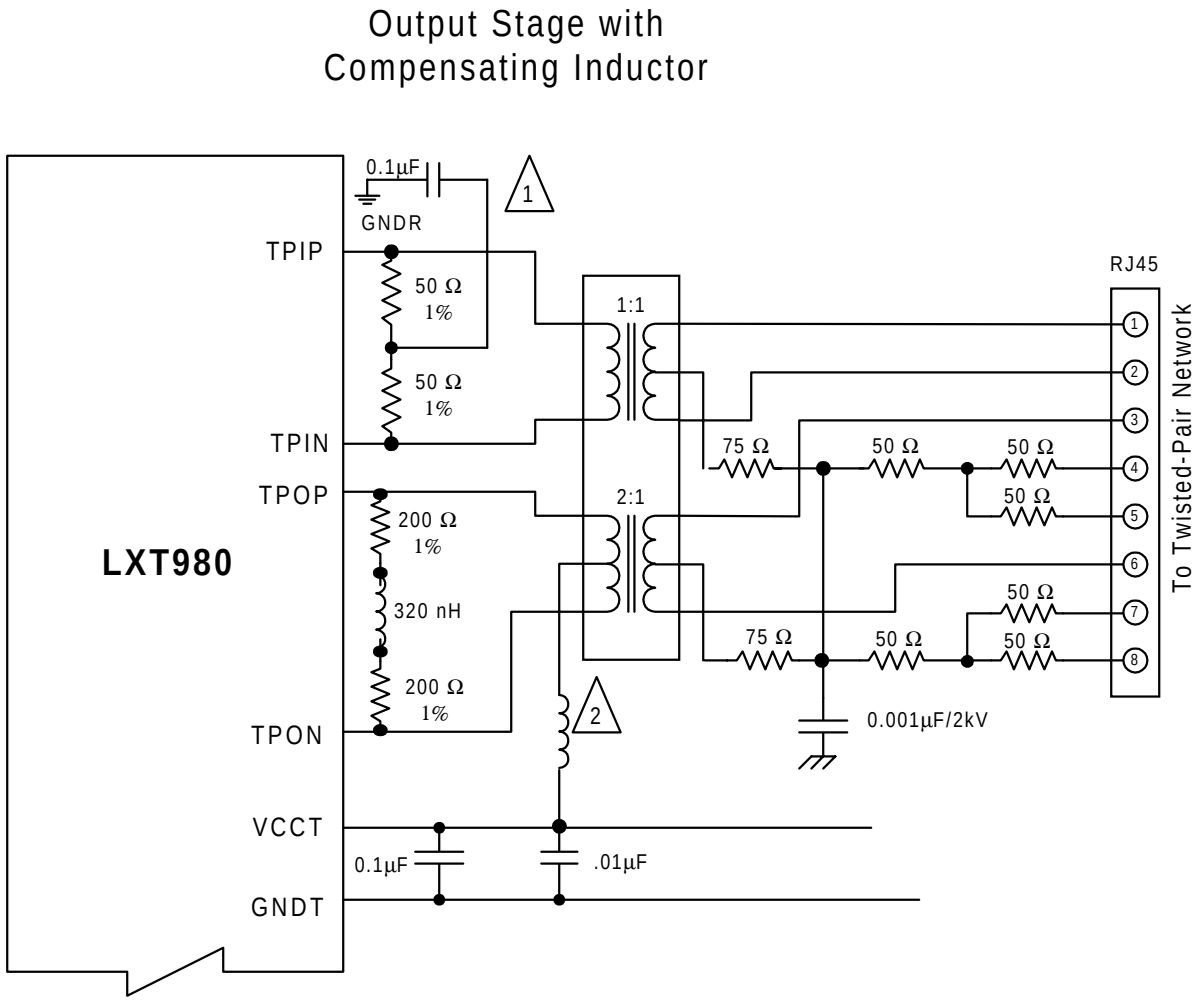
Figure 19: Typical Fiber Port Interface



1. If the Fiber Interface is not used, FIBIN, FIBIP, FIBON, FIBOP and SIGDET may be left unconnected.

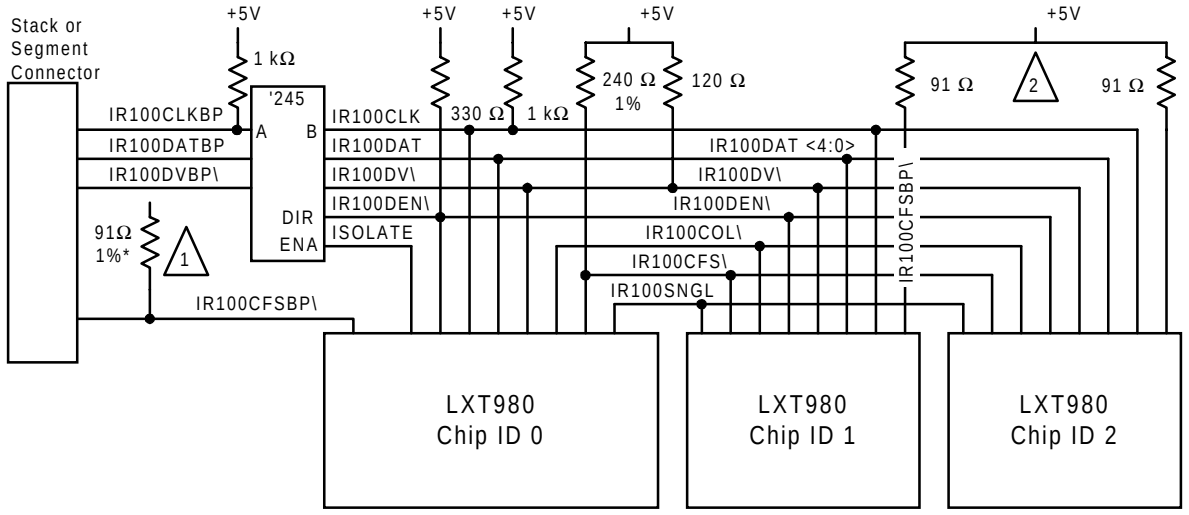
2. Refer to fiber transceiver manufacturers recommendations for termination circuitry.
Suitable fiber transceivers include the HFBR-5103 and HFBR-5105.

Figure 20: Typical Twisted-Pair Port Interface and Power Supply Filtering



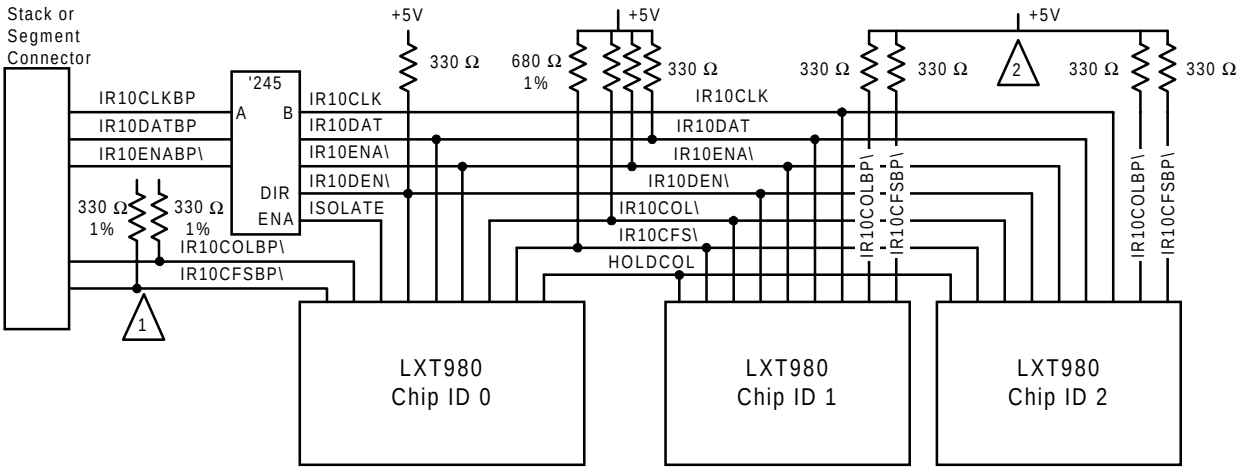
1. Receiver common mode bypass cap may improve BER performance in systems with noisy power supplies.
2. A single ferrite bead may be used to supply centertap current to all 4 ports.

Figure 21: Typical 100 Mbps IRB Implementation



1. In stacked configurations, all devices with ChipID = 0 are tied together at $\overline{\text{IR100CFSBP}}$. The entire stack must be pulled up by only one resistor per signal. Pull-up resistor is installed in the base board only.
2. All devices with ChipID ≠ 0 require individual pull-up resistors at $\overline{\text{IR100CFSBP}}$.
3. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors

Figure 22: Typical 10 Mbps IRB Implementation



1. In stacked configurations, all devices with ChipID = 0 are tied together at $\overline{\text{IR10COLBP}}$ and $\overline{\text{IR10CFSBP}}$. The entire stack must be pulled up by only one resistor per signal. Pull-up resistors are installed in the base board only.
2. All devices with ChipID ≠ 0 require individual pull-up resistors at $\overline{\text{IR10COLBP}}$ and $\overline{\text{IR10CFSBP}}$.

Figure 23: Typical Serial Management Interface Connections

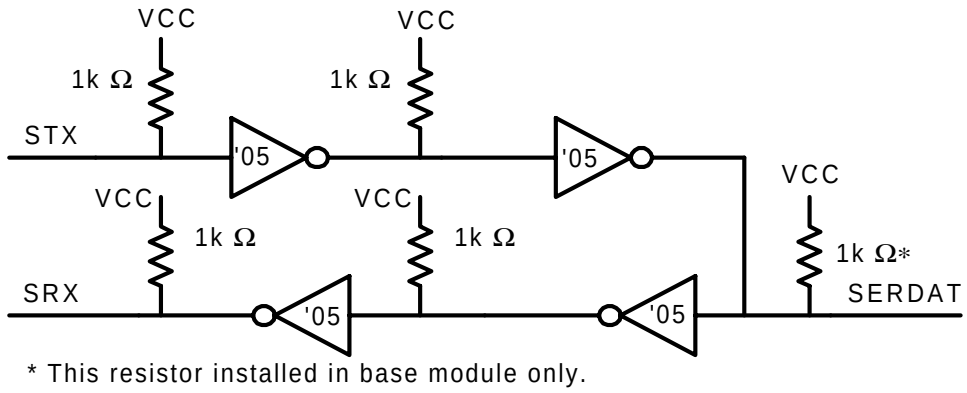
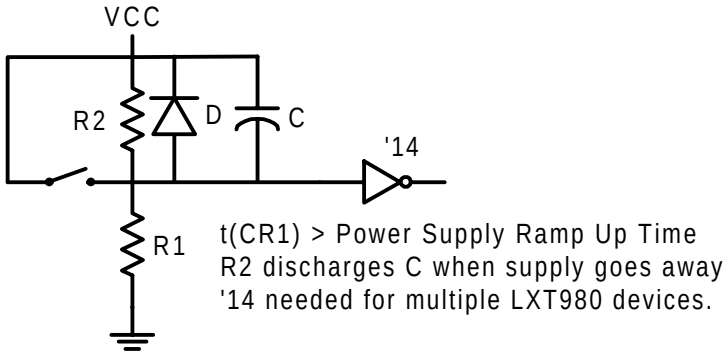


Figure 24: Typical Reset Circuit



TEST SPECIFICATIONS

NOTE

Tables 24 through 48 and Figures 25 through 40 represent the performance specifications of the LXT980/980A and are guaranteed by test except, where noted, by design. The minimum and maximum values listed in Tables 26 through 48 are guaranteed over the recommended operating conditions specified in Table 25.

Table 24: Absolute Maximum Ratings

Parameter		Symbol	Min	Max	Units
Supply voltage		VCC	-0.3	6	V
Operating temperature	Ambient	TOPA	-15	+80	ºC
	Case	TOPC	–	+130	ºC
Storage temperature		TST	-65	+150	ºC

CAUTION

Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 25: Operating Conditions

Parameter		Sym	Min	Typ[1]	Max	Units
Recommended supply voltage		VCC	4.75	5.0	5.25	V
		VCCV	4.75	5.0	5.25	V
		VCCR	4.75	5.0	5.25	V
		VCCT	4.75	5.0	5.25	V
Recommended operating temperature	Ambient	TOPA	0	–	70	°C
	Case	TOPC	0	–	115	°C
Power consumption	Auto-Negotiation	PC	–	–	3.5	W
	100BASE-TX, 4 ports active	PC	–	–	3.5	W
	10BASE-T, 4 ports active	PC	–	–	3.4	W
	100BASE-FX, 4 ports active	PC	–	–	3.0	W

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 26: Input Clock Requirements

Parameter[1]	Symbol	Min	Typ[2]	Max	Units	Test Conditions
Frequency	–	–	25	–	MHz	–
Frequency Tolerance	–	–	–	±100	PPM	–
Duty Cycle	–	40	–	60	%	–

1. These requirements apply to the external clock supplied to the LXT980, not to LXT980 test specifications.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 27: I/O Electrical Characteristics

Parameter	Sym	Min	Typ[1]	Max	Units	Test Conditions
Input Low voltage	V_{IL}	–	–	0.8	V	TTL inputs
		–	–	30	% V_{CC}	CMOS inputs [2]
		–	–	1.0		Schmitt triggers [3]
Input High voltage	V_{IH}	2.0	–	–	V	TTL inputs
		70	–	–	% V_{CC}	CMOS inputs [2]
		V_{CC} - 1.0	–	–	V	Schmitt triggers [3]
Hysteresis voltage	–	1.0	–	–	V	Schmitt triggers [3]
Output Low voltage	V_{OL}	–	–	0.4	V	I_{OL} = 1.6 mA
Output Low voltage (LED)	V_{OLL}	–	–	1.0	V	I_{OLL} = 10 mA
Output High voltage	V_{OH}	2.4	–	–	V	I_{OH} = 40 µA
Input Low current	I_{IL}	-100	–	–	µA	–
Input High current	I_{IH}	–	–	100	µA	–
Output rise / fall time	T_{RF}	–	3	10	ns	C_L = 15 pF

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Does not apply to IRB pins. Refer to Tables 28 and 29 for IRB I/O characteristics.
3. Applies to RESET and CLK25 pins only.

Table 28: 100 Mbps IRB Electrical Characteristics

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage		V_{OL}	–	.3	.7	V	R_L = 330 Ω
Output rise or fall time		T_{RF}	–	4	10	ns	C_L = 15 pF
Input High voltage		V_{IH}	V_{CC} - 2.0	–	–	V	CMOS inputs
			V_{CC} - 1.0	–	–	V	IR100CLK (Schmitt trigger)
Input Low voltage		V_{IL}	–	–	2.0	V	CMOS inputs
			–	–	1.0		IR100CLK (Schmitt trigger)
Hysteresis voltage		–	1.0	–	–	V	IR100CLK (Schmitt trigger)
$\overline{\text{IR100CFS}}$ current	single drive	–	–	8.0	–	mA	R_L = 240 Ω
	collision	–	–	16.0	–	mA	R_L = 240 Ω
$\overline{\text{IR100CFSBP}}$ current	single drive	–	–	22.0	–	mA	R_L = 91 Ω[2]
	collision	–	–	45.0	–	mA	R_L = 91 Ω[2]
$\overline{\text{IR100CFS/BP}}$ voltage	single drive	–	–	2.8	–	V	–
	collision	–	–	0.6	–	V	–

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. 91Ω resistors provide greater noise immunity. Systems using 91Ω resistors are backwards stackable with systems using 100Ω resistors.

Table 29: 10 Mbps IRB Electrical Characteristics

Parameter		Symbol	Min	Typ[1]	Max	Units	Test Conditions
Output Low voltage		VOL	0	.1	.4	V	RL = 330 Ω
Output rise or fall time		TRF	–	4	10	ns	CL = 15 pF
Input High voltage		VIH	VCC - 2.0	–	–	V	CMOS inputs
			VCC - 2.0	–	–	V	IR10CLK (Schmitt trigger)
Input Low voltage		VIL	–	–	2.0	V	CMOS inputs
			–	–	1.0	V	IR10CLK (Schmitt trigger)
Hysteresis voltage		–	0.5	–	–	V	IR10CLK (Schmitt trigger)
$\overline{\text{IR10CFS}}$ current	single drive	–	–	3.2	–	mA	RL = 680 Ω
	collision	–	–	6.6	–	mA	RL = 680 Ω
$\overline{\text{IR10CFSBP}}$ current	single drive	–	–	8.1	–	mA	RL = 330 Ω
	collision	–	–	17.0	–	mA	RL = 330 Ω
$\overline{\text{IR10CFS/BP}}$ voltage	single drive	–	1.9	2.8	3.2	V	–
	collision	–	.25	0.6	0.8	V	–

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.

Table 30: 100BASE-TX Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Peak differential output voltage (single ended)	VP	0.95	1.0	1.05	V	Note 2
Signal amplitude symmetry	–	98	–	102	%	Note 2
Signal rise/fall time	TRF	3.0	–	5.0	ns	Note 2
Rise/fall time symmetry	TRFS	–	–	0.5	ns	Note 2
Duty cycle distortion	–	–	–	+/- 0.5	ns	Offset from 8 ns pulse width at 50% of pulse peak,
Overshoot	VO	–	–	5	%	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Measured at line side of transformer, line replaced by 100Ω (±.1%) resistor.

Table 31: 100BASE-FX Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage (single ended)	VOP	0.6	–	1.0	V	–
Signal rise/fall time	TRF	–	–	1.6	ns	10 <-> 90%, 2.0 pF load
Jitter (measured differentially)	–	–	–	1.3	ns	–
Receiver						
Peak differential input voltage	VIP	0.55	–	1.5	V	–
Common mode input range	VCMIR	2.25	–	VCC - 0.5	V	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.

Table 32: 10BASE-T Transceiver Electrical Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
Transmitter						
Peak differential output voltage	VP	2.2	2.5	2.8	V	Measured at line side of transformer, line replaced by 100Ω (± .1%) resistor
Transmit timing jitter addition[2]	–	–	±6.4	±10	ns	0 line length for internal MAU
Transmit timing jitter added by the MAU and PLS sections[2, 3]	–	–	±3.5	±5.5	ns	After line model specified by IEEE 802.3 for 10BASE-T internal MAU
Receiver						
Receive input impedance	ZIN	–	3.4	–	kΩ	Between TPIP/TPIN
Differential Squelch Threshold	VDS	300	420	585	mV	5 MHz square wave input, 750 mVpp

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Parameter is guaranteed by design; not subject to production testing.
3. IEEE802.3 specifies maximum jitter additions at 1.5 ns for the AUI cable, 0.5 ns from the encoder, and 3.5 ns from the MAU.

Figure 25: 100 Mbps Port-to-Port Delay Timing

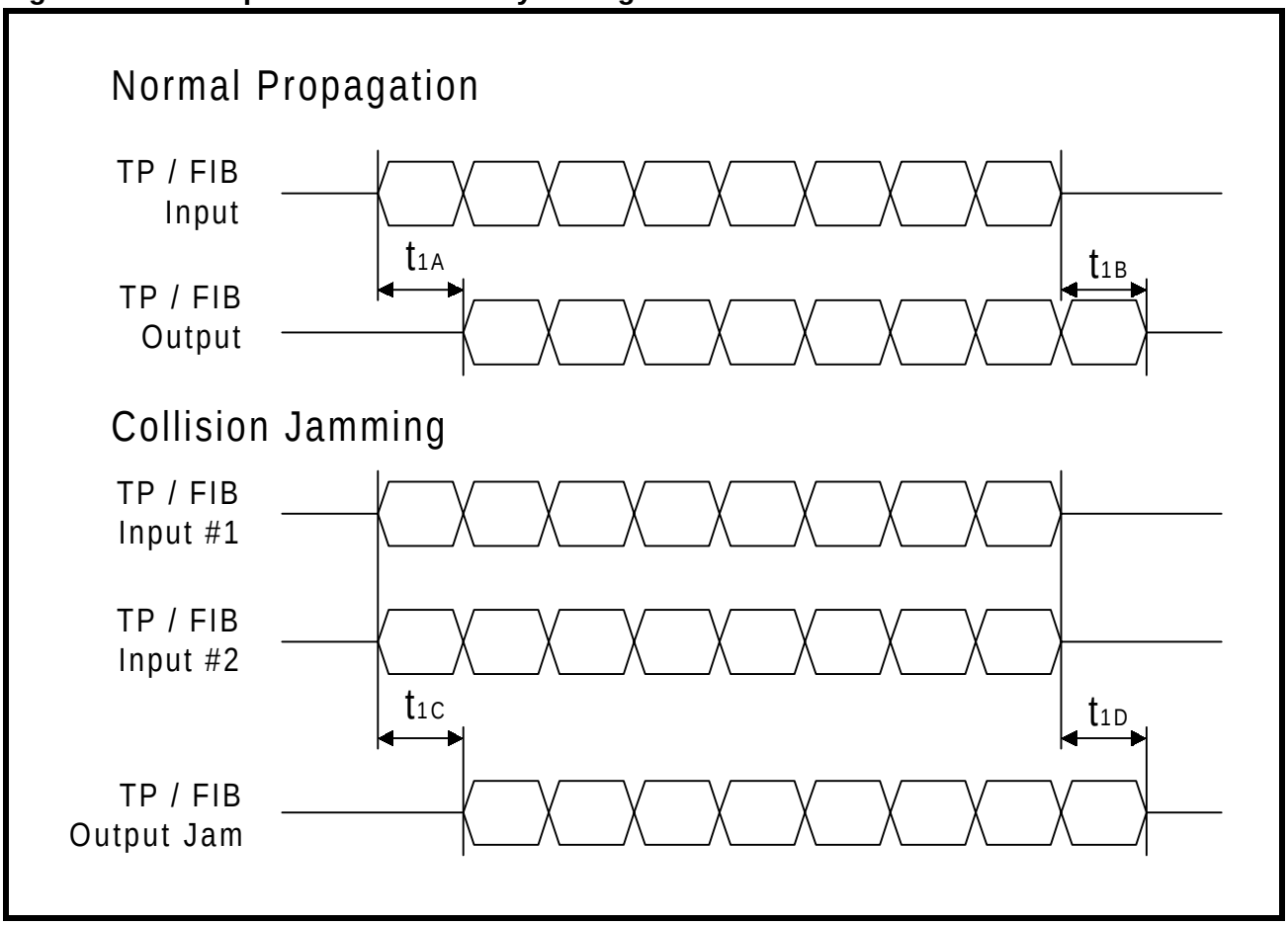


Table 33: 100 Mbps Port-to-Port Delay Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, start of transmission	t1A	–	–	46	BT	–
TPIP/N or FIBIP/N to TPOP/N or FIBOP/N, end of transmission	t1B	–	–	46	BT	–
TPIP/N or FIBIP/N collision to TPOP/N or FIBOP/N, start of jam	t1C	–	–	46	BT	–
TPIP/N or FIBIP/N idle to TPOP/N or FIBOP/N, end of jam	t1D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 26: 100BASE-TX Transmit Timing - PHY MODE MII

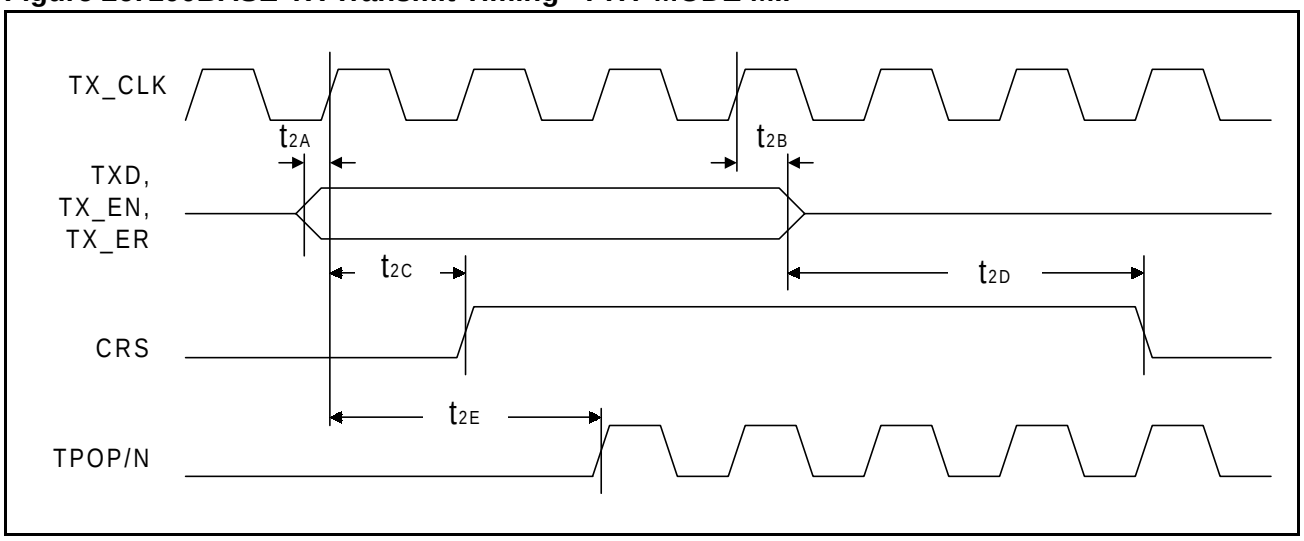


Table 34: 100BASE-TX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Condition
TXD, TX_EN, TX_ER Setup to TX_CLK High	t2A	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t2B	5	–	–	ns	–
TX_EN sampled to CRS asserted	t2C	0	–	4	BT	–
TX_EN sampled to CRS de-asserted	t2D	0	–	16	BT	–
TX_EN sampled to TPOP/N active (Tx latency)	t2E	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 27: 100BASE-TX Receive Timing - PHY Mode MII

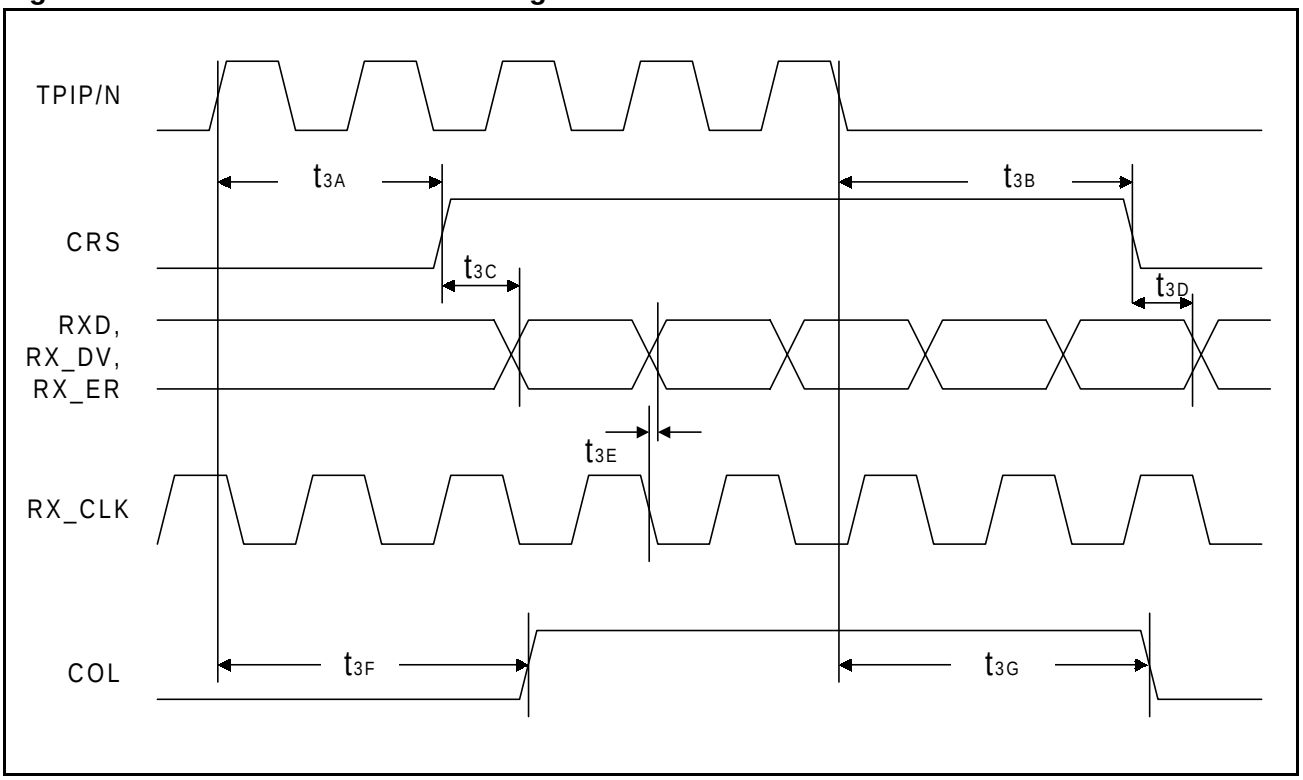


Table 35: 100BASE-TX Receive Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to CRS asserted	t3A	–	–	46	BT	–
TPIP/N quiet to CRS de-asserted	t3B	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t3C	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t3D	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t3E	–	–	10	ns	–
TPIP/N in to COL asserted	t3F	–	–	46	BT	–
TPIP/N quiet to COL de-asserted	t3G	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 28: 100BASE-TX Transmit Timing - MAC Mode MII

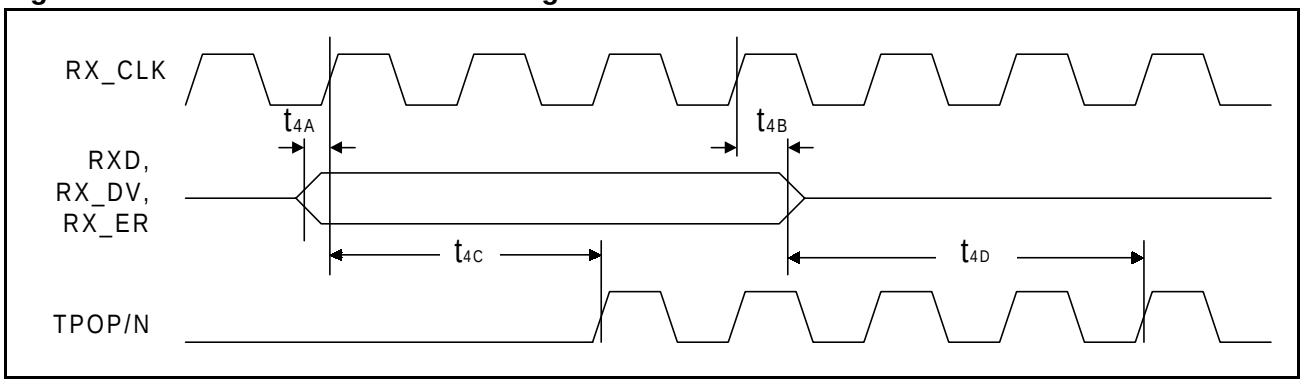


Table 36: 100BASE-TX Transmit Timing Parameters - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t4A	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t4B	5	–	–	ns	–
RXD sampled to TPO asserted	t4C	–	–	46	BT	–
RXD sampled to TPO de-asserted	t4D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 29: 100BASE-TX Receive Timing - MAC Mode MII

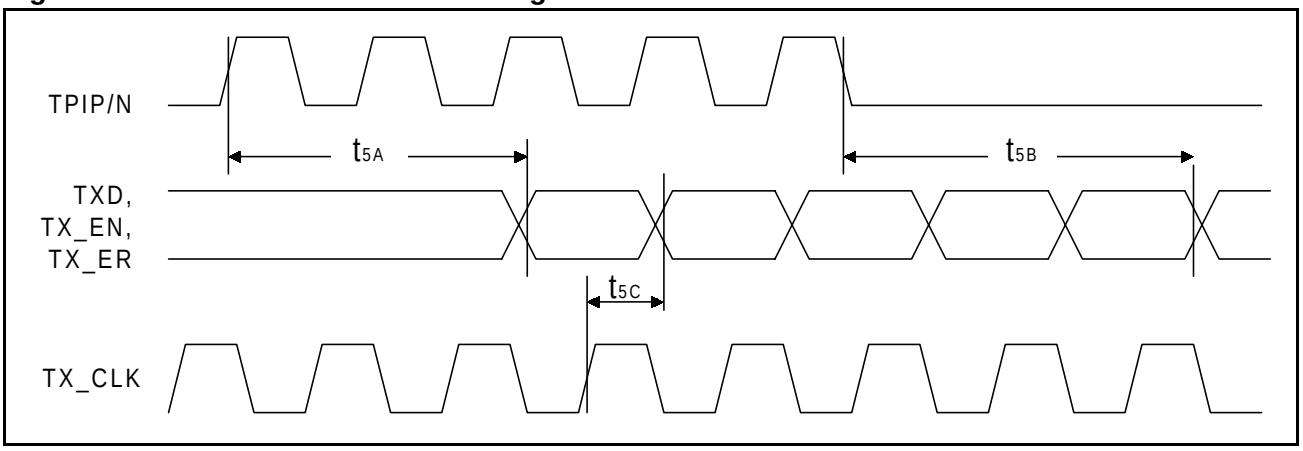


Table 37: 100BASE-TX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to TXD, TX_EN, TX_ER	t5A	–	–	46	BT	–
TPIP/N quiet to TXD de-asserted	t5B	13	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t5C	0	–	25	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 30: 100BASE-FX Transmit Timing - PHY Mode MII

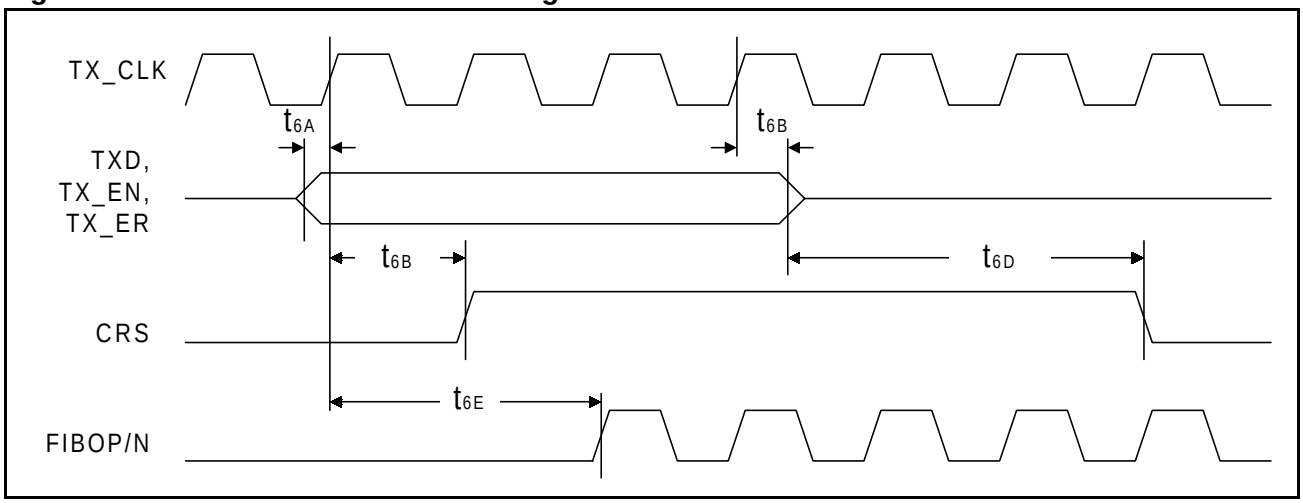


Table 38: 100BASE-FX Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t6A	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t6B	5	–	–	ns	–
TX_EN sampled to CRS asserted	t6C	0	–	4	BT	–
TX_EN sampled to CRS de-asserted	t6D	0	–	16	BT	–
TX_EN sampled to FIBOP/N out (Tx latency)	t6E	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 31: 100BASE-FX Receive Timing - PHY Mode MII

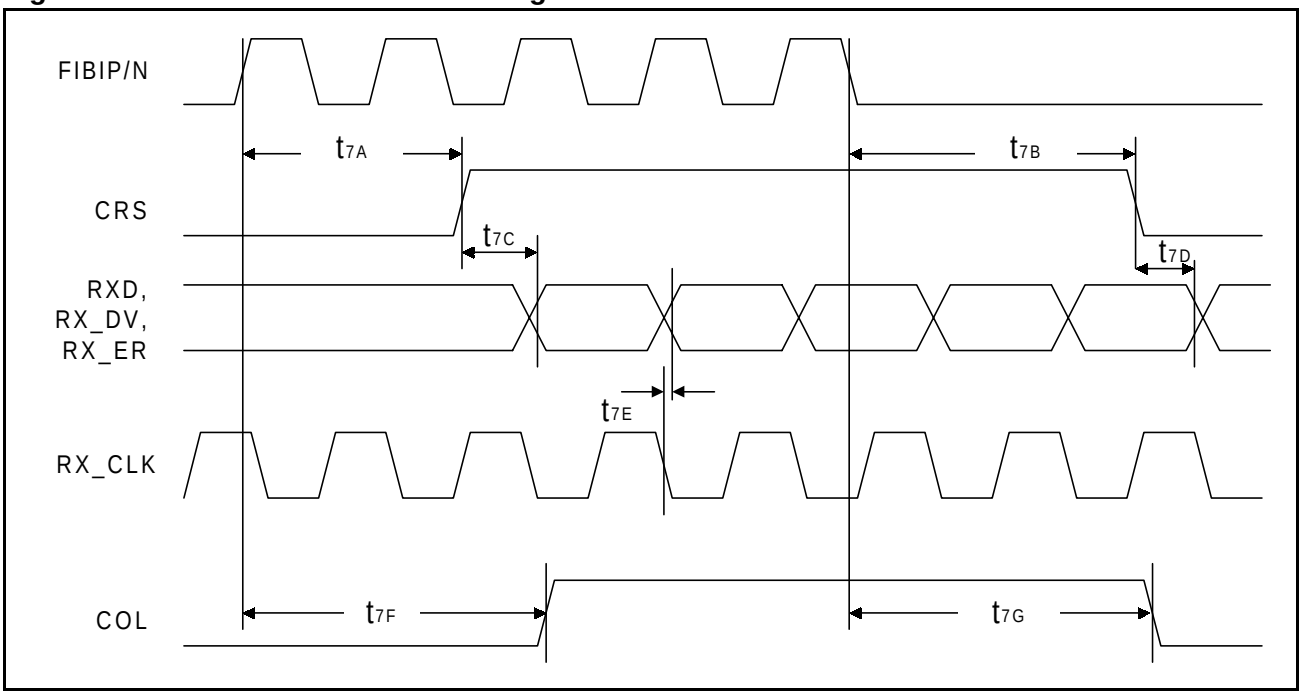


Table 39: 100BASE-FX Receive Timing - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
FIBIP/N in to CRS asserted	t7A	–	–	46	BT	–
FIBIP/N quiet to CRS de-asserted	t7B	–	–	46	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t7C	1	–	4	BT	–
CRS de-asserted to RXD, RX_DV, RX_ER de-asserted	t7D	–	–	3	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t7E	–	–	10	ns	–
FIBIP/N in to COL asserted	t7F	–	–	46	BT	–
FIBIP/N quiet to COL de-asserted	t7G	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 32: 100BASE-FX Transmit Timing - MAC Mode MII

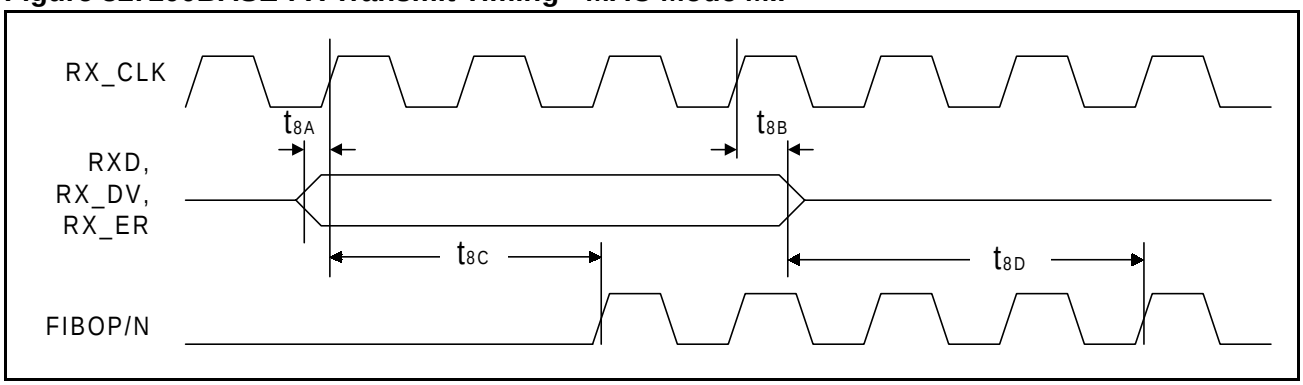


Table 40: 100BASE-FX Transmit Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
RXD, RX_DV, RX_ER Setup to RX_CLK High	t8A	10	–	–	ns	–
RXD, RX_DV, RX_ER Hold from RX_CLK High	t8B	5	–	–	ns	–
RXD sampled to FIBOP/N asserted	t8C	–	–	46	BT	–
RXD sampled to FIBOP/N de-asserted	t8D	–	–	46	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 33: 100BASE-FX Receive Timing - MAC Mode MII

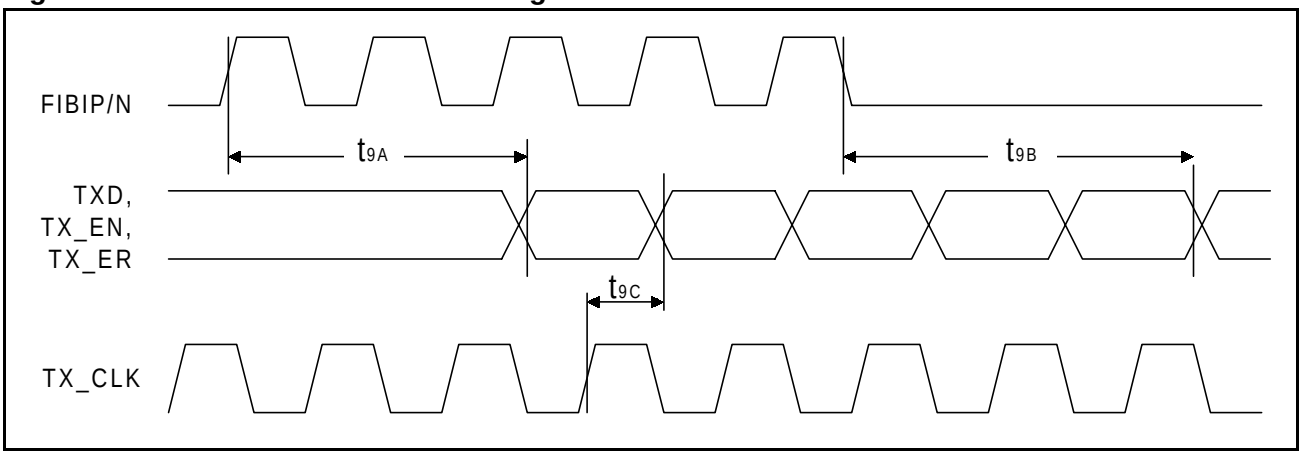


Table 41: 100BASE-FX Receive Timing - MAC Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
FIBIP/N in to TXD, TX_EN, TX_ER	t9A	–	–	46	BT	–
FIBIP/N quiet to TXD de-asserted	t9B	–	–	46	BT	–
TX_CLK rising edge to TXD, TX_EN, TX_ER valid	t9C	0	–	25	ns	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 34: 10BASE-T Transmit Timing - PHY Mode MII

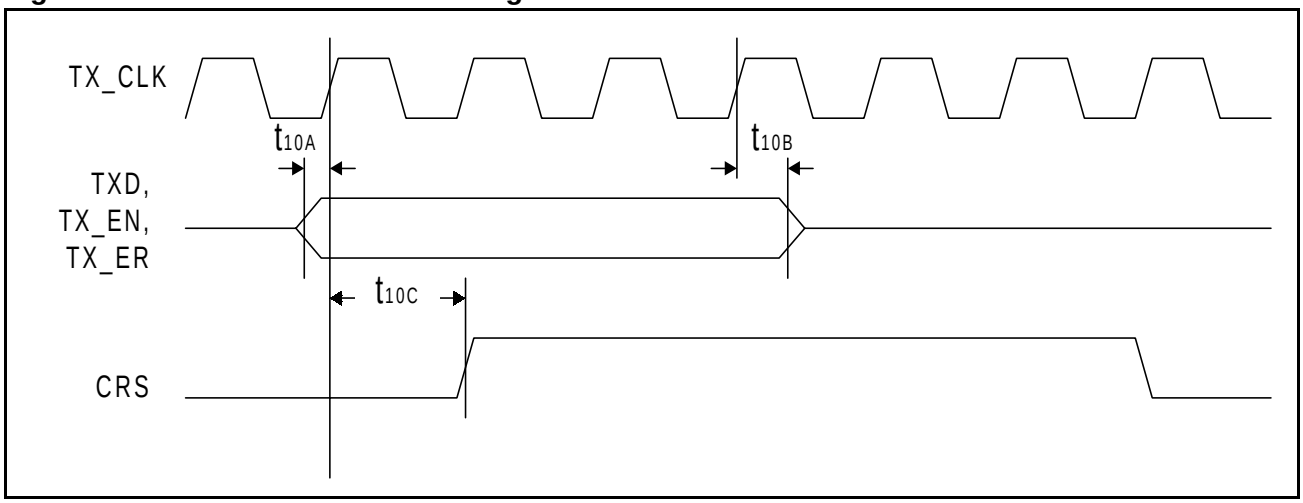


Table 42: 10BASE-T Transmit Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TXD, TX_EN, TX_ER Setup to TX_CLK High	t10A	10	–	–	ns	–
TXD, TX_EN, TX_ER Hold from TX_CLK High	t10B	5	–	–	ns	–
TX_EN sampled to CRS asserted	t10C	0	.9	2	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 10BASE-T = 10^{-7} s or 100 ns.

Figure 35: 10BASE-T Receive Timing - PHY Mode MII

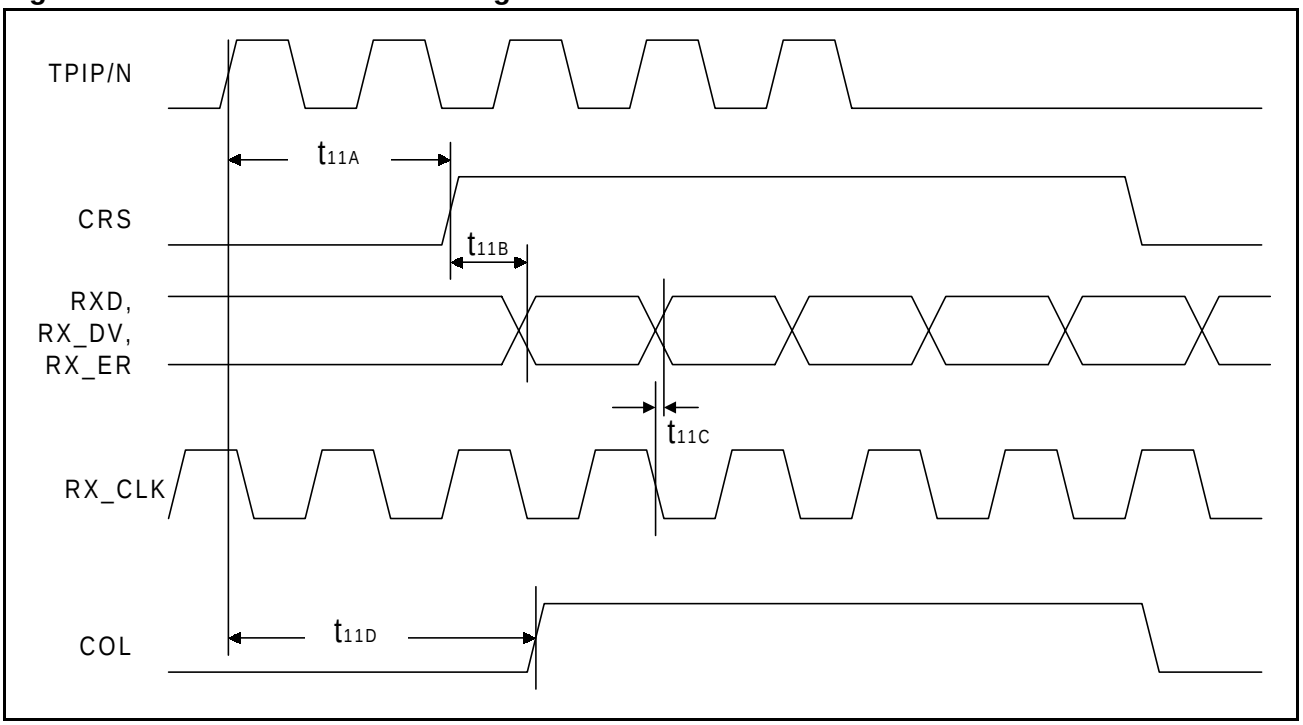


Table 43: 10BASE-T Receive Timing Parameters - PHY Mode MII

Parameter	Sym	Min	Typ[1]	Max	Units[2]	Test Conditions
TPIP/N in to CRS asserted	t11A	5	6.6	8	BT	–
CRS asserted to RXD, RX_DV, RX_ER	t11B	70	76	84	BT	–
RX_CLK falling edge to RXD, RX_DV, RX_ER valid	t11C	–	–	10	ns	–
TPIP/N in to COL asserted	t11D	6	7.4	9	BT	–

1. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 10BASE-T = 10^{-7}s or 100 ns.

Figure 36: 100 Mbps IRB Timing

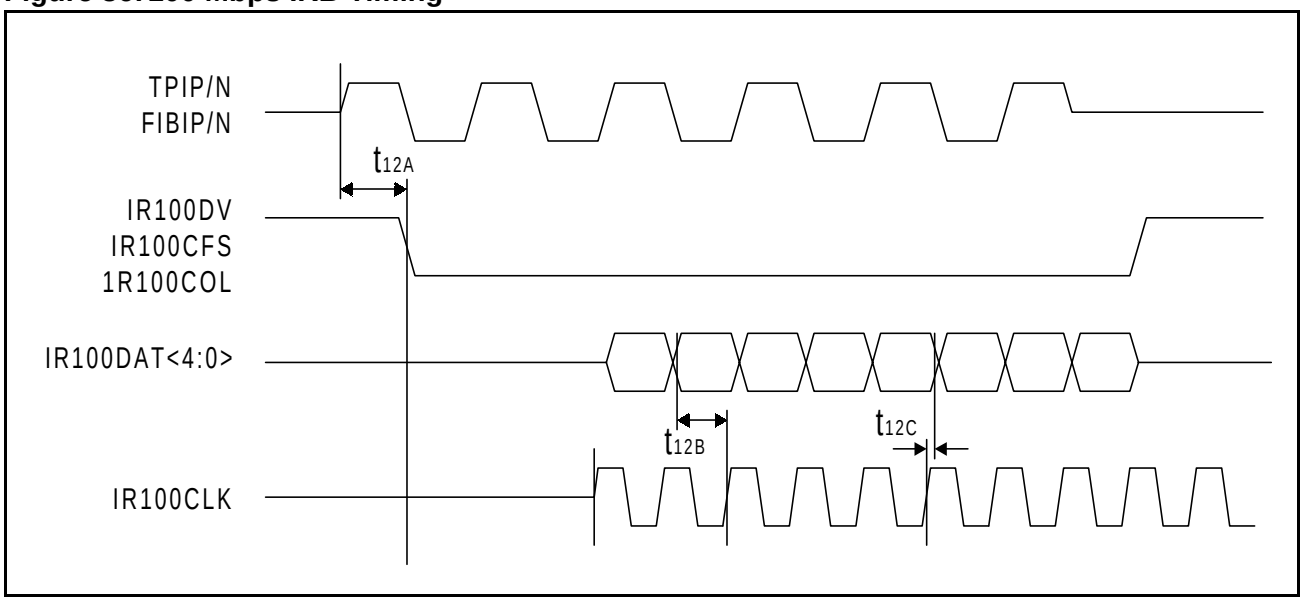


Table 44: 100 Mbps IRB Timing Parameters[1]

Parameter	Symbol	Min	Typ[2]	Max	Units[3]	Test Conditions
TPIP/N or FIBP/N to $\overline{\text{IR100DV}}$ Low	t12A	18	24	30	BT	–
IR100DAT to IR100CLK setup time.	t12B	–	10	–	ns	–
IR100DAT to IR100CLK hold time.	t12C	–	0	–	ns	–

1. This table contains propagation delays from the TP ports to the IRB for normal repeater operation. All values in this table are output timings.
2. Typical figures are at 25 C and are for design aid only; not guaranteed and not subject to production testing.
3. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 100BASE-T = 10^{-8} s or 10 ns.

Figure 37: 10 Mbps IRB Receive Timing

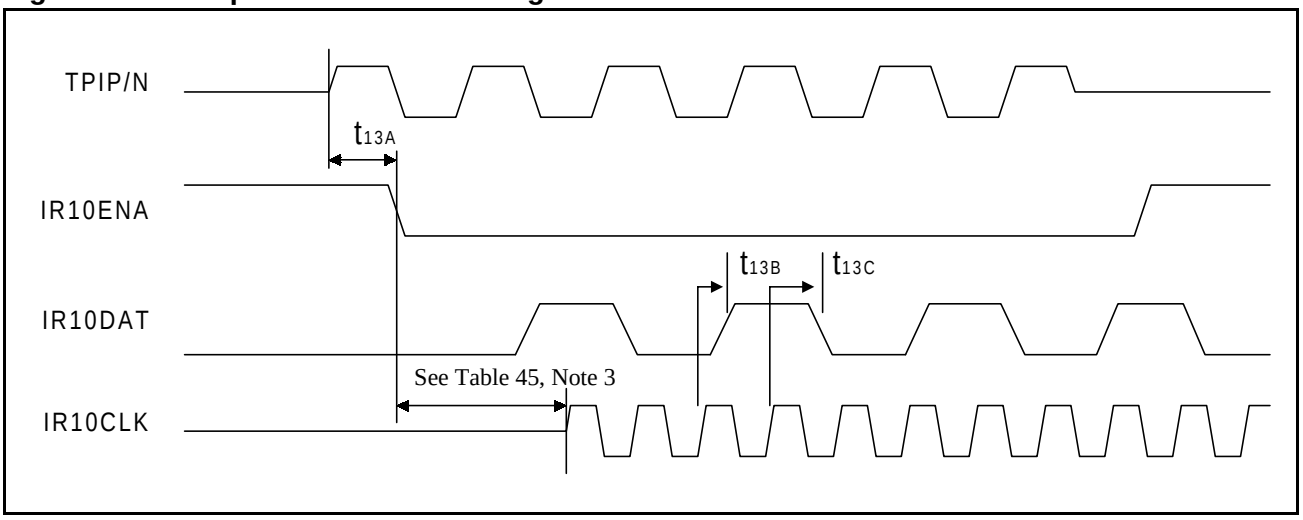


Table 45: 10 Mbps IRB Receive Timing Parameters[1]

Parameter	Symbol	Min	Typ[2]	Max	Units[4]	Test Conditions
TPIP/N to $\overline{\text{IR10ENA}}$ Low	t13A	3	5.1	7	BT	–
IR10CLK rising edge to IR10DAT rising edge.	t13B	25	-	55	ns	330 Ω pull-up, 150 pF load on IR10DAT. 1 kΩ pull-up, 150 pF load on IRCLK. All measurements at 2.5V.
IR10CLK rising edge to IR10DAT falling edge.	t13C	5	-	25	ns	

1. This table contains propagation delays from the TP ports to the IRB for normal repeater operation. All values in this table are output timings.
2. Typical values are at 25 °C and are for design aid only; not guaranteed and not subject to production testing.
3. There is a delay of approximately 13 to 16 bit times between the assertion of $\overline{\text{IR10ENA}}$ and the assertion of IR10CLK and IR10DAT. This delay does not affect repeater operation because downstream devices begin generating preamble as soon as $\overline{\text{IR10ENA}}$ is asserted.
4. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 10BASE-T = 10^{-7} s or 100 ns.

Figure 38: 10 Mbps IRB Transmit Timing

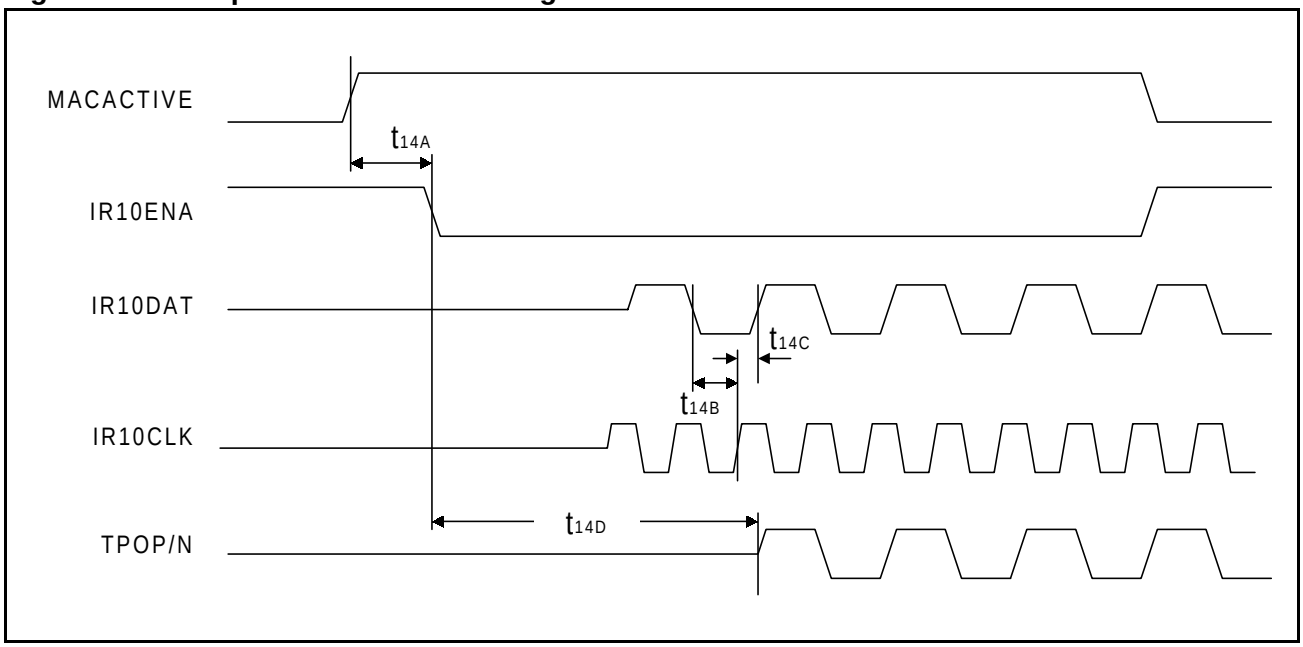


Table 46: 10 Mbps IRB Transmit Timing Parameters

Parameter	Symbol	Min	Typ[1]	Max	Units[2]	Test Conditions
MACACTIVE to $\overline{\text{IR10ENA}}$ assertion delay [3]	t14A	–	100	–	ns	MACACTIVE High to $\overline{\text{IR10ENA}}$ Low. [4]
IR10DAT (input) to IR10CLK setup time	t14B	–	20	–	ns	IR10DAT valid to IR10CLK rising edge.[4]
IR10CLK to IR10DAT (input) hold time	t14C	–	0	–	ns	IR10CLK rising edge to IR10DAT change.[4]
$\overline{\text{IR10ENA}}$ asserted to TPOP/N active	t14D	5	5.1	6	BT	–

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Bit Time (BT) is the duration of one bit as transferred to/from the MAC and is the reciprocal of bit rate. BT for 10BASE-T = 10^{-7} s or 100 ns.
3. External devices should allow at least one 10 MHz clock cycle (10 ns) between assertion of MACACTIVE and $\overline{\text{IR10ENA}}$.
4. Input.

Figure 39: Serial Management Interface Timing

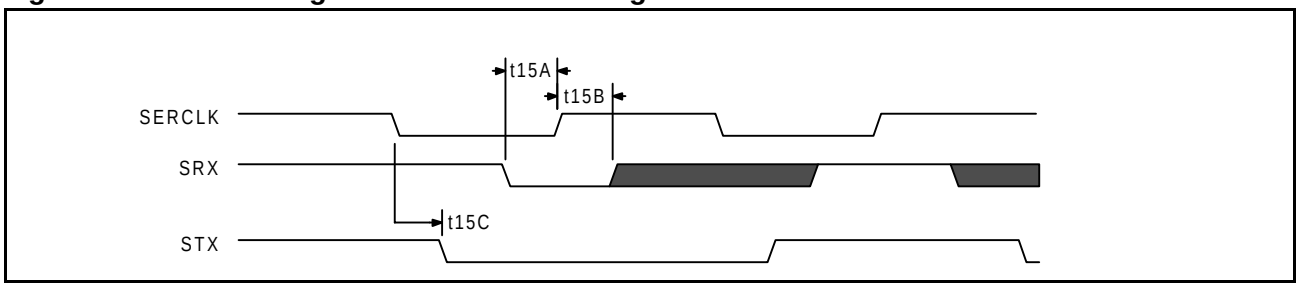


Table 47: Serial Interface Timing Characteristics [1]

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
SERCLK input frequency	–	–	–	2.0	MHz	Depending on RECONFIG, this is either an input or output.
SERCLK output frequency	–		625	–	kHz	
Data to clock setup time	t15A	0	–	–	ns	SRX valid to SERCLK rising edge. [2]
Clock to data hold time	t15B	200	–	–	ns	SERCLK rising edge to SRX change. [2]
Data propagation delay	t15C	–	–	200	ns	SERCLK falling edge to STX valid. [3]

1. Typical values are at 25° C and are for design aid only; they are not guaranteed and not subject to production testing.
2. Input.
3. Output.

Figure 40: PROM Interface Timing

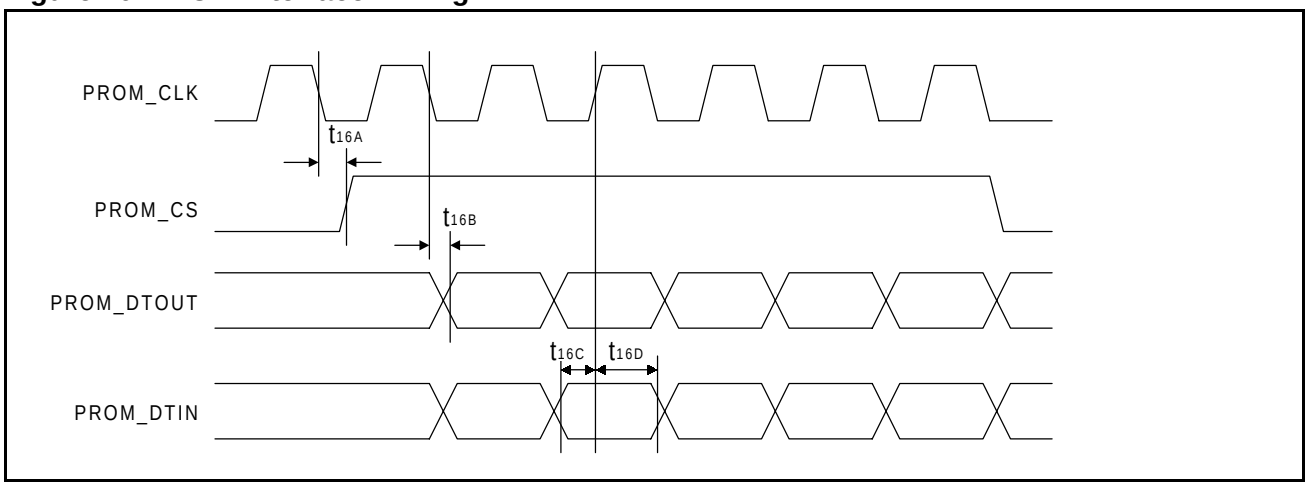


Table 48: PROM Interface Timing Characteristics

Parameter	Symbol	Min	Typ[1]	Max	Units	Test Conditions
PROM_CLK	–	–		1.0	MHz	PROM_CLK frequency.
CLK to PROM_CS delay	t16A	–		200	ns	CLK falling edge to PROM_CS.
CLK to PROM_DTOUT delay	t16B	–		20	ns	CLK falling edge to PROM_DTOUT.
PROM_DTIN to CLK setup time	t16C	20		–	ns	PROM_DTIN to CLK rising edge.
PROM_DTIN to CLK hold time	t16D	20		–	ns	PROM_DTIN to CLK rising edge.

REGISTER DEFINITIONS

The LXT980/980A register set is composed of multiple 32-bit registers of the types listed in Table 49. All register addresses are hexadecimal.

Table 49: Register Set

Base Address[1]	Register Type	Bit Assignments & Description
00X	Port 1 Counters (TP/FX)	Refer to Tables 50 and 51.
01X	Port 2 Counters (TP/FX)	
02X	Port 3 Counters (TP/FX)	
03X	Port 4 Counters (TP/FX)	
04X	Port 5 Counters (MII)	
05X	Additional Counters (100 only)	
05X, 06X	RMON Counters	Refer to Tables 50 and 52.
07X	Port Addresses	Refer to Tables 53 and 54.
08X	Authorized Addresses	Refer to Table 53.
08X, 09X	Global Addresses	Refer to Tables 53 and 55.
09X	Port Control & Status	Refer to Tables 56 through 63.
09X, 0AX, 0BX, 188, 189, 190, 191	General Setup/Status	Refer to Tables 64 through 82.

1. X = Offset address of register desired. Note that base register addresses for port counters are offset by 1 (00x refers to Port 1, 01X to Port 2, 02X to Port 3, 03X to Port 4 and 04X to Port 5).

Counter Registers

Table 50 shows bit assignments. When reading a 64-bit counter, read the lower address (lower 32 bits of counter) first, followed by the upper address. The first read causes all 64 bits to be simultaneously latched into an internal holding register. The second read is directed to this holding register. The statistics bit must be set off to write to the counters.

Table 50: Counter Register Bit Assignments

31	30	29	28	27	26	25: 7	6	5	4	3	2	1	0
D31	D30	D29	D28	D27	D26	D25:D7	D6	D5	D4	D3	D2	D1	D0

Port Counter Registers

The Port Counter descriptions in Table 51 are intended to be illustrative. For the exact definition of these counters, refer to the Repeater MIB, RFC 1516. All counters count packets, octets or events that were received at each port. In the descriptions, the length of a packet never includes preamble or framing bits (start of frame, end of frame, dribble bits, etc.), but an “event” does include these items.

Table 51: Port Counter Registers

Name	Offset Addr[1]	Description
Registers Used When Running at 10 or 100 Mbps		
rptrMonitorPortReadableFrames	0X0	Counts valid-length (64 to 1518 bytes), valid-CRC, collision-free packets. Depending on the state of the Count-Mode bit (6) in the Repeater Configuration Register, this counter will count either all packets (CountMode=0) or only Unicast Packets (CountMode=1).
rptrMonitorPortReadableOctets (Lower/Upper)	0X1, 0X2	Counts the number of octets in all valid-length (64 to 1518 bytes), valid-CRC, collision-free packets, not including preamble and framing bits. This register is not affected by the CountMode bit.
rptrMonitorPortFrameCheckSequence	0X3	Counts valid length, collision-free packets that had FCS errors, but were correctly framed (had an integral number of octets).
rptrMonitorPortAlignmentErrors	0X4	Counts valid length, collision-free packets that had FCS errors and were incorrectly framed (had a non-integral number of octets).
rptrMonitorPortFramesTooLong	0X5	Counts packets that had a length greater than 1518 octets.
rptrMonitorPortShortEvents	0X6	**10M:** Counts events ≤80 bit times.
		100M: Counts events ≤ 88 bit times.
rptrMonitorPortRunts	0X7	**10M:** Counts events > 80 and ≤ 504 bit times.
		100M: Counts events ≥ 92 and ≤ 504 bit times.[2]
rptrMonitorPortCollisions	0X8	Counts the number of collisions that occurred, not including late collisions.
rptrMonitorPortLateEvents	0X9	Counts the number of times collision was detected more than 512 bit times after the start of carrier.
rptrMonitorPortVeryLongEvents	0XA	Counts the number of times any activity continued for more than 4 to 7.5 ms.
rptrMonitorPortDataRateMismatches	0XB	Counts the number of times the incoming data rate mismatched the local clock source enough to cause a FIFO underflow or overflow.
rptrMonitorPortAutoPartitions	0XC	Counts the number of times this port has been partitioned by the Auto-partition algorithm.
rptrTrackSourceAddrChanges	0XD	Counts the number of times the source address has changed. Minimum roll-over time of 81 hours.

1. Replace “X” in address with specific port to be addressed (offsets 0 through 4 correspond to Ports 1 through 5).
2. For 100M: the “Short Events” register counts events ≤ 88 bit times; the “Port Runts” register counts events ≥ 92. A 4-bit-time differential exists because 100M operates with nibble boundaries, so data packets ≤ 4 bits are counted as 4.

Table 51: Port Counter Registers – continued

Name	Offset Addr[1]	Description
rptrMonitorPortBroadcastPkts	0XE	Counts the number of good broadcast packets received by this port. Counter is not cleared by ZeroCount bit.
rptrMonitorPortMulticastPkts	0XF	Counts the number of good multicast packets received by this port. Counter is not cleared by ZeroCount bit.
Registers used only when running at 100 Mbps		
rptrMonitorPortIsolates - Port 1	050	Counts the number of times a port auto isolates. NOTE: When these counters increment, none of the other port counters will increment since the frame never had a valid start.
rptrMonitorPortIsolates - Port 2	051	
rptrMonitorPortIsolates - Port 3	052	
rptrMonitorPortIsolates - Port 4	053	
rptrMonitorPortIsolates - Port 5	054	
rptrMonitorSymbolErrorDuringPacket - Port 1	055	Counts the number of time a packet contained symbol errors. Only one symbol error is counted per packet.
rptrMonitorSymbolErrorDuringPacket - Port 2	056	
rptrMonitorSymbolErrorDuringPacket - Port 3	057	
rptrMonitorSymbolErrorDuringPacket - Port 4	058	

1. Replace “X” in address with specific port to be addressed (offsets 0 through 4 correspond to Ports 1 through 5).
2. For 100M: the “Short Events” register counts events ≤ 88 bit times; the “Port Runts” register counts events ≥ 92. A 4-bit-time differential exists because 100M operates with nibble boundaries, so data packets ≤ 4 bits are counted as 4.

RMON Counter Registers

The interface counter descriptions in Table 52 are intended to be illustrative. For the exact definition of these counters, refer to the RMON MIB, RFC 1757. All counters count events, octets or packets that were received from the interface. Packet length never includes preamble or framing bits (start of frame, end of frame, dribble bits, etc.).

Table 52: RMON Counter Registers

Name	Type	Addr	Description
etherStatsOctets	R/W	05C, 05D	Number of data octets including those in bad packets and octets in FCS fields, but does not include preamble or other framing bits.
etherStatsPkts	R/W	05E	Number of packets received (from network), including errored packets.
etherStatsBroadcastPkts	R/W	05F	Number of good broadcast packets received. Counter is not cleared by ZeroCount bit.
etherStatsMulticastPkts	R/W	060	Number of good multicast packets received.
etherStatsCRCAlignErrors	R/W	061	Number of valid-length packets (64 to 1518 bytes inclusive) that had a bad Frame Check Sequence (FCS).
etherStatsUndersizePkts	R/W	062	Number of well-formed packets that were smaller than 64 octets.
etherStatsOversizePkts	R/W	063	**LXT980:** Number of well-formed packets that were longer than 1518 octets.
			LXT980A: Number of well-formed packets that were longer than 1518 octets and smaller than 2044.
etherStatsFragments	R/W	064	Number of ill-formed packets less than 64 octets. Note: Any event without a start-of-frame delimiter (0-octet packet) will be counted as a fragment, no matter how long it is.
etherStatsJabbers	R/W	065	**LXT980:** Number of ill-formed packets longer than 1518 octets. An ill-formed packet is one with an FCS error.
			LXT980A: Number of ill-formed packets longer than 1518 octets, and number of packets (good and bad) greater than/equal to 2044. An ill-formed packet is one with an FCS error.
etherStatsCollisions/ rptr Monitor Transmit Collisions	R/W	066	The best estimate of the total number of collisions on this interface.
etherStatsPkts64Octets	R/W	067	No. of packets (good and bad) that were 64 octets long.
etherStatsPkts65to127Octets	R/W	068	No. of packets (good and bad) between 65 and 127 octets long.
etherStatsPkts128to255Octets	R/W	069	No. of packets (good and bad) between 128 and 255 octets long.
etherStatsPkts256to511Octets	R/W	06A	No. of packets (good and bad) between 256 and 511 octets long.
etherStatsPkts512to1023Octets	R/W	06B	No. of packets (good and bad) between 512 and 1023 octets long.
etherStatsPkts1024to1518Octets	R/W	06C	No. of packets (good and bad) between 1024 and 1518 octets long.
Not Used	R/W	06D	
rptrMonitorTotalOctets (Lower/Upper)	R/W	06E, 06F	Total number of octets contained in valid frames received on this segment. Counter is not cleared by ZeroCount bit.

Ethernet Address Registers

All Ethernet address registers consist of two 32-bit registers that together contain a 48-bit Ethernet address. Refer to Table 53 for register bit assignments.

Table 53: Ethernet Address Register Bit Assignments

Upper Address	Bits 15:0 contain bits 47:32 of the Ethernet Address.
Lower Address	Bits 31:0 contain bits 31:0 of the Ethernet Address.

Port Address Tracking Registers

The port address tracking register set is described in Table 54. These registers continuously monitor the source addresses of packets emanating from the corresponding ports. Refer to Table 53 for bit assignments.

Table 54: Port Address Tracking Registers

Name	Size, bits	Addr	Description
rptrAddrTrackNewLastSrcAddress Port 1	48	070, 071	Stores the value of the last Source Address received. Can also act as NewLastSourceAddress via SW. These addresses power up unknown, but can be zeroed by software. Example Address: 00-20-7B-03-02-01 First Read: $_{msb}037B2000_{lsb}$. Second Read: $_{msb}$ XXXX0102$_{lsb}$ All addresses must read in order. Only the first read updates the holding register. X's are currently defined as zeros.
rptrAddrTrackNewLastSrcAddress Port 2	48	072, 073	
rptrAddrTrackNewLastSrcAddress Port 3	48	074, 075	
rptrAddrTrackNewLastSrcAddress Port 4	48	076, 077	
rptrAddrTrackNewLastSrcAddress Port 5 (MII)	48	078, 079	

1. All port address tracking registers are Read/Write.

Search Address Registers

The Search Address Register set is described in Table 55.

Table 55: Search Address Registers

Name	Type	Addr	Size (bits)	Description
Search Address Register Refer to Table 53 for bit assignments.	R/W	08A, 08B	48	On-board address search register. Should the user wish to find out if a particular source address has been seen on any of the ports, on any of the segments, this register would be used. Each port within an LXT980 chip will be checked for traffic originating from the source address matching this register. If a match is found, the port number where the traffic originated will be saved thus allowing software to determine where the address is located. The register that contains the port from the Search Address Match Function is the Search Address Match Register. (default = Xs)
Search Port Match Register Refer to Table 56 for bit assignments.	R	090	5	This register holds the port number of the host which uses the address specified in the Search Address Register. When the Auto-Clear bit (bit 11) in the Repeater Configuration Register is set to a ‘0’, this register is cleared upon reading. If the Auto-Clear bit is set to a ‘1’, this register’s bit(s) are cleared by writing a ‘1’ to the appropriate bit(s). (default = 0s)

Control and Status Registers

The Control and Status Register set includes general port control and status registers that conform to the bit assignments shown in Tables 56, 58, and 60. Additional control and status registers with alternate bit assignments are shown in Tables 61 through 68.

Port Link Control Register

The Port Link Control Register is described in Table 57. Refer to Table 56 for Port Link Control Register bit assignments.

Table 56: Port Link Control and Status Register Bit Assignments

31:4	3	2	1	0
Rsvd	Port 4	Port 3	Port 2	Port 1

Table 57: Port Link Control Register

Name	Type	Addr	Description
Port Link Control	R/W	091	This register controls the link function of the 4 twisted-pair ports of the LXT980. When disabled, a port will no longer be disconnected due to link fail. When enabled, the port will only remain connected to the network so long as link pulses are being received: 0 = disable, 1 = enable (default).

General Port Control Registers

The General Port Control Register set is described in Table 59. Refer to Table 58 for the General Port Control Registers bit assignments.

Table 58: General Port Control and Status Register Bit Assignments

31:5	4	3	2	1	0
Rsvd	Port 5 (MII)	Port 4	Port 3	Port 2	Port 1

Table 59: General Port Control Registers

<table>
<tr><th>Name</th><th>Type</th><th>Addr</th><th>Description</th></tr>
<tr><td rowspan="11">Port Alternate Partition Algorithm Control</td><td rowspan="11">R/W</td><td rowspan="11">094</td><td colspan="3">LXT980</td></tr>
<tr><td colspan="3">Provides per-port selection of partition algorithms.
0 = normal (default)
1 = alternate</td></tr>
<tr><td><u>Speed</u></td><td><u>Normal</u></td><td><u>Alternate</u></td></tr>
<tr><td>10M</td><td>Un-partition a port when data can be either received or transmitted from the port for 450-560 bit times without a collision on that port.</td><td>Un-partition a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.</td></tr>
<tr><td>100M</td><td>Un-partition a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.</td><td>Un-partition a port when data can be either received or transmitted from the port for 450-560 bit times without a collision on that port.</td></tr>
<tr><td colspan="3">LXT980A</td></tr>
<tr><td colspan="3">Provides per-port selection of partition algorithms.
0 = normal
1 = alternate (default)</td></tr>
<tr><td><u>Speed</u></td><td><u>Normal</u></td><td><u>Alternate</u></td></tr>
<tr><td>10M</td><td colspan="2">Un-partition a port when data can be either received or transmitted from the port for 450-560 bit times without a collision on that port.</td></tr>
<tr><td>100M</td><td>Un-partition a port only when data can be transmitted to the port for 450-560 bit times without a collision on that port.</td><td>Un-partition a port when data can be either received or transmitted from the port for 450-560 bit times without a collision on that port.</td></tr>
<tr><td>Port Enable</td><td>R/W</td><td>095</td><td colspan="3">This register controls whether a port is enabled/disabled. If the $\overline{\text{MGR\_PRES}}$ signal is Low on power up, then all ports will be disabled until such time that management software re-enables them. Otherwise the ports will power on enabled.
0 = disable, 1 = enable (default = 1).</td></tr>
</table>

Port Learn and Speed Control Registers

The port learn and speed control register set is described in Table 61. Refer to Table 61 for the bit assignments of these registers.

Table 60: Port Learn and Speed Control Registers

31:10	9	8	7	6	5	4	3	2	1	0
Rsvd	Port 5 (MII)		Port 4		Port 3		Port 2		Port 1	

Table 61: Port Learn and Speed Control Registers

Name	Type	Addr	Description		
Port Authorized Learn Enable Control	R/W	096	This register sets the level of learning each port uses. The Learn Settings are as follows:		
			Bit 1	**Bit 0**	**Function**
			0	0	Learn new source addresses.
			0	1	Next Lock. Learn only the first source address encountered. After a port learns its first address, it changes the Authorized Learn bits (for that port) to a “10” to lock down the address.
			1	0	Lock. Hardware locked-down the address. Only software can write to this address.
			1	1	Reserved.
Port Speed Control	R/W	097	This register overrides the hardware settings. Enabling auto-negotiation via software requires writing to both the Port Speed Control Register and the Auto-Negotiate Configuration Register (see Table 82 on page 89). Forcing a port’s speed overrides and disables auto-negotiation. The MII (expansion) port is not software-configurable. Default is set by pins SPD0 and SPD1. Settings are as follows:		
			SPD1	**SPD0**	**Function**
			0	0	If auto-negotiate is enabled, advertise all abilities. Otherwise port is disabled.
			0	1	Force 10 Mbps TP
			1	0	Force 100 Mbps Fiber (Does not apply to MII)
			1	1	Force 100 Mbps TP

Port Status Registers

The port status register set is described in Table 63. Bit assignments are shown in Table 62.

Table 62: Port Status Register Bit Assignments

31:4	4 [1]	3	2	1	0
Rsvd	Port 5 (MII)	Port 4	Port 3	Port 2	Port 1

1. Bit 4 used only in the port partition and port speed status registers.

Table 63: Port Status Registers

Name	Type[1]	Addr	Description
Port Link Status	R	098	A read of this register will reflect the current link status of the 4 twisted-pair ports within a LXT980 chip. A ‘1’ indicates that the port is currently in the LINK_GOOD state. (default = 0s)
Port Polarity Status	R	099	A read of this register will reflect the current polarity status of the 4 twisted-pair ports within a LXT980 chip. A ‘1’ indicates that the polarity has been crossed for a given port. (default = 0s)
Port Partition Status	R	09A	A read of this register will reflect the current partition status of all 5 ports within a LXT980 chip. A ‘1’ indicates that the port has been partitioned out of the repeater. A ‘0’ is read if the port is connected. (default = 0s)
Port Speed Status	R	09C	Indicates the current status of each port. 0 = port is connected at 10 Mbps 1 = port is connected at 100 Mbps
Port Isolation Status (Fast Ethernet Only)	R	09D	Indicates the current isolation status of each port operating in Fast Ethernet. Fast Ethernet Port Isolation (Clause 27.3.2 of 802.3u)

1. R = Read Only

Interrupt Status/Mask Registers

The interrupt status and mask registers are described in Tables 65 and 66. Refer to Table 64 for bit assignments.

Table 64: Interrupt Status/Mask Register Bit Assignments

31:8	7	6	5	4	3	2	1	0
Reserved	Far-End Fault	Reserved	Jabber	Isolate	Partition	FCC	Source Address Change	Speed Change Detected

Table 65: Interrupt Status/Mask Register

Name	Type	Addr	Description
Interrupt Status Register	R(/W)[1]	0AE	This register captures status bits within the LXT980 and holds them. Refer to Table 66 for bit descriptions.
Interrupt Mask Register	R/W	0AF	This register allows masking of individual interrupts. 0 = do not mask (default) 1 = mask

1. R(/W) When the register clear bit (bit11) in the repeater configuration register is set to a '0', this register is cleared upon reading. If the register clear bit is set to a '1', these register bit(s) are cleared by writing a '1' to the appropriate bit(s).

Table 66: Interrupt Status Register Bit Definitions

Bit	Name	Type[1]	Description	Default
31:8	Reserved	R/W	Reserved - Write as 0s; ignore on read.	N/A
7	Far End Fault	R/W	A '1' indicates that one of four conditions has occurred: 1. A port in fiber mode received the remote fault code from its link partner. 2. A port in auto-negotiation received 3 FLPs in a row with the remote fault bit set. 3. A port is in fiber mode with remote fault reporting enabled, and either the receive PLL is unlocked or the signal detect input has been lost. 4. A port in auto-negotiation is transmitting FLPs with the remote fault bit set. In conditions 1 and 2 the link partner has detected the remote fault condition and is sending it to the LXT980. In conditions 3 and 4 the LXT980 has detected the remote fault condition and is sending it to the link partner.	0
6	Reserved	R/W	Reserved - Write as 0s; ignore on read.	0

1. R = Read only; R/W = Read/Write.

Table 66: Interrupt Status Register Bit Definitions – continued

Bit	Name	Type[1]	Description	Default
5	Jabber	R	A ‘1’ indicates that a port is in jabber state. During 100 Mbps operation, jabber occurs when any receiver remains active for more than 57,500 bit times. The LXT980 exits this state when all receivers return to the idle condition. During 10 Mbps operation, jabber occurs when any port remains actively transmitting for longer than 40,000 to 75,000 bit times. The LXT980 will assert a minimum-IFG idle period when a port is jabbering.	0
4	Isolate	R/W	A ‘1’ indicates that a port has been isolated (100 Mbps only). The LXT980 isolates any port that transmit more than two successive false carrier events. A false carrier event is defined as a packet that does not start with a /J/K symbol pair.	0
3	Partition	R/W	A ‘1’ indicates that a port has been partitioned. In 100 Mbps operation, the LXT980 partitions any port that participates in excess of 60 consecutive collisions. In 10 Mbps operation, the LXT980 partitions any port that participates in excess of 32 consecutive collisions. Once partitioned, the LXT980 will continue monitoring and transmitting to the port, but will not repeat data received from the port until it properly un-partitions.	0
2	FCC	R/W	A ‘1’ indicates that a port has received too many false carrier events	0
1	SA Change	R/W	A ‘1’ indicates that a port address changed from that stored in the last-SourceAddress register.	0
0	Speed Change	R/W	A ‘1’ indicates that a port speed change was detected.	0

1. R = Read only; R/W = Read/Write.

MII Status Register

The MII Status register is described in Table 68. Refer to Table 67 for bit assignments. This is a 32-bit register.

Table 67: MII Status Register Bit Assignment

31:2	1	0
Reserved	Select 10 Mbps or 100 Mbps 0 = 10 Mbps 1 = 100 Mbps	Select connecting device type 0 = MAC Mode (connected to a PHY) (Available at 100 Mbps only) 1 = PHY Mode (connected to a MAC) (Available at either 10 or 100 Mbps)

Table 68: MII Status Register

Name	Type	Addr	Description
MII Register	R	0B4	Used to give the status of the MII port. Default is set by pins.

Configuration Registers

The Configuration Register set is described in Table 69. Bit assignments for the configuration registers are shown in Tables 70 through 77.

Table 69: Configuration Registers

Name	Type[1]	Addr	Description
Repeater Configuration Register	R/W	0AB	Refer to Table 70 for bit assignments.
Repeater Serial Configuration Register	R	0AC	This 8 bit register holds user-defined data. These bits may be used to indicate the type of board configuration, port count or other vendor-related data. Default is set by pins.
Device/Revision ID register	R	0AD	This register follows the IEEE 1149.1 specification. Refer to Table 72 for bit assignments. The upper 4 bits identify the device revision level. The next 16 bits store the Part ID Number, which in this case is hexadecimal '3D4'. The next 11 bits contain a JEDEC Manufacturer ID, which for Level One is hexadecimal 'FE'. The lowest bit (0) is set only for the first device in a chain.
Reserved	R	0B0	Ignore on read.
Global LED Control Register	R/W	0B1	Refer to Table 73 for bit assignments. This register reflects the LED Mode set by pins 207 and 208, and provides software control for the global Fault LED.

LED Mode, Bit Encoding (read only from pins):

Bit 5	Bit 4	Mode Selected
0	0	Mode 1
0	1	Mode 2
1	0	Mode 3
1	1	Reserved

Global Fault LED, Bit Encoding:

Bits 3 : 2	Modes 1 & 3	Mode 2
0 0	LED off	LED off
0 1 [2]	Hardware control	Hardware control
1 0	Reserved	LED slow blink
1 1 [3]	LED off	LED on steady

1. R = Read only; W = Write only; R/W = Read /Write.
2. Default value if manager is not present.
3. Default value if manager is present.

Table 69: Configuration Registers – continued

Name	Type[1]	Addr	Description
Port LED Control Register	R/W	0B2	This register provides a measure of software control over the port LEDs. Refer to Table 74 for bit assignments. During reset, the state of this register is all 1s. If a manager is present, this register remains in the all 1s state after reset. Otherwise, the bits default to hardware control. Encoding is as follows:
			Bits 1 : 0 / **Modes 1 & 3** / **Mode 2**
			0 0 / LED off / LED off
			0 1 / Reserved / LED fast blink
			1 0 [2] / Hardware Control / Hardware Control
			1 1 [3] / LED off / LED on steady
LED Timer Control Register	R/W	0B3	Refer to Table 75 for bit assignments. Bits 8-15 of this register set the fast blink frequency of the LEDs. Bits 0-7 set the slow blink frequency. The same formula is used in each case, with a maximum of 128 Hz and a minimum of 0.5 Hz. Example: fast blink = x32 (0.4 sec) slow blink = xCC (1.6 sec)
Repeater Reset Register	W	0B5	Writing any data value to this register with the Least Significant Bit (LSB) = 1 causes the repeater functional logic to reset. (All bits other than LSB do not matter.) The counters and configuration information will be held static and will not be reset. (default = 0s)
Software Reset Register	W	0B6	Writing any data value to this register with the Least Significant Bit (LSB) = 1 is identical to a hardware reset. (All bits other than LSB do not matter.) Everything is reset except the Source Address RAM. (default = 0s)
Assign Address Register (1 and 2)	W	188, 189	Refer to Table 76 for bit assignments. Writing a valid 48-bit ID (one that matches the EPROM ID) to this register causes the device to change its Hub ID to the contents of the EPROM ID register listed below. This register cannot be read.
EPROM Address Register (1 and 2)	R	190, 191	These two registers contain the 48-bit ID read in from EPROM at power-up. Refer to Table 77 for bit assignments.

1. R = Read only; W = Write only; R/W = Read /Write.
2. Default value if manager is not present.
3. Default value if manager is present.

Repeater Configuration Register

This register contains many of the global repeater settings. The Repeater Configuration Register is described in Table 71. Refer to Table 70 for bit assignments of the Repeater Configuration Register.

Table 70: Repeater Configuration Register Bit Assignments

31:13	12	11	10	9	8	7	6	5	4	3	2	1:0
Reserved	Enable Port Late Event	Auto Clear	Stats Enable	Send /T/R	Iso 100	Iso 10	Uni-cast Frame Count	Arbit Input Value	Zero Cntrs	Enable FIFO Error	Enable Manchstr Code Violation	Reserved

Table 71: Repeater Configuration Register Bit Definitions

Bit	Name	Type[1]	Description	Default
31:13	Reserved	R/W	Reserved - Write as ‘0s; ignore on read.	N/A
12	Enable PortN Late Event	R/W	A ‘0’ does not allow out-of-window collisions to increment portN’s Late Event Counter. A ‘1’ does allow it.	0
11	Auto-Clear	R/W	A ‘0’ causes Interrupt Status Register and Search Port Match Register to automatically clear when read. A ‘1’ requires that the appropriate register bits be written to be cleared. This is done by writing a ‘1’ to the bit(s) that are to be cleared.	0
10	Statistics Enable	R/W	Turns statistics gathering on and off. A ‘1’ enables statistics gathering. ‘0’ disables statistics gathering.	1
9	Send /T/R	R/W	Forces a good /T/R after each 100 Mbps transmission. A ‘1’ forces /T/R. ‘0’ disables forced /T/R.	0
8	Isolate 100	R/W	Isolates the $\overline{\text{IR100CFS}}$ stack signal and provides an output pin for disabling an external backplane transceiver. A ‘1’ isolates. ‘0’ does not isolate.	0
7	Isolate 10	R/W	Isolates the $\overline{\text{IR10COL}}$ and $\overline{\text{IR10CFS}}$ signals and provides an output pin for disabling an external backplane transceiver. A ‘1’ isolates. ‘0’ does not isolate.	0
6	CountMode	R/W	Changes the definition of portReadableFrames to only count Unicast Frames. A ‘1’ counts Unicast only. ‘0’ counts all.	0
5	Arbitration Input Value	R	As read from input pin.	N/A
4	Zero Counters	R/W	A ‘1’ causes the LXT980 to sequentially walk through each counter location and zero its contents[2]. When all counter locations have been cleared[3], this bit will be reset to a ‘0’.	0

1. R = Read only; R/W = Read/Write.
2. While zeroing is in progress, the CPU will be locked out from accessing the statistics RAM until the Zero Counters bit has been reset back to ‘0’. This will be approximately 15 µs.
3. The rptrMonitorPortBroadcastPkts and rptrMonitorPortMulticastPkts counters (refer to Table 51 on page 70) are not cleared by the Zero Counters bit.

Table 71: Repeater Configuration Register Bit Definitions – continued

Bit	Name	Type[1]	Description	Default
3	Enable FIFO error	R/W	When set to '1', the LXT980 enters transmit collision upon detection of a data rate mismatch.	1
2	Enable Manchester Code Violation	R/W	When set to '1', the LXT980 enters transmit collision upon detection of a Manchester code violation (10 Mbps only)	0
1:0	Reserved	R/W	Reserved - Write as '0s; ignore on read.	N/A

1. R = Read only; R/W = Read/Write.
2. While zeroing is in progress, the CPU will be locked out from accessing the statistics RAM until the Zero Counters bit has been reset back to '0'. This will be approximately 15 µs.
3. The rptrMonitorPortBroadcastPkts and rptrMonitorPortMulticastPkts counters (refer to Table 51 on page 70) are not cleared by the Zero Counters bit.

Table 72: Device/Revision Register Bit Assignment

31:28	27:12	11:8	7:1	0
Version	**Part No.**	**Jedec Continuation Characters**	**JEDEC ID[1]**	**1st in Chain[2]**
0100 (LXT980)	0000 0011 1101 0100	0000	111 1110	See Note 2
0110 (LXT980A)				

1. The JEDEC ID is an 8-bit identifier. However, the MSB is for parity only and is ignored. Level One's JEDEC ID is FE (1111 1110) which becomes 111 1110.
2. First Chain Bit = 0 if ChipID ≠ 000.
   First Chain Bit = 1 if ChipID = 000.

Table 73: Global LED Control Register Bit Assignments

31:6	5	4	3	2	1:0
Reserved	**Mode Control**		**Global Fault LED**		**Reserved**

Table 74: Port LED Control Register Bit Assignments

31:10	9	8	7	6	5	4	3	2	1	0
Rsvd	**Port 5 (MII)**		**Port 4**		**Port 3**		**Port 2**		**Port 1**	

Table 75: LED Timer Control Register Bit Assignments

31:16	15:8	7:0
Reserved	Slow Blink Frequency	Fast Blink Frequency
1. Period = 7.8125 ms x (Register Value + 1) 2. $\text{Frequency} = \frac{1}{7.8125\text{ms} \times (\text{RegisterValue} + 1)}$		

Table 76: Address Assignment Register Bit Assignments

Assign Addr 1	31:0		
	Bits (47:16) of the EPROM Serial number		
Assign Addr 2	31:21	20:16	15:0
	Zeros	Hub ID(4:0)	Bits (15:0) of the EPROM serial number

Table 77: EPROM Address Register Bit Assignments

EPROM Addr 1	31:0	
	Bits(47:16) of the EPROM serial number	
EPROM Addr 2	31:16	15:0
	Zero's	Bits (15:0) of the EPROM serial number

Auto-Negotiation Registers

Table 78: Auto-Negotiation Registers

Name	size bits	Addr	Type[1]	Description
Auto-Negotiate Link Partner Ability #1 (Port 1)	16	09E	R	Refer to Table 79
Auto-Negotiate Link Partner Ability #2 (Port 2)	16	09F	R	
Auto-Negotiate Link Partner Ability #3 (Port 3)	16	0A0	R	
Auto-Negotiate Link Partner Ability #4 (Port 4)	16	0A1	R	
Auto-Negotiate Status #1 (Port 1)	16	0A2	R	Refer to Table 80
Auto-Negotiate Status #2 (Port 2)	16	0A3	R	
Auto-Negotiate Status #3 (Port 3)	16	0A4	R	
Auto-Negotiate Status #4 (Port 4)	16	0A5	R	
Auto-Negotiate Advertisement #1 (Port 1)	16	0A6	R/W	Refer to Table 81
Auto-Negotiate Advertisement #2 (Port 2)	16	0A7	R/W	
Auto-Negotiate Advertisement #3 (Port 3)	16	0A8	R/W	
Auto-Negotiate Advertisement #4 (Port 4)	16	0A9	R/W	
Auto-Negotiate Configuration	8	0AA	R/W	Refer to Table 82

1. R = Read only; R/W = Read/Write.

Table 79: Auto-Negotiation Link Partner Ability Registers

Bit	Name	Description	Type [1]	Default
15	Next Page	1 = Link Partner has ability to send multiple pages 0 = Link Partner has no ability to send multiple pages	R	N/A
14	Acknowledge	1 = Link Partner has received Link Code Word from LXT980 0 = Link Partner has not received Link Code Word from LXT980	R	N/A
13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R	N/A
12:10	Reserved	Write as 0, ignore on read	R	N/A
9	100BASE-T4	1 = Link Partner is 100BASE-T4 capable. 0 = Link Partner is not 100BASE-T4 capable.	R	N/A
8	100BASE-TX full-duplex	1 = Link Partner is 100BASE-TX full-duplex capable. 0 = Link Partner is not 100BASE-TX full-duplex capable.	R	N/A
7	100BASE-TX	1 = Link Partner is 100BASE-TX capable. 0 = Link Partner is not 100BASE-TX capable.	R	N/A

1. R = Read only.

Table 79: Auto-Negotiation Link Partner Ability Registers – continued

Bit	Name	Description	Type [1]	Default
6	10BASE-T full-duplex	1 = Link Partner is 10BASE-T full-duplex capable. 0 = Link Partner is not 10BASE-T full-duplex capable.	R	N/A
5	10BASE-T	1 = Link Partner is 10BASE-T capable. 0 = Link Partner is not 10BASE-T capable.	R	N/A
4:0	Selector Field	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future Auto-Negotiation development. <11111> = Reserved for future Auto-Negotiation development. Unspecified or reserved combinations shall not be transmitted.	R	N/A

1. R = Read only.

Table 80: Auto-Negotiation Status Registers

Bit	Name	Description	Type[1]	Default
15:5	Reserved	Write as zero, ignore on read.	R	
4	Parallel Detection Fault	1 = More than one of the PMAs detects a valid link. 0 = No conflict.	R/LH	
3	Link Partner Next Page Able	1 = Link partner is next page able. 0 = Link partner is not next page able.	R	
2	Next Page Able	0 = Local device is not next page able.	R	
1	Page Received	1 = Three identical and consecutive link code words have been received from link partner. 0 = Three identical and consecutive link code words have not been received from link partner.	R/LH	
0	Link Partner Auto-Negotiation Able	1 = Link partner is auto-negotiate able. 0 = Link partner is not auto negotiate able.	R/LH	

1. R = Read only; LH = Latching high.

Table 81: Auto-Negotiation Advertisement Register

Bit	Name	Description	Type [1]	Default
15	Next Page	1 = Phy has ability to send multi-pages. 0 = Phy has no ability to send multi-pages.	R	0
14	Reserved	Write as zero, ignore on read.	R	0
13	Remote Fault	1 = Remote fault. 0 = No remote fault.	R/W	0
12:10	Reserved	Write as zero	R	0
9	100BASE-T4	1 = 100BASE-T4 capability is available. 0 = 100BASE-T4 capability is not available. The LXT980 does not support 100BASE-T4 operation.	R	0
8	100BASE-TX FD	1 = DTE is 100BASE-TX full-duplex capable. 0 = DTE is not 100BASE-TX full-duplex capable.	R	0
7	100BASE-TX	1 = DTE is 100BASE-TX capable. 0 = DTE is not 100BASE-TX capable.	R[2]	1
6	10BASE-T FD	1 = DTE is 10BASE-T full-duplex capable. 0 = DTE is not 10BASE-T full-duplex capable.	R	0
5	10BASE-T	1 = DTE is 10BASE-T capable. 0 = DTE is not 10BASE-T capable.	R[2]	1
4:0	Selector Field,	<00001> = IEEE 802.3. <00010> = IEEE 802.9 ISLAN-16T. <00000> = Reserved for future auto-negotiation development. <11111> = Reserved for future auto-negotiation development. Unspecified or reserved combinations should not be transmitted.	R	00001

1. R = Read only; R/W = Read/Write.
2. These settings are determined by the port speed control register and the auto negotiate configuration register.

Table 82: Auto-Negotiation Configuration Register

Bit	Name	Description	Type[1]	Default
7	Restart Negotiate (Port 4)	Writing a '1' causes the port to renegotiate if its Auto-Negotiate Enable bit is set to '1'. Writing a '1' to this bit overrides the port external configuration settings. These bits are self-clearing.	W	0
6	Restart Negotiate (Port 3)		W	0
5	Restart Negotiate (Port 2)		W	0
4	Restart Negotiate (Port 1)		W	0
3	Auto-Negotiate Enable (Port 4)	1 = Port auto negotiate is enabled. 0 = Port auto negotiate is not enabled. Enabling auto-negotiation via software requires writing to both the Port Speed Control Register and the Auto-Negotiate Configuration Register (see Table 61 on page 77). If Auto negotiate is not enabled, the port will take on the speed forced values set in the port speed control register. If auto negotiate is enabled, all abilities will be advertised. Forcing a port speed via the port speed control register (refer to Table 61) will always override and disable auto-negotiation.	R/W	1
2	Auto-Negotiate Enable (Port 3)		R/W	1
1	Auto-Negotiate Enable (Port 2)		R/W	1
0	Auto-Negotiate Enable (Port 1)		R/W	1

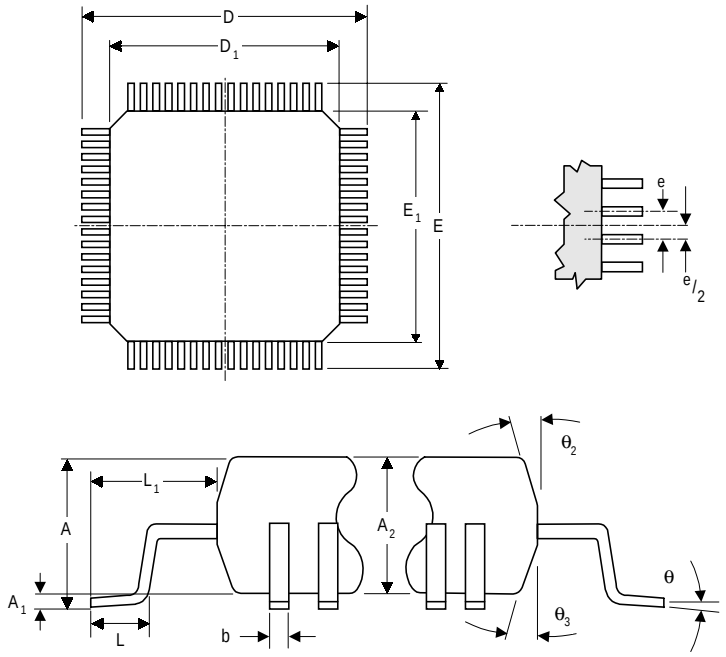
1. W = Write; R/W = Read/Write.

MECHANICAL SPECIFICATIONS

Figure 41: Package Specifications

208-Pin Plastic Quad Flat Package

- Part Numbers:
  - LXT980QC
  - LXT980AHC
- Commercial Temperature Range (0°C to 70°C)



Dim	Millimeters	
	Min	Max
A	-	4.10
A1	0.25	-
A2	3.20	3.60
b	0.17	0.27
D	30.30	30.90
D_1	27.70	28.30
E	30.30	30.90
E_1	27.70	28.30
e	.50 BASIC	
L	0.50	0.75
L_1	1.30 REF	
q	0°	7°
θ_2	5°	16°
θ_3	5°	16°

REVISION HISTORY

Table 83: Changes from Rev 1.3 to 1.4 (3/99)

Section	Page	Change	Description
LED Mode 2	26	Add	Add “Link up” to 10M Blink Description.

Table 84: Changes from Rev 1.2 to Rev 1.3 (2/99)

Section	Page	Change	Description
General Description	1	Add	To the first paragraph, add the following sentence: “This data sheet applies to all LXT980 products (LXT980, LXT980A, and any subsequent variants), except as specifically noted.”
Pin Assignments Figure 1	4	Modify Add	Pin 74: For LXT980A, Pin name is AUTO_BLINK. Add note at bottom of figure.
		Add	Add Data Code, Trace Code, Part#, and Lot# information to pinout figure.
Signal Descriptions	5-14	Modify	Editorial clean-up: re-order, clarify information in “Type” column.
IRB Signal Description	8	Modify	For $\overline{\text{IR100CFSB}}$ signal, change pull-up resistor value from 82Ω to 91Ω.
Power Supply and Indication Signal Description Table 9	13	Add	Add note regarding Pin 74 (see “GND” in Symbol column).
Misc. Signal Desc. Table 11	14	Add	Add note regarding Pin 74 (see “AUTO_BLINK” in Symbol column).
Port LEDS	24	Add	Add “Link Loss” paragraph explaining LED indication during link loss.
LED Mode 1 Table 13	25	Modify Add	To “Port*n*LED3” row: change “No link established” to “No link, (fast blink)”. Add note at bottom of table explaining “AUTO_BLINK” pin for LXT980A.
LED Mode 2 Table 14	26		Correct information and reformat to account for LXT980A and Hardware control for 10M versus 100M operation. Add “AUTO_BLANK” note at the bottom of table.
LED Mode 3 Table 15	27	Delete	For PORT*n*LED row: delete “established” under Blink column.
IRB Signal Details Table 17	29	Modify	For $\overline{\text{IR100CFSBP}}$ signal, change pull-up resistor value from 82Ω to 91Ω .
Typical 100 Mbps Implementation Figure 21	46	Modify	For $\overline{\text{IR100CFSBP}}$ signal, change pull-up resistor value from 82Ω to 91Ω .

Table 84: Changes from Rev 1.2 to Rev 1.3 (2/99) – continued

Section	Page	Change	Description
100 Mbps IRB Electrical Char. Table 28	50	Modify	For $\overline{IR100CFSBP}$, "Test Conditions" column: change RL value from 82Ω to 91Ω.
10 Mbps IRB Receive Timing Parameters Figure 37 Table 45	65	Modify	Change figure and table to correctly represent data to clock prop. delay, not setup and hold times, as previously shown.
10 Mbps IRB Transmit Timing Parameters Figure 38 Table 46	66	Delete	In Table 46: Delete IR10CLK to IR10DAT (output) propagation delay parameter; in Figure 38, delete associated timing references.
Port Counter Regs. Table 51	70	Modify Add	For "rptrMonitorPortRunts" register, 100M operation: change ">92" to "≥ 92". Add Note 2 explaining 100M operation nibble boundaries.
RMON Counter Registers Table 52	72	Add	To"etherStatsOversizePkts" and "etherStatsJabbers" add LXT980 and LXT980A relevant information to Description column.
Gen. Port Con. Regs. Table 59	76	Add	To Port Alternate Partition Algorithm Control Register: add Bit Description information for LXT980A.
Port Learn and Speed Control Regs. Table 61	77		To Port Speed Control Register description: add information on "Enabling auto-negotiation via software".
Device/Revision Reg. Table 72	84	Modify Add	Correct LXT980 value from 0000 to 0100. Add LXT980A value of 0110.
A/N Config. Reg. Table 82	89	Add	To Auto-Negotiation Configuration Register description: add information on "Enabling auto-negotiation via software".
Mechanical Specs.	90	Add	Add LXT980AHC part number.
Backpage	100	Modify	Update.

Table 85: Changes from Rev 1.1 to Rev 1.2 (12/98)

Section	Page	Change	Description
Features	1	Modify	Change 0 - 70° temperature range to “Case temperature range: 0 - 115°.
Pin Assign Figure 1	4	Correct	Change IRQ to $\overline{\text{IRQ}}$ to correctly indicate as “Active Low”.
			Change Macactiv to Macactive. (Correct text throughout.)
Mode Control Signals Table 1	5	Add	Add “PD” to CONFIG<0:7> Type column.
MAC Mode MII Interface Signal	7	Delete	Delete last sentence in “Transmit Error” description.
IRB Signals Table 4	7	Modify	Re-write, expand description of $\overline{\text{IR100CFS}}$ signal.
	8		Re-write, expand description of $\overline{\text{IR100CFSBP}}$, and $\overline{\text{IR100DV}}$ signals.
			Change $\overline{\text{IRDEN}}$ to $\overline{\text{IR100DEN}}$.
		Add	Add “Schmitt MOS PU” to IR100SNGL, IR100COL, IR100DV, IR100DAT<0:4>.
			Add “PD” to IR100CLK.
			Add a 1k pull-up resistor to IR100CLK; modify description accordingly.
	9	Modify	Change $\overline{\text{IRDEN}}$ to $\overline{\text{IR10DEN}}$.
		Add	Add “PD” to IR10DAT, IR10CLK.
			Add “MOS PU” to IR10ENA, IR10COL.
		Modify	Change “Analog” to “MOS” on IR10COLBP.
			Re-write, expand description of $\overline{\text{IR10CFS}}$, $\overline{\text{IR10CFSBP}}$, and MACACTIVE signals. Change “IRCFS” to $\overline{\text{IR10CFS}}$.
Twisted-Pair Port Signals	10	ADD	To “Twisted-Pair Outputs and “Twisted-Pair Inputs” descriptions add “These pins can be left open when not used.”
SMI Signals	11	Add	Add “PD” to SERCLK.
		Modify	Re-write Arbitration In/Out description.
			To Manager Present description, change first sentence to read: “This signal is sensed at power up *and hardware reset*.”
Power Supply & Indication Signals Table 9	13	Modify	Replace “-” under Type column with respective “Analog” and “Digital” indications.
			Change “1% 22 kΩ resistor” to “22.1 kΩ, 1% resistor.
PROM Interface Table 10	14	Modify	Re-write, expand descriptions of PROM_CS and PROM_DTOUT.
		Add	Add “PD” to PROM_CLK, PROM_DTN.
		Delete	Delete “PD” from PROM_CS, PROM_DTOUT.
MII	20	Add	Add following note: The MII does not auto-negotiate, auto speed change, auto-link, or partition.

Table 85: Changes from Rev 1.1 to Rev 1.2 (12/98) – continued

Section	Page	Change	Description
Repeater Operation	21	Add	Add “or one long collision approximately 575.2 µs long”.
		Modify	In Un-isolate bullet: change “transmits” to “receives”.
			In Jabber bullet: change “all receivers” to “all jabbering receivers”.
Power Requirements	23	Modify	Re-write first and second sentences under “Power” heading.
Bias Resistor			Change “1% 22 kΩ resistor” to “22.1 kΩ, 1% resistor.
IRB Bus Pull-ups	23	Add	Add IR100CLK.
MAC IRB Access	27	Modify	Re-write first sentence to indicate MACACTIVE is a “TTL-level” pin.
IRB Isolation		Add	Add a NOTE: “Inter-board analog signals will be isolated internally by the device.”
IRB Signal Details Table 17	28	Modify	Change “No” to “1 kΩ” under Pull-up heading for IR100CLK signal.
			Change $\overline{\text{IR100CFSBP}}$ pull-up resistor value to 82Ω.
MII Port Operation	29	Delete	Delete first sentence of 2nd paragraph.
MII Port Timing Considerations	30	Modify	Re-write paragraph.
MII Timing Issues Figure 8			Clarify MII-to-MII, PHY-to-MAC Prop. Delay.
Auto-Clearing Registers	31	Add	Add description/explanation of “Clear on Read” Registers.
SMI Message Fields Table 19	32	Modify	For Chip ID message: change “eight modules” to “eight LXT980 devices on a board or sub-system”.
Chain Arbitration	35	Add	To second paragraph, add the following sentence: “Tie to ARBOUT of the SCC or to previous hub in the daisy chain. The first hub ARBIN can also be grounded.”
Address Re-arbitration			Add the following sentences: “This message will be sent regardless of arbitration method; however, with “Chain” arbitration mechanism, it will be sent once. The message can be ignored.”
General Design Guidelines	37-38	Modify	Update section; remove references to separate analog & digital ground planes and associated ferrite bead filter.
RBIAS Pin	38	Modify	Change “1% 22 kΩ resistor” to “22.1 kΩ, 1% resistor.
Magnetics Information Table 23 Table 24	39	Modify	Remove Suggested Magnetics List and update Magnetics Specifications. Move differential to CMR from “Min” to “Max” column; indicate as -40 and -35 for.1 to 60 MHz and 60 to 100 MHz, respectively.
Pwr & Gnd Connections Figure 18	42	Modify	Removed filter bead separating Analog and Digital grounds. Change “1% 22 kΩ resister” to 22.1 kΩ, 1%.

Table 85: Changes from Rev 1.1 to Rev 1.2 (12/98) – continued

Section	Page	Change	Description
Twisted-Pair Port Interface Figure 20	44	Modify	Reverse RJ45 connections to show repeater I/F, not NIC. Should be: TPOP = 3, TPON = 6 TPIP = 1, TPIN = 2
Typ. 100 Mbps IRB Implement Figure 21	45	Add	Add two 1 kΩ resistors to IR100CLK line, on either side of the ‘245 buffer.
		Modify	Change $\overline{\text{IR100CFSBP}}$ pull-up resistor value to 82Ω.
Test Specifications	47	Modify Delete	Re-write “NOTE”; Delete “Over Recommended Range” from all Table titles (28-49).
Absolute Max Ratings Table 25		Modify	Increase Max Case Temp to 130.
			Revise Warning to address immediate EOS damage.
100 Mbps IRB Electrical Characteristics	48	Modify	Change $\overline{\text{IR100CFSBP}}$ Test Condition R_L value to 82Ω.
10 Mbps IRB Electrical Characteristics Table 29	49	Modify	Output Low voltage: Change Min, Typ, and Max values. IR10CFS current for single drive: Change Typ value. IR10CFS/BP voltage for single drive and collision: change Min, Typ, and Max values.
Test Spec Tables 33 - 48	51-65	Modify	Clarify definition of Bit times (BT) for both 10 and 100BASE-TX. This appears as a note to the “Unit” column.
			Change Timing Parameter Symbol convention.
Test Spec Figures 25 - 40			Modify figures to correspond to Timing Parameter convention changes.
Test Spec Figure 34 Table 42	60	Delete	Delete “TX_EN sampled to TPOP active (Tx latency)”.
10T Tx Timing Table 42		Modify	Modify TX_EN sampled to CRS asserted Min, Typ, and Max values.
10T Rx Timing Table 43	61	Modify	TPIP/N in to CRS asserted: change MIN, Typ, and Max values. CRS asserted to RXD, RX_DV, RX_ER: change MIN, Typ, and Max values. TPIP/N in to COL asserted: change MIN, Typ, and Max values.
100 IRB Timing Table 44 Figure 36	62	Delete Modify	Delete IR100ENA asserted to TPOP/N or FIBOP/N active and corresponding figure element.
			TPIP/N or FIBP/N to IR100DV Low: change Min, Typ, and Max values.
10 Mbps IRB Receive Timing Table 45	63	Modify	TPIP/N to IR10ENA Low: change Min, Typ values.

Table 85: Changes from Rev 1.1 to Rev 1.2 (12/98) – continued

Section	Page	Change	Description
10 IRB Tx Timing Table 46	64	Modify	IR10ENA asserted to TPOP/N active: change Min, Typ, and Max values.
Port Counter Register Table 51	67	Modify	rptrMonitorPortShortEvents counter should increment as follows: 10M: Count events ≤ 80 bit times. 100M: Count events ≤ 88 bit times.
			rptrMonitorPortRunts counter should increment as follows: 10M: Count events > 80 and ≤ 504 bit times. 100M: Count events > 92 and ≤ 504 bit times.
RMON Counter Registers Table 52	69 - 70	Add	To “etherStatsBroadcastPkts” description add: “Counter is not cleared by ZeroCount bit. To “rptrMonitorTotalOctets” description add: “Counter is not cleared by ZeroCount bit.
Repeater Reset Register Table 69	78	Correct	Rewrite “Repeater Reset Register” description. Rewrite “Software Reset Register” description.
LED Timer Control Register Table 75	81	Correct	Bit Assignments 15:8 is “Slow Blink Frequency”; 7:0 is Fast Blink Frequency.
Throughout	All	Modify	Replace “module” with “board” where appropriate.
All	All	Modify	Light editing throughout.
Backpage	94	Modify	Update

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Table 86: Changes from Rev 1.0 to Rev 1.1

Section	Page	Change	Description
Table 1, Mode Control Signals	5	Add	Added Pull-up notation to port select signals
Table 4, IRB Signals	8	Add	Add Pull-down notation to pin 199, MMSTRIN. Added Schmitt Trigger info to IR100CLK
Table 7, Serial I/F Signals	11	Add/ Correct	Added Pull-down & pull-up notations to various signals. Changed SERCLK type from Output to Input/Output
Table 8, LED Signals	12	Add/ Correct	Changed type from Open Drain to Active Low Output. Added Pull-down notation to LED select signals
Table 9, Power Signals	13	Addition	Added Pull-down notations to RPS_PRES signal. Added Pull-up notations to RPS_FAULT signal.
Table 10, Mode PROM Signals	14	Add	Added note to PROM_CLK description regarding applicability to ChipID=0.
Table 11, Misc. Signals	14	Add	Added Pull-down notations to ChipID signals.

Table 86: Changes from Rev 1.0 to Rev 1.1 – continued

Section	Page	Change	Description
Functional Description	15-35	Modify	Editorial rewrite of sections on Repeater Operation, IRB Operation, MII Port Operation.
Figure 5 App Block Diagram	17	Modify	Added serial termination resistors to MII outputs.
Tables 16 & 17, IRB Signals	27	Add	Added new tables to clarify interconnection and pull-up requirements.
Chain Arbitration	35	Add	Add sentence: “Tie to ARBOUT of the SCC or to previous hub in the daisy chain. The first hub ARBIN can also be grounded.”
Application Information	36-37	Modify & Add	Revised and expanded write-ups on general design guidelines, power & gnd filtering, TP & fiber interfaces, etc.
Table 23, Magnetics List	38	Add	Expanded list of available magnetics.
Table 23, Magnetics Specs	38	Add	Added Return Loss specs for ‘Enhanced’ magnetics.
Figure 18 Pwr & Gnd	41	Add	Added new diagram showing Power & Ground circuits
Figure 19 Fiber I/F	42	Modify	Deleted Note 1 suggesting digital supply for fiber bias circuit in combination TP & fiber applications.
Figure 20 TP I/F	43	Modify & Add	Changed Note 2 to refer to TPI bypass cap, instead of chassis gnd bypass. Added new material showing compensating inductor.
Figure 21 100M IRB	44	Modify	Added pull-ups to ChipID 1 & 2, and added Note specifying treatment of IR100CFSBP.
Figure 22 10M IRB	44	Modify	Added pull-ups to ChipID 1 & 2, and added Note specifying treatment of IR10CFSBP and IR10COLBP.
Table 24, Absolute Max Ratings	46	Add	Added Max Case Temp.
Table 25, Ops Conditions	46	Add & Modify	Added Max Case Temp. Increased FX Mode power consumption.
Table 27 I/O Characteristics	47	Add	Defined Schmitt Trigger specs as applicable to CLK25 & RESET
Table 28 IRB100 Characteristics	47	Add	Added Schmitt Trigger specs for IR100CLK.
Table 29, IRB10 Characteristics	48	Add	Added Schmitt Trigger specs for IR10CLK. Expanded table to address single & double drive values.
Table 30, TX Characteristics	48	Modify	Modified parameters to match LXT970.
Table 31, FX Characteristics	49	Modify	Modified parameters to match LXT970.
Figure 27 100TX Receive	52	Correct	Corrected diagram to match table (show tDPD instead of tDSU/tDH).

Table 86: Changes from Rev 1.0 to Rev 1.1 – continued

Section	Page	Change	Description
Tables 34, 36, 38, 40 & 42 Tx Timing	51-59	Modify	Changed t_{DH} (data hold from clock high) from 0 to 5 ns.
Table 46 10IRB Tx Timing	63	Correct	Corrected parameter symbols for t_{IRDPD} and t_{IRTPON}
Table 61 Gen Port Control Registers	72	Modify	Added info to clarify the default and alternate partition algorithms.
Table 68 Interrupt Register	75	Correct & Add	Reversed settings. Was active low (0 = interrupt. 1 = no interrupt, default). Now active high (1 = interrupt. 0 = no interrupt, default). Added material on Jabber, Isolate & Partition conditions. Added info to clarify mask/no mask settings.
Table 73 Rptr Config Reg	80	Modify	Renamed bit 11 as ‘Auto-Clear’ and rewrote description to clarify function. Changed default value of bit 9 from 1 to 0.
Figure 41 Pkg Specs	87	Modify	Replaced ‘basic’ values with min & max for D, D1, E and E1.

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Revision	Date	Status
1.4	03/99	Minor correction to LED Mode 2 Indications description.
1.3	02/99	Add A8 design revision; minor editing.
1.2	12/98	Additions to Signal Descriptions; add Clear on Read description; correct Twisted-Pair Interface figure; add Transmit/Receive Timing Parameter values.

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