OKI Semiconductor

MSM6598

80-DOT COMMON DRIVER

GENERAL DESCRIPTION

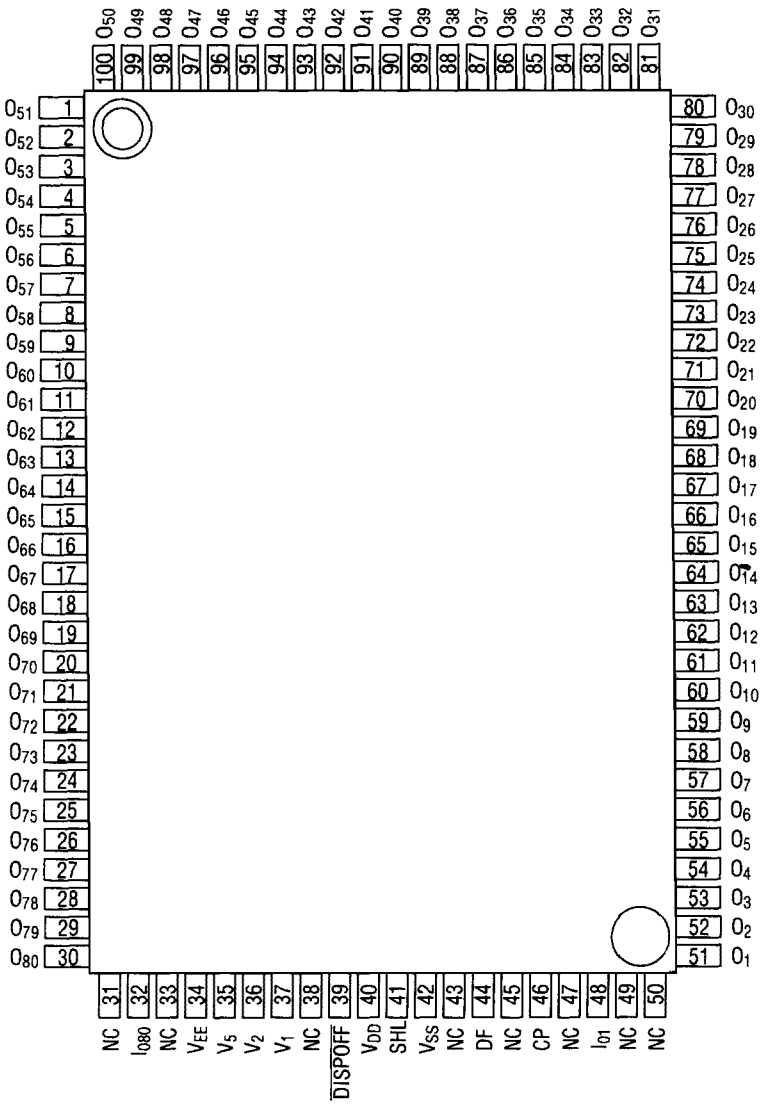
The MSM6598 GS is an LCD dot matrix common driver. This CMOS IC is composed of an 80-bit bidirectional shift register, level shifters for each bit, and a 4-level driver. The 80-line LCD output can be increased by adding an IC using the I/O terminals in a cascade connection. Bias power can be freely supplied externally to support a wide range of liquid crystal panels.

FEATURES

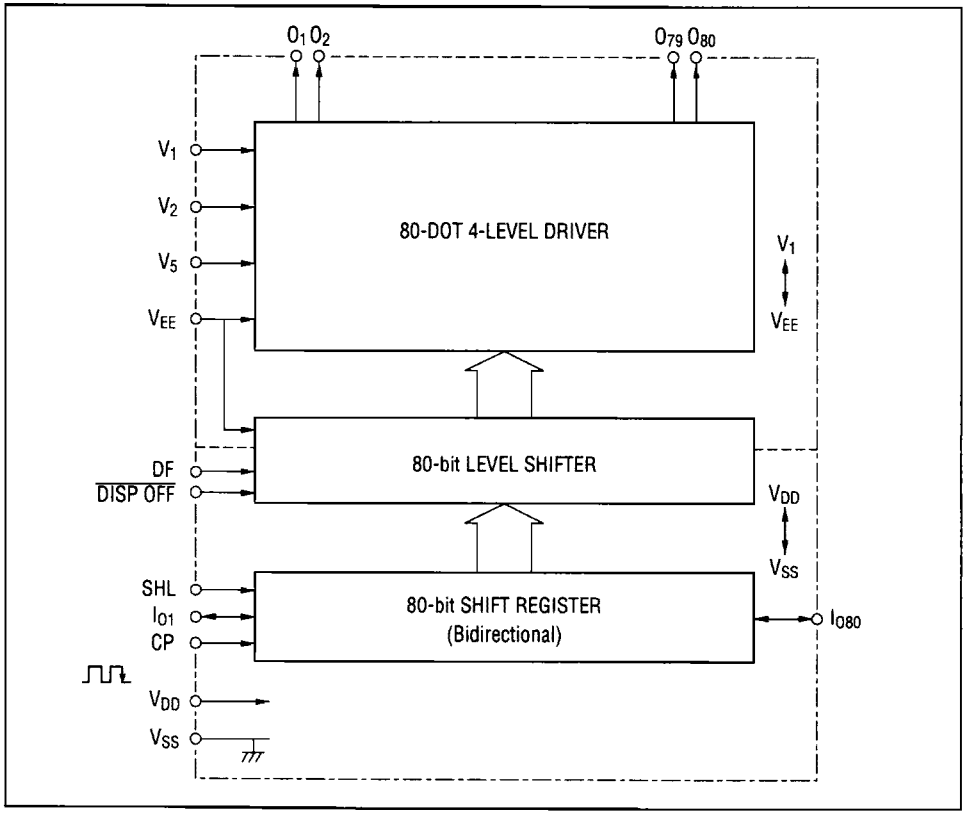
- Logic power voltage: 4.5 V to 5.5 V
- Liquid crystal driving voltage: wide 18 to 30 V range
- Supports 1/64 to 1/256 duty liquid crystal panel
- Liquid crystal output: 80
- Bias power can be supplied externally
- 100-pin plastic QFP (Quad Flat Package)
  (QFP 100-P-1420-K)

PIN CONFIGURATION

(Top View)
100 Lead Plastic Quad Flat Package



FUNCTIONAL BLOCK DIAGRAM



ELECTRIC CHARACTERISTICS

• Absolute Maximum Rating

Parameter	Symbol	Condition	Rating	Unit
Power Voltage (1)	V_{DD}	Ta = 25°C	-0.3 to 6.5	V
Power Voltage (2)	$V_{DD} - V_{EE}$ *1	Ta = 25°C	0 to 32	V
Input Voltage	V_I	Ta = 25°C	-0.3 to V_{DD} + 0.3	V
Storage Tempeature	T_{stg}	-	-55 to +150	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$

• Operation Range

Parameter	Symbol	Condition	Rating	Unit
Power Voltage (1)	V_{DD}	-	4.5 to 5.5	V
Power Voltage (2)	$V_{DD} - V_{EE}$ *1	-	18 to 30	V
Operating Temperature	T_{OP}	-	-20 to +75	°C

*1 $V_1 > V_2 > V_5 > V_{EE}$, $V_1 \leqq V_{DD}$

• DC Characteristics

(V_{DD} = 5V ±10%, Ta = -20 to +75°C)

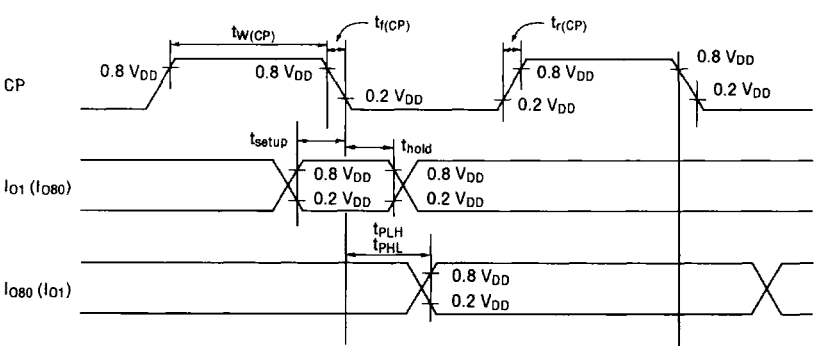
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
H Input Voltage	V_{IH} *1	–	0.8V_{DD}	–	–	V
L Input Voltage	V_{IL} *1	–	–	–	0.2V_{DD}	V
H Input Current	I_{IH} *1	V_{IH} = V_{DD} V_{DD} = 5.5V	–	–	1	µA
L Input Current	I_{IL} *1	V_{IL} = 0V V_{DD} = 5.5V	–	–	-1	µA
H Output Voltage	V_{OH} *2	I_O = -0.4mA V_{DD} = 4.5V	V_{DD}-0.4	–	–	V
L Output Voltage	V_{OL} *2	I_O = 0.4mA V_{DD} = 4.5V	–	–	0.4	V
ON Resistance	R_{ON} *4	V_{DD}-V_{EE} = 25V V_{DD} = 4.5V $\lvert V_N - V_O \rvert$ = 0.25V	–	–	1.0	kΩ
Current Consumption	I_{DD}	CP = 28 kHz V_{DD} = 5.5V V_{DD}-V_{EE} = 25V No load	–	–	100	µA
Input Capacity	C_I	f = 1 MHz	–	5	–	pF

*1 Applicable to CP, I_{O1}, I_{O80}, SHL, DF, $\overline{DISPOFF}$ terminals
*2 Applicable to I_{O1}, I_{O80} terminals
*3 VN = V_{DD} to V_{EE}, V_2 = 1/16 (V_{DD}-V_{EE}), V_5 = 15/16 (V_{DD}-V_{EE}), V_{DD} = V_1
*4 Applicable to O_1 to O_{80} terminals

• Switching Characteristics

(V_{DD} = 5V ±10%, Ta = -20 to +75°C, CL = 15pF)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
"H", "L" Propagation Delay Time	t_{PLH} t_{PHL}	–	–	–	250	ns
Maximum Clock Frequency	f_{CP}	–	1	–	–	MHz
CP Pulse Width	$t_{w(CP)}$	–	63	–	–	ns
Data Setup Time I_{O1} (I_{O80}) → CP	t_{setup}	–	100	–	–	ns
Data Hold Time CP → I_{O1}(I_{O80})	t_{hold}	–	100	–	–	ns
CP Rise, Fall Time	$t_{r(CP)}$,$t_{f(CP)}$	–	–	–	50	ns



TRUTH TABLE

DF	Latch Data	$\overline{DISPOFF}$	Driver Out (O_1 to O_{80})
L	L	H	V_2
L	H	H	V_{EE}
H	L	H	V_5
H	H	H	V_1
X	X	L	V_1

PIN DESCRIPTION

- **I_{O1}, I_{O80}, SHL**
  Input/Output terminals of the 80-bit bidirectional shift register. Shift direction is selected by the SHL terminal. Table 1 shows I_{O1}, I_{O80} and SHL functions.

SHL	Shift Direction	I_{O1}/I_{O80}	Input/Output	Function
L	$O_1 \rightarrow O_{80}$	I_{O1}	Input	Scan data input terminal of shift register, inputs data synchronously with clock. Note 1.
		I_{O80}	Output	Shift register output terminal, outputs data synchronously with clock pulse with delay of number of bits (80) of scan data input from I_{O1} terminal. For a cascade connection, see the application circuit example.
H	$O_{80} \rightarrow O_1$	I_{O80}	Input	Scan data input terminal of shift register, inputs data synchronously with clock. Note 1.
		I_{O1}	Output	Output terminal of shift register, outputs data synchronously with clock pulse with delay of number of bits (80) of scan data input from I_{O80} terminal. For a cascade connection, see application circuit example.

< Table 1 >

Note 1
Relationship between scan data (I_{O1}, I_{O80}) and liquid crystal drive output (O_1 to O_{80}) is shown in Table 2.

I_{O1}, I_{O80}	Liquid Crystal Drive Output
"H"	Selected level (V_1, V_{EE})
"L"	Unselected level (V_2, V_5)

< Table 2 >

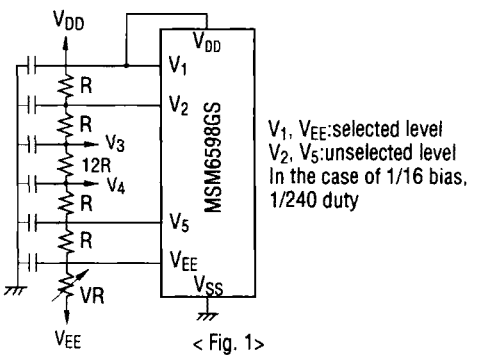
- **CP**
  Shifts scan data at trailing edge of clock pulse of 80-bit bidirectional shift register.

- **DF**
  Signal input terminal for AC synchroniza-tion of liquid crystal drive waveform. Inputs regular frame inversion signals.

- **V_{DD}, V_{SS}**
  Power terminals of the MSM6598GS. Usually V_{DD} = 4.5V to 5.5V, and V_{SS} is GND terminal used with V_{SS} = 0V.

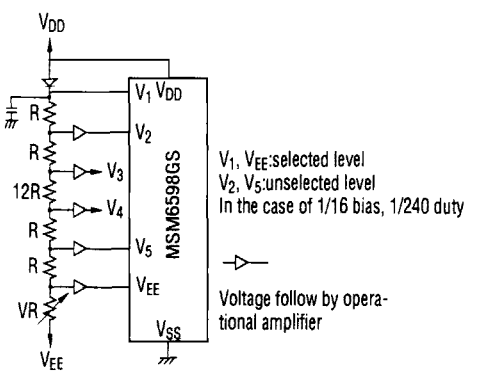
- **$\overline{\text{DISP OFF}}$**
  Input terminal to control O_1 to O_{80} output terminals. V_1 level is output from O_1 to O_{80} terminals when at "L" level input. See the "Truth Value Table".

- **V_1, V_2, V_5, V_{EE}**
  Bias power terminals for liquid crystal drive. Usually bias power supply is used by resistive division. Fig. 1 shows when bias voltage is supplied for liquid crystal driving by resistive division. The V_1 terminal can be used separately from the V_{DD} terminal.



< Fig. 1>

Fig. 2 shows when bias voltage is supplied using an operational amplifier. Low impedance of bias power supply and low current consumption is possible by using an operational amplifier.

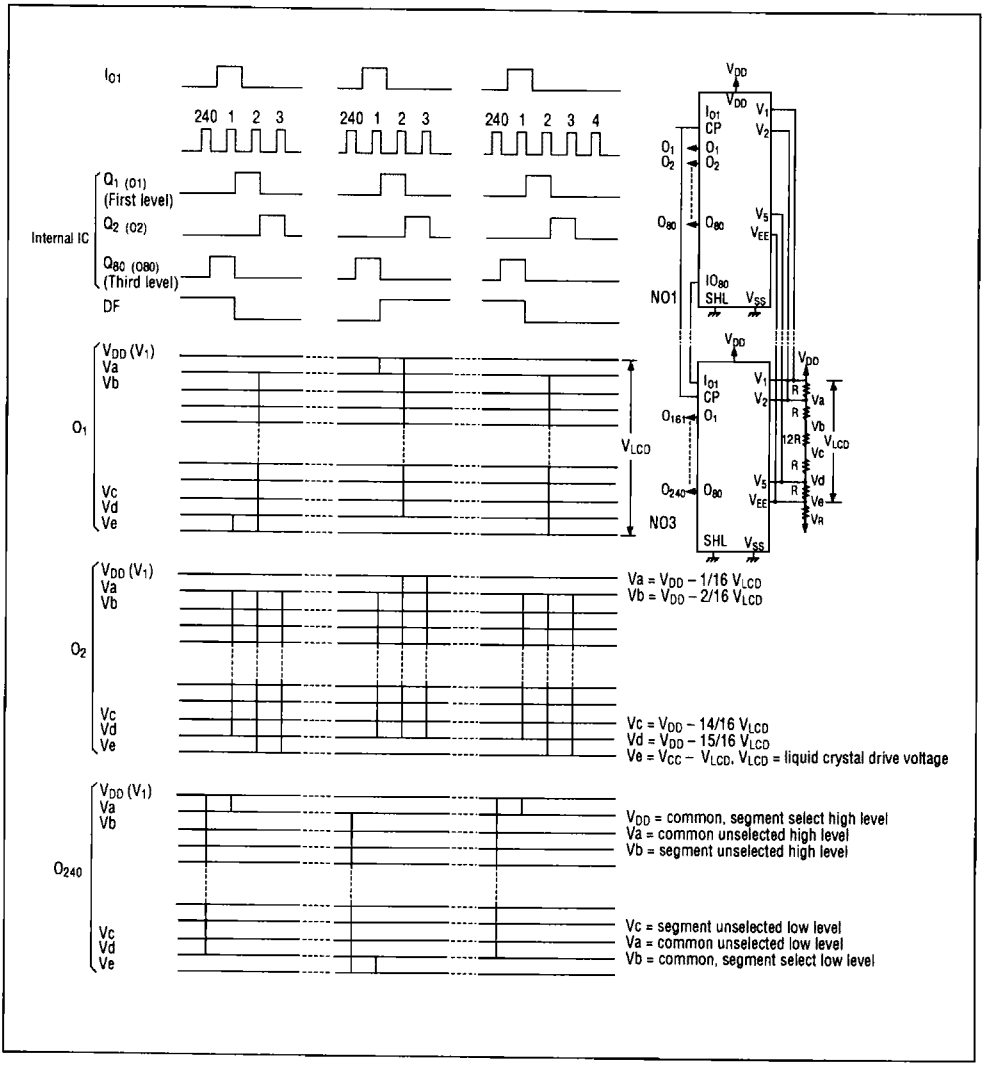


< Fig. 2>

- **O_1 to O_{80}**
  Output terminals for the 4-level driver of the MSM6598GS. Terminals directly correspond to each bit of shift register. One of four levels, V_1, V_2, V_5 and V_{EE}, is selected and output by a combination of shift register data and DF signals. See the "Truth Value Table". Connect this output to the common side of liquid crystal panel.

Note: Precautions when turning power ON/OFF:
This IC releases a high voltage in the liquid crystal drive system. If a high voltage is applied to the system when the power of the logic system is in floating status, excess current flows, and the IC may be damaged. Follow the sequence below when turning power ON/OFF.
When turning power ON:
Logic system ON → liquid crystal drive system ON, or both systems ON at same time.
When turning power OFF:
Liquid crystal drive system OFF → Logic system OFF, or both systems OFF at same time.

TIMING CHART (1/240 duty, 1/16 bias)



APPLICATION CIRCUIT