SONY CXK5863P/M/J 25/30/35

8192-word × 8-bit High Speed CMOS Static RAM

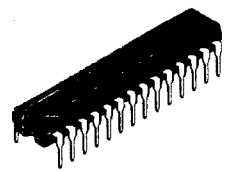
Description

CXK5863P/M/J are 65,536 bits high speed CMOS static RAMs organized as 8,192 words by 8-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

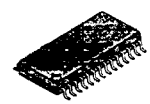
Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μW (Typ.)
- Low power operation 150mW (Typ.)
- Single + 5V supply : 5V ± 10%
- Fully static memory···No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output three state output.
- Directly TTL compatible all inputs and outputs.
- Low voltage data retention 2.0V (Min.)
- Full CMOS.
- Available in 28 pin 300mil DIP, 450mil SOP, 300mil SOJ.

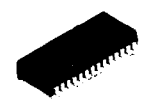
CXK5863P
28 pin DIP (Plastic)



CXK5863M
28 pin SOP (Plastic)



CXK5863J
28 pin SOJ (Plastic)



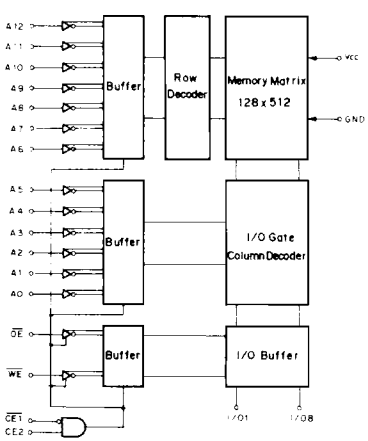
Structure

Silicon gate CMOS IC

Function

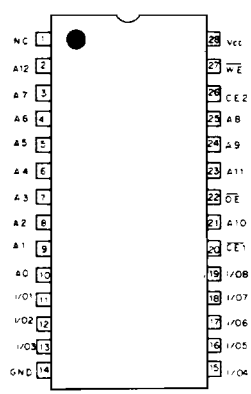
8192-word × 8-bit static RAM

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O8	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground
NC	Non connection

E89739 - ST

Absolute Maximum Ratings Ta = 25°C, GND = 0V

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		− 0.5* to + 7.0	V
Input voltage	V_{IN}		− 0.5* to V_{CC} + 0.5	V
Input and output voltage	$V_{I/O}$		− 0.5* to V_{CC} + 0.5	V
Allowable power dissipation	P_D	CXK5863P/J	1.0	W
		CXK5863M	0.7	W
Operating temperature	Topr		0 to + 70	°C
Storage temperature	Tstg		− 55 to + 150	°C
Soldering temperature	Tsolder		260 • 10	°C • sec

***Note**) V_{CC}, V_{IN}, $V_{I/O}$ = − 3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O8	V_{CC} Current
H	X	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
X	L	X	X	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	X	L	Write	Data in	I_{CC1}, I_{CC2}

X : "H" or "L"

DC Recommended Operating Conditions Ta = 0 to + 70°C, GND = 0V

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC} + 0.3	V
Input low voltage	V_{IL}	− 0.3*	—	0.8	V

***Note**) V_{IL} = − 3.0V Min. for pulse width less than 20ns.

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Electrical Characteristics

DC and operating characteristics

V_{CC} = 5V ± 10%, GND = 0V, Ta = 0 to +70℃

Item	Symbol	Test condition	−25/30/35			Unit
			Min.	Typ.*	Max.	
Input leakage current	I_{LI}	V_{IN} = GND to V_{CC}	−1	—	1	μA
Output leakage current	I_{LO}	$V_{I/O}$ = GND to V_{CC}, $\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}	−1	—	1	μA
Operating power supply current	I_{CC1}	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH}, V_{IN} = V_{IH} or V_{IL} I_{OUT} = 0mA	—	30	60	mA
Average operating current	I_{CC2}	Cycle = Min, Duty = 100%, I_{OUT} = 0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1}$ ≧ V_{CC} − 0.2V or CE2 ≦ 0.2V V_{IN} ≧ V_{CC} − 0.2V or V_{IN} ≦ 0.2V	—	1	100	μA
	I_{SB2}	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}, V_{IN} = V_{IL} or V_{IH}	—	10	25	mA
Output high voltage	V_{OH}	I_{OH} = −4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL} = 8.0mA	—	—	0.4	V

* V_{CC} = 5V, Ta = 25℃

I/O capacitance

Ta = 25℃, f = 1MHz

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN} = 0V	—	7	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	10	pF

Note) This parameter is sampled and is not 100% tested.

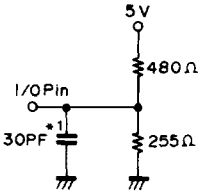
AC characteristics

• AC test conditions

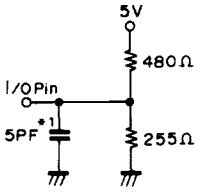
V_{CC} = 5V ± 10%, Ta = 0 to +70℃

Item	Condition
Input pulse high level	V_{IH} = 3.0V
Input pulse low level	V_{IL} = 0V
Input rise time	tr = 5ns
Input fall time	tf = 5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



* 1. including scope and jig capacitance

* 2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WHZ}

Fig. 1

• **Read cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t_{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t_{OE}	—	15	—	15	—	20	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}* t_{LZ2}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}* t_{HZ2}*	0	15	0	15	0	20	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	13	0	13	0	15	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	20	—	20	—	20	ns

• **Write cycle**

Item	Symbol	−25		−30		−35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	12	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	20	—	25	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	13	0	13	0	15	ns

* Transition is measured ±500mV from steady voltage with specified loading in Fig. 1-(2). This parameter is sampled and is not 100% tested.

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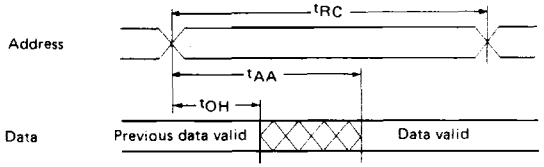
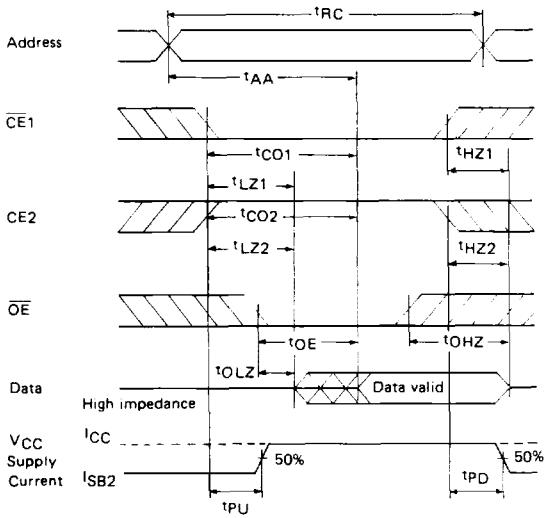
Timing Waveform

1) Read cycle

• Read cycle No. 1 : [$\overline{CE1}$ = $\overline{OE}$ = V_{IL}, CE2 = V_{IH}, $\overline{WE}$ = V_{IH}]

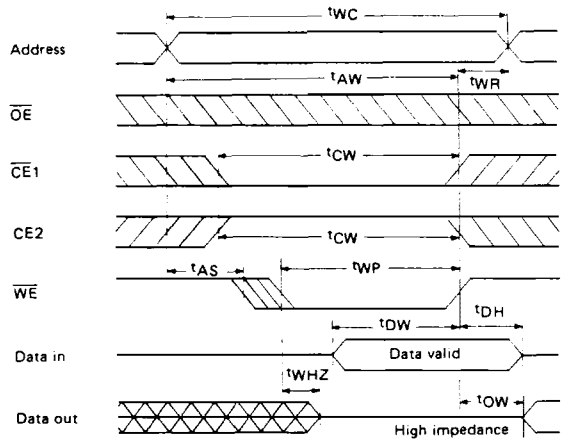


• Read cycle No. 2 : [$\overline{WE}$ = V_{IH}]

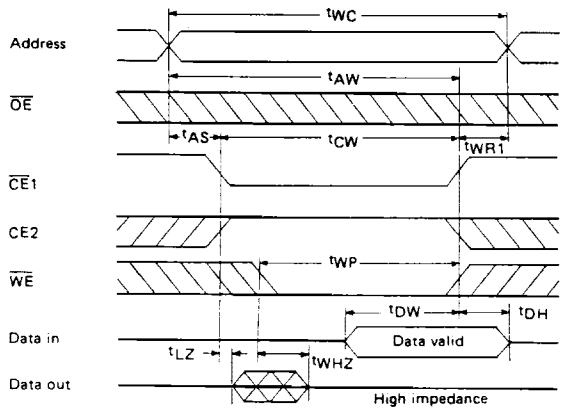


2) Write cycle

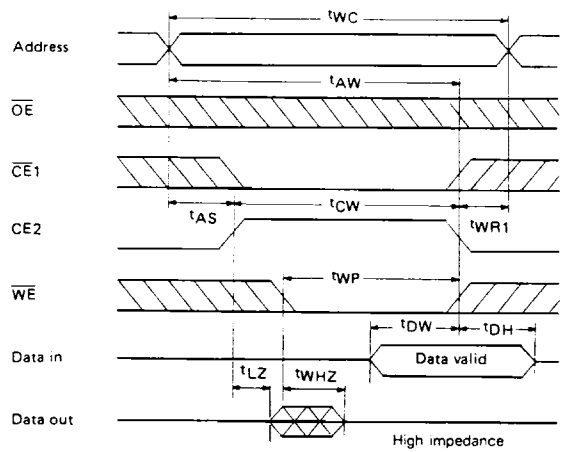
• Write cycle No. 1 : [$\overline{WE}$ control]



• Write cycle No. 2 : [$\overline{CE1}$ control]



• Write cycle No. 3 : [CE2 control]



During I/O pins are in the output state, the data input signals of opposite phase to the output must not be applied.

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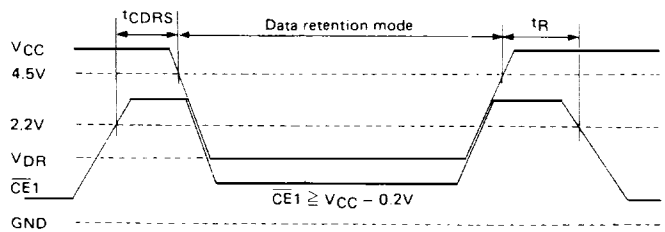
Data Retention Characteristics Ta = 0 to + 70°C

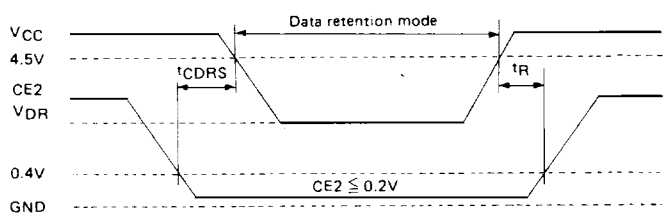
Item	Symbol	Test condition	– 25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	V_{CC} = 3.0V *1	—	0.5	50	µA
	I_{CCDR2}	V_{CC} = 2.0 to 5.5V *1	—	1.0	100	µA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

*1 $\overline{CE1} \geqq V_{CC} - 0.2V$ or $CE2 \leqq 0.2V$, $V_{IN} \geqq V_{CC} - 0.2V$ or $V_{IN} \leqq 0.2V$
*2 t_{RC} : Read cycle time

Data Retention Waveform (1) : [$\overline{CE1}$ control]

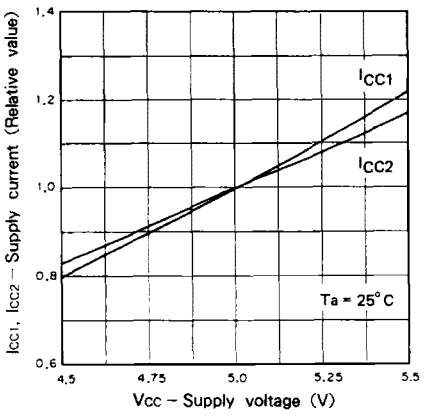


Data Retention Waveform (2) : [CE2 control]

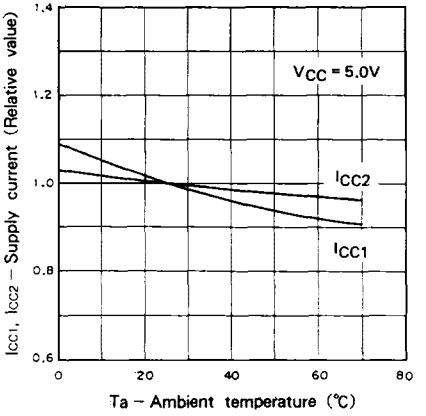


Example of Representative Characteristics

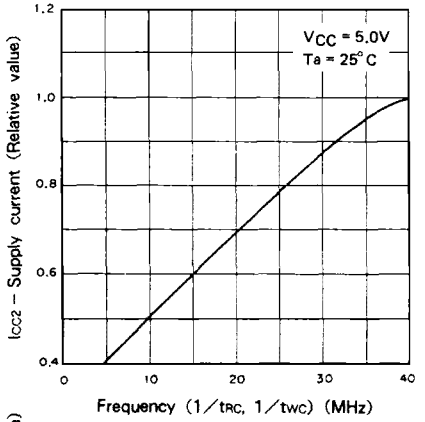
Supply current vs. Supply voltage



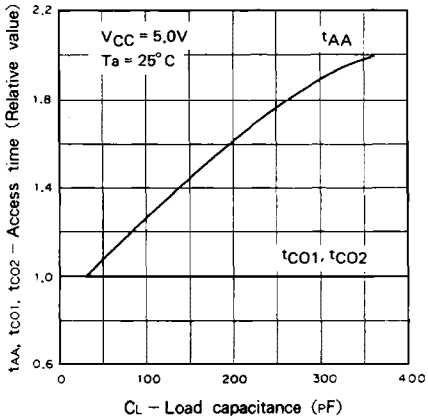
Supply current vs. Ambient temperature



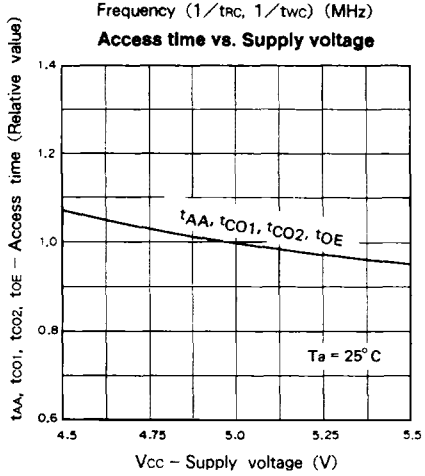
Supply current vs. Frequency



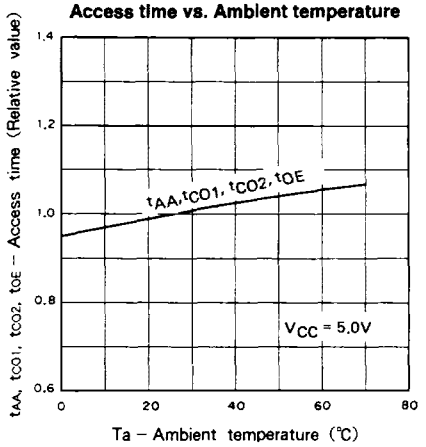
Access time vs. Load capacitance



Access time vs. Supply voltage



Access time vs. Ambient temperature



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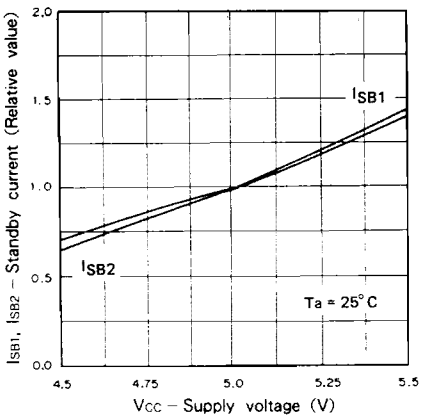
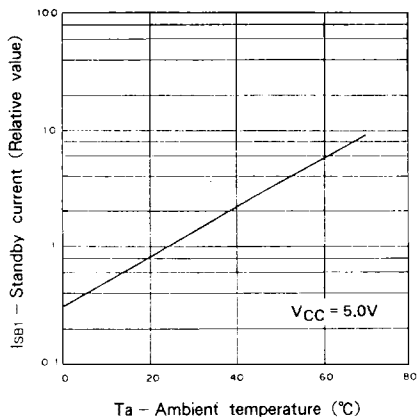
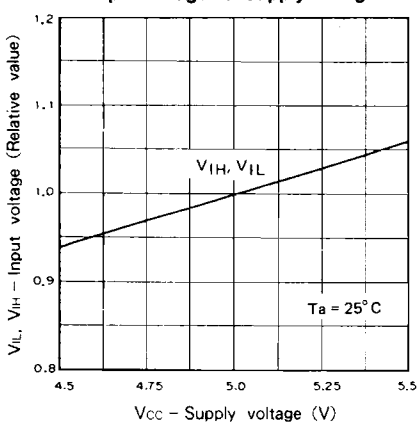
Standby current vs. Supply voltage



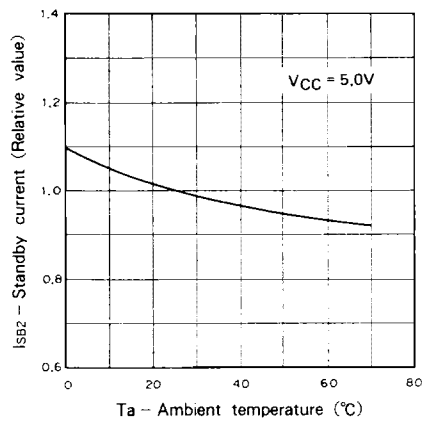
Standby current vs. Ambient temperature



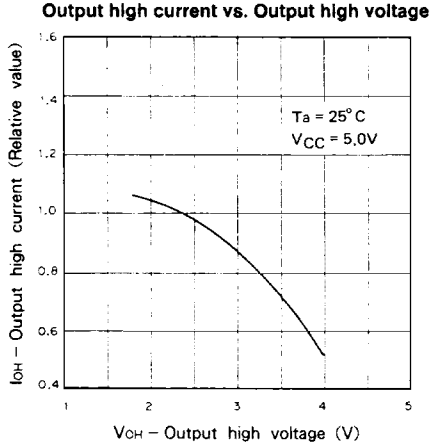
Input voltage vs. Supply voltage



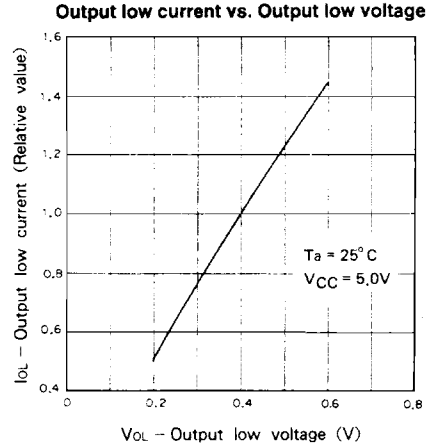
Standby current vs. Ambient temperature



Output high current vs. Output high voltage

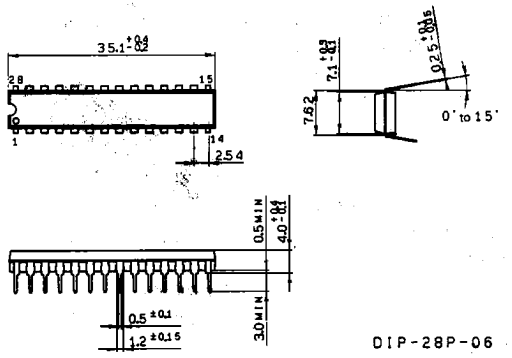


Output low current vs. Output low voltage



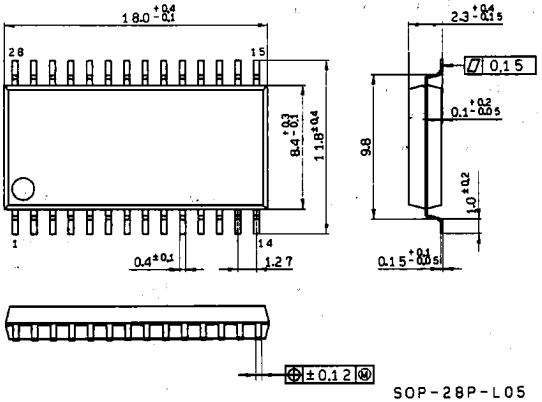
Package Outline Unit : mm

CXK5863P 28 pin DIP (Plastic) 300mil 2.0g



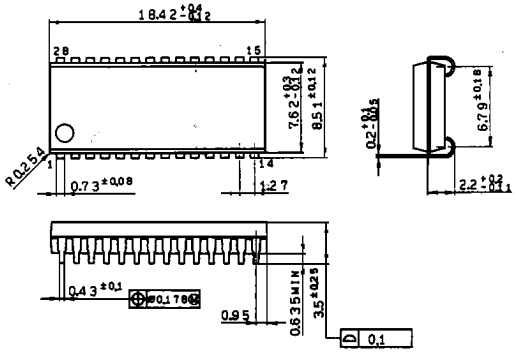
DIP-28P-06

CXK5863M 28 pin SOP (Plastic) 450mil 0.7g



SOP-28P-L05

CXK5863J 28 pin SOJ (Plastic) 300mil 0.8g



SOJ-28P-01

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