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INS1671 Asynchronous/Synchronous Transmitter/Receiver

General Description

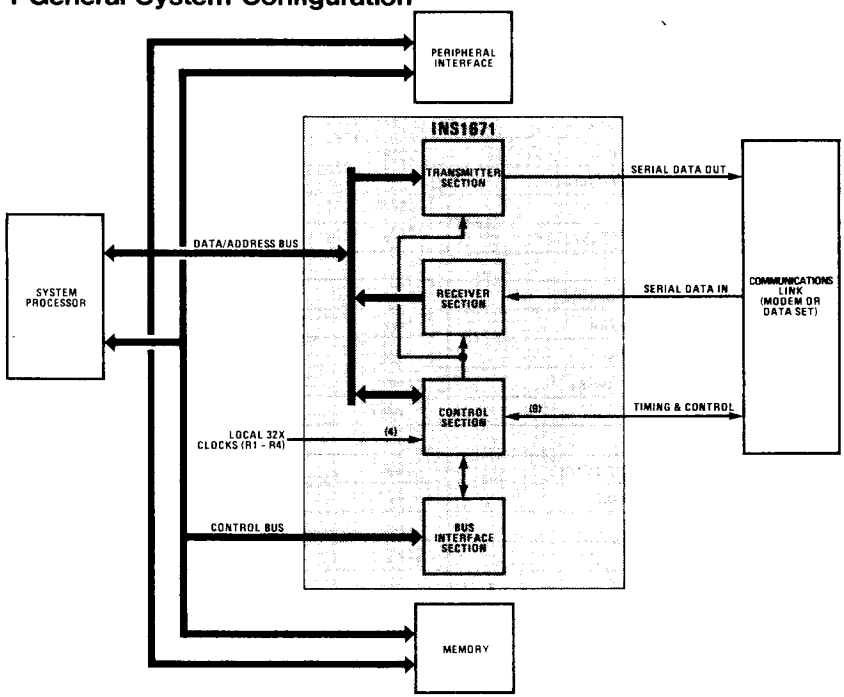
The INS1671 is a programmable Asynchronous/Synchronous Transmitter/Receiver (ASTRO) chip housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, provides a serial data input/output interface in a bus-structured system. The chip is capable of full duplex operation with synchronous or asynchronous data communications systems.

The INS1671 is designed to operate on a multiplexed, bidirectional bus with other bus-oriented devices. The functional configuration of the INS1671 is programmed by the system software via the bus and all parallel data transfers within the system are accomplished over the bus lines. In addition, the INS1671 contains a provision for hardwiring a unique 5-bit identification code to a chip, thereby allowing up to 32 INS1671 devices to be addressed via the multiplexed bus.

Features

- Synchronous and Asynchronous Full Duplex Operations
- Synchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Two Contiguous SYN Characters Provide Synchronization
  - Programmable SYN and DLE Characters Stripping
  - Programmable SYN and SYN-DLE Characters Insertion
- Asynchronous Mode Capabilities
  - Selectable 5- to 8-Bit Characters
  - Line Break Detection
  - 1-, 1½-, or 2-Stop Bit Detection
  - False Start Bit Detection
  - Automatic Serial Echo Mode
- DC to 1M Baud Rate
- 8 Selectable Clock Rates (4 Programmable)
- Transmission Error Detection Capabilities
  - Parity
  - Overrun
  - Framing
- Double Buffering of Data
- 8-Bit Bidirectional Bus for Data, Status, and Control Words
- All Inputs and Outputs TTL Compatible
- On-Line Diagnostic Mode
- Reduces System Component Count
- Direct Plug-In Replacement for Western Digital FD1671

INS1671 General System Configuration



Absolute Maximum Ratings

V_{DD} with Respect to V_{BB} (Ground) . . . . . +20 V to −0.3 V
Maximum Voltage to Any Input with Respect to V_{BB} . . . +20 V to −0.3 V
Operating Temperature. . . . . 0°C to +70°C
Storage Temperature . . . . . −55°C to +125°C
Power Dissipation . . . . . 1000 mW

Note: Maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under dc electrical characteristics.

DC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12.0 V ± 0.6 V, V_{BB} = −5.0 V ± 0.25 V, V_{SS} = 0 V, V_{CC} = +5 V ± 0.25 V

Symbol	Parameter	Unit	Min	Typ	Max	Conditions
I_{LI}	Input Leakage	μA			10	$V_{IN} = V_{DD}$
I_{LO}	Output Leakage	μA			10	$V_{OUT} = V_{DD}$
I_{BB}	V_{BB} Supply Current	mA			1	V_{BB} = −5 V
I_{CCAVE}	V_{CC} Supply Current	mA			80	
I_{DDAVE}	V_{DD} Supply Current	mA			10	
V_{IH}	Input High Voltage	V	2.4			
V_{IL}	Input Low Voltage (All Inputs)	V			0.8	
V_{OH}	Output High Voltage	V	2.8			I_O = −100 μA
V_{OL}	Output Low Voltage	V			0.4	I_O = 1.6 mA

AC Electrical Characteristics

T_A = 0°C to +70°C, V_{DD} = +12.0 V ± 0.6 V, V_{BB} = −5.0 V ± 0.25 V, V_{CC} = +5.0 V ± 0.25 V, V_{SS} = 0 V, C_{LMAX} = 20 pF

Symbol	Parameter	Unit	Min	Typ	Max	Conditions
t_{AS}	Address Setup Time	ns	0			
t_{AH}	Address Hold Time	ns	150			
t_{ARL}	Address to $\overline{RPLY}$ Delay	ns			400	
t_{CS}	$\overline{CS}$ Width	ns	250			
t_{CSRLF}	$\overline{CS}$ to Reply Off Delay	ns	0		250	R_L = 2.7 kΩ
READ CYCLE						
t_{ARE}	Address to $\overline{RE}$ Spacing	ns	250			
t_{RECSH}	$\overline{RE}$ and $\overline{CS}$ Overlap	ns	20			
t_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	ns	250			
t_{RED}	$\overline{RE}$ to Data Out Delay	ns			180	C_L = 20 pF
t_{RE}	$\overline{RE}$ Width	ns	200		1000	
WRITE CYCLE						
t_{AWE}	Address to $\overline{WE}$ Spacing	ns	250			
t_{WECSH}	$\overline{WE}$ and $\overline{CS}$ Overlap	ns	20			
t_{WE}	$\overline{WE}$ Width	ns	200		1000	
t_{DS}	Data Setup Time	ns	150			
t_{DH}	Data Hold Time	ns	100			
t_{WECS}	$\overline{WE}$ to $\overline{CS}$ Spacing	ns	250			

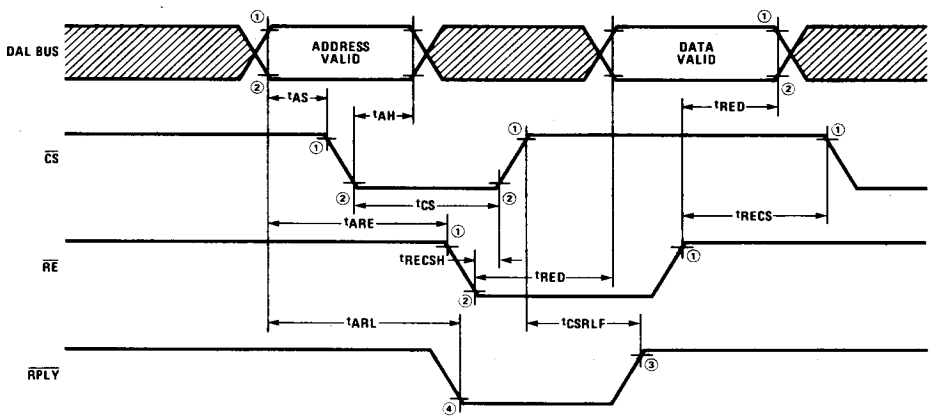
Interrupt

Symbol	Parameter	Unit	Min	Typ	Max	Conditions
t_{CSI}	$\overline{CS}$ to $\overline{IACKI}$ Delay	ns	0			
t_{CSRE}	$\overline{CS}$ to $\overline{RE}$ Delay	ns	250			
t_{CSREH}	$\overline{CS}$ and $\overline{RE}$ Overlap	ns	20			
t_{RECS}	$\overline{RE}$ to $\overline{CS}$ Spacing	ns	250			
t_{PI}	$\overline{IACKI}$ Pulse Width	ns	200			
t_{IAD}	$\overline{IACKI}$ to Valid ID Code Delay	ns			250	(Note 1)
t_{RED}	$\overline{RE}$ Off to $\overline{DAL}$ Open Delay	ns			180	
t_{IARL}	$\overline{IACKI}$ to $\overline{RPLY}$ Delay	ns			250	
t_{CSRLF}	$\overline{CS}$ to $\overline{RPLY}$ Off Delay	ns	0		250	$R_L = 2.7\,k\Omega$
t_{IAIH}	$\overline{IACKI}$ On to $\overline{INTR}$ Off Delay	ns			300	
t_{II}	$\overline{IACKI}$ to $\overline{IACKO}$ Delay	ns			200	
t_{REI}	$\overline{RE}$ Off to $\overline{IACKO}$ Off Delay	ns			250	

Note 1: If $\overline{RE}$ goes low after $\overline{IACKI}$ goes low, the delay will be from the falling edge of $\overline{RE}$.

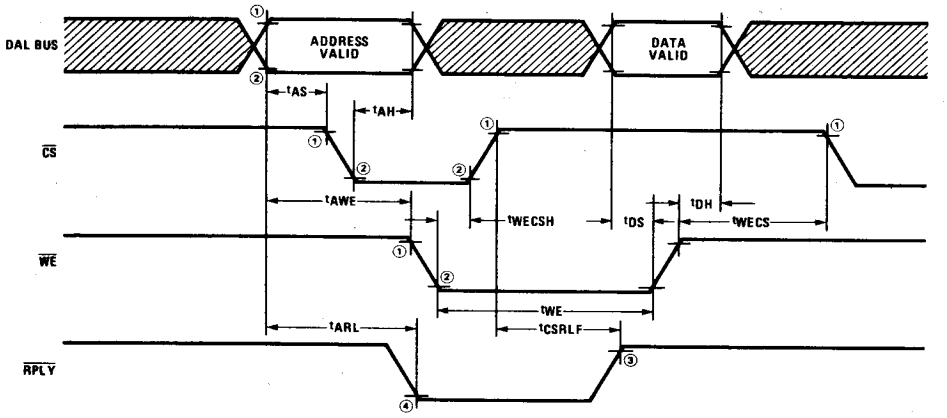
Timing Waveforms

① = V_{IH} (MIN) = 2.4 V
② = V_{IL} (MAX) = 0.8 V
③ = V_{OH} (MIN) = 2.8 V
④ = V_{OL} (MAX) = 0.4 V

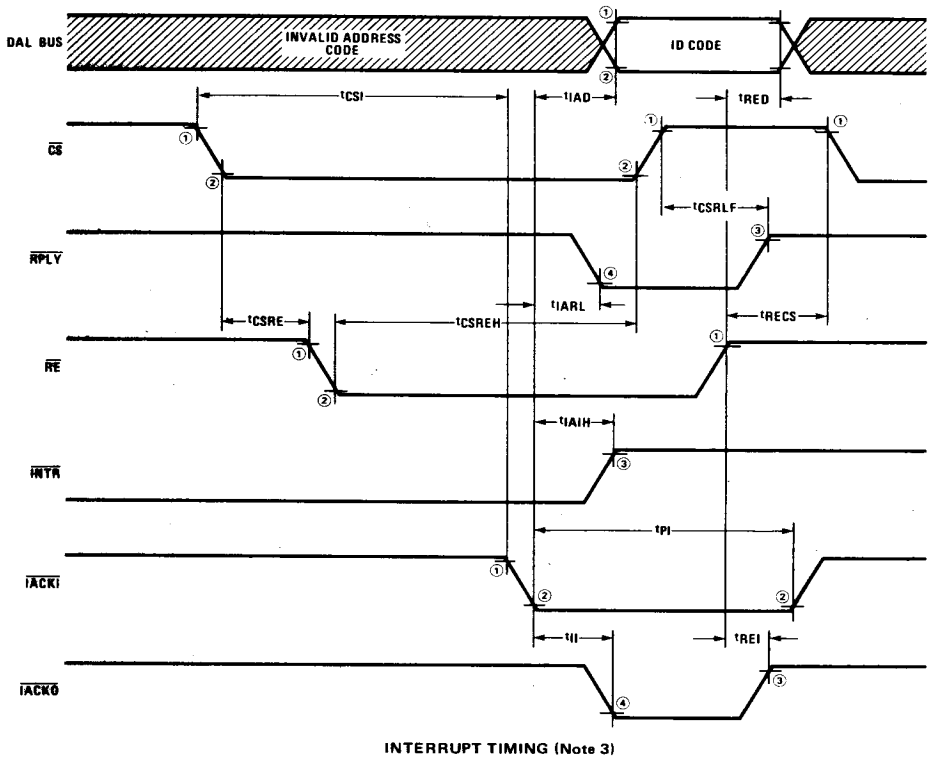


READ TIMING (Note 1)

Timing Waveforms (cont.)



WRITE TIMING (Notes 1 & 2)

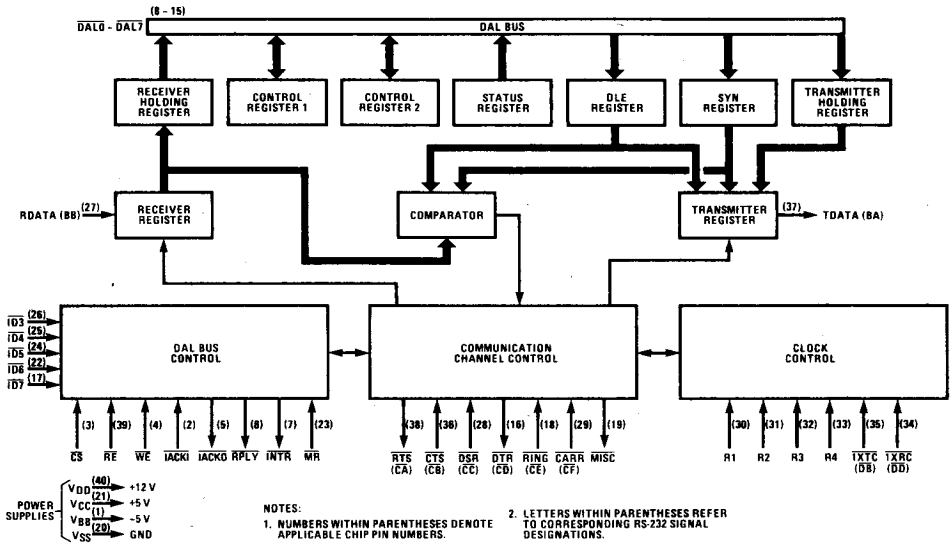


INTERRUPT TIMING (Note 3)

NOTES:

1. ID DECODE is the major factor in t_{ARE}, t_{AWE}, and t_{ARL} timing.
2. If changing Control Register 1 while processing data, the $\overline{WE}$ pulse width must be contained within the Data Valid envelope to insure correct data processing.
3. DAL0 must be a logic high coincident with an active $\overline{CS}$ to form an invalid address during Daisy Chain Interrupt Response.

INS1671 Functional Block Diagram



INS1671 Functional Pin Definitions

The following describes the function of all INS1671 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 and a high represents a logic 1 (refer to dc characteristics).

INPUT SIGNALS

Chip Select ($\overline{CS}$): When low, the chip is selected by a valid address on the DAL Bus. This enables communication between the INS1671 and the CPU (or controller).

Select Code ($\overline{ID7}$ - $\overline{ID3}$): Five input pins that are used for hardwiring a unique 5-bit identification code to the chip. The unique code is used to select the chip when addressing up to 32 INS1671 devices and to identify the chip when responding to interrupts.

Read Enable ($\overline{RE}$): When low coincident with an active $\overline{CS}$ input, allows the CPU (or controller) to read either of the following: data, control words, and status information from associated registers of the chip; or interrupt identification information. A Read operation is initiated by the controller when it places an 8-bit address on the Data Access Lines (DAL) Bus coincident with a low-level $\overline{CS}$ input. When bits 3 through 7 of the 8-bit address input match the unique 5-bit identification code of the chip, the device is selected. Bits 0 through 2 of the 8-bit address input are then used to select INS1671 registers to read from as indicated below.

A_2	A_2	A_0	Selected Register
0	0	0	Control Register 1
0	1	0	Control Register 2
1	0	0	Status Register
1	1	0	Receiver Holding Register

When the $\overline{RE}$ input is made active (low) by the controller, the INS1671 gates the contents of the addressed register onto the DAL Bus. When the $\overline{RE}$ and $\overline{CS}$ inputs are both returned to a high level, the Read operation is terminated and the chip is deselected.

Write Enable ($\overline{WE}$): When low coincident with an active $\overline{CS}$ input, allows the CPU (or controller) to write data or control words into associated registers of the chip. A Write operation is initiated by the controller as described above for a Read operation. However, bits 0 through 2 of the 8-bit address input are used to select INS1671 registers to be written into as indicated below.

A_2	A_1	A_0	Selected Register
0	0	0	Control Register 1
0	1	0	Control Register 2
1	0	0	SYN Register
1	0	0	DLE Register
1	1	0	Transmitter Holding Register

When the $\overline{WE}$ input is made active (low) by the controller, the INS1671 gates the data from the DAL Bus into the addressed register. As indicated in the above table, the same address (100) is used to write data into both the SYN and DLE registers. The INS1671 is set up so that data is written into the SYN Register and then into the DLE Register by a succeeding $\overline{WE}$ input with address 100. Any intervening Write or Read operation with a different register address causes the next address 100 input to select the SYN Register. When the $\overline{WE}$ and $\overline{CS}$ inputs are both returned to a high level, the Write operation is terminated and the chip is deselected.

Master Reset ($\overline{MR}$): When low, clears the Control Register, Status Register, and other controls of the chip.

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Interrupt Acknowledge In ($\overline{IACKI}$): Forced low by the CPU (or controller) when it is polling to determine which device is requesting an interrupt. When the device requesting the interrupt receives a low-level $\overline{IACKI}$ input coincident with a low-level $\overline{RE}$ input, the chip places its unique 5-bit identification code ($\overline{ID7}$ - $\overline{ID3}$) on the $\overline{DAL7}$ through $\overline{DAL3}$ lines, respectively, and a high (Receiver interrupt) or low (Transmitter interrupt) on the $\overline{DAL2}$ line of the DAL Bus. Also, at this time, the requesting device provides a low-level Reply ($\overline{RPLY}$) output and all other INS1671 devices receiving a low-level $\overline{IACKI}$ input force their Interrupt Acknowledge Output ($\overline{IACKO}$) signal to a low level. When the $\overline{RE}$ input returns to a high level, the interrupt identification information is removed from the DAL Bus.

Clock Rates (R1 - R4): Four input pins that accept four different local 32X baud rate clocks for the Transmitter and Receiver sections of the chip. The clock input at the R4 pin may be divided down into a 32X clock from either a 32X, 64X, 128X, or 256X clock input. The 32X clock is only used in the Asynchronous mode. Internal Control Register 2 selects the use of the local clocks.

Received Data (RDATA): Serial data input from the communications link (MODEM or data set).

Clear to Send ($\overline{CTS}$): When low, enables the Transmitter section of the chip to transmit serial data to a MODEM or data set.

Data Set Ready ($\overline{DSR}$): If low (On) or high (Off) when the internal Data Terminal Ready signal (bit 0 of Control Register 1) is high (On), generates an interrupt. The Data Set Ready input appears as bit 6 in the internal Status Register.

Ring Indicator ($\overline{RING}$): If low (On) when the internal Data Terminal Ready signal (bit 0 of Control Register 1) is low (Off), generates an interrupt.

Carrier Detector ($\overline{CARR}$): If low (On) or high (Off) when the internal Data Terminal Ready signal (bit 0 of Control Register 1) is high (On), generates an interrupt. The Carrier Detector input appears as bit 5 in the internal Status Register.

Transmitter Timing ($\overline{1XTC}$): This input is the 1X baud rate clock for the Transmitter section of the chip. The 1X clock is primarily used in the Synchronous mode. Internal Control Register 2 selects the use of the 1X clock. Transmitter data is clocked out of the INS1671 on the falling edge of this clock input.

Receiver Timing ($\overline{1XRC}$): This input is the 1X baud rate clock for the Receiver section of the chip. The 1X clock is primarily used in the Synchronous mode. Internal Control Register 2 selects the use of the 1X clock. Receiver data is clocked into the INS1671 on the rising edge of this clock input.

V_{BB}: -5-volt supply.

V_{CC}: +5-volt supply.

V_{DD}: +12-volt supply.

V_{SS}: Ground (0-volt) reference.

OUTPUT SIGNALS

Interrupt ($\overline{INTR}$): Open-drain output that goes low when any one of the communication interrupt conditions indicated below occurs.

1. Data Received (Receiver Holding Register Full)
2. Transmitter Holding Register Empty
3. Carrier Detector On ($\overline{CARR}$ input low)
4. Carrier Detector Off ($\overline{CARR}$ input high)
5. Data Set Ready On ($\overline{DSR}$ input low)
6. Data Set Ready Off ($\overline{DSR}$ input high)
7. Ring Indicator On ($\overline{RING}$ input low)

Interrupt Acknowledge Out ($\overline{IACKO}$): Goes low in response to a low-level $\overline{IACKI}$ input, when the chip is not the interrupting device. (The $\overline{IACKO}$ output is mutually exclusive with the $\overline{RPLY}$ output.)

Reply ($\overline{RPLY}$): Open-drain output that goes low when the chip is selected by a valid address on the DAL Bus or when the chip identifies itself as the interrupting device during interrupt polling.

Transmitted Data (TDATA): Composite serial data output to a MODEM or data set. This output is held in the Marking state (logic 1) when the Transmitter section of the chip is disabled.

Data Terminal Ready ($\overline{DTR}$): Set low when the CPU (or controller) is ready to communicate with a MODEM or data set. This output is generated by bit 0 of Control Register 1.

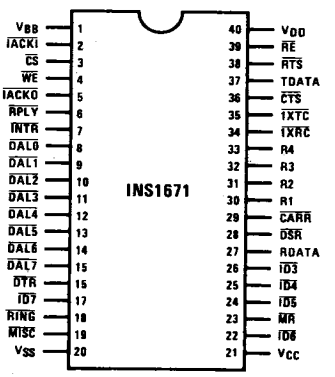
Request to Send ($\overline{RTS}$): Set low when the CPU (or controller) is ready to transmit data to a MODEM or data set. This output is enabled by bit 1 of Control Register 1.

Miscellaneous ($\overline{MISC}$): User-designated, programmable low-level output. This output is controlled by bit 4 of Control Register 1.

INPUT/OUTPUT SIGNALS

Data Access Lines (DAL) Bus: This bus comprises eight input/output lines ($\overline{DAL0}$ - $\overline{DAL7}$). The bus provides bidirectional communications between the CPU (or controller) and the INS1671. Data, control words, status information and address information are transferred via the DAL Bus.

Pin Configuration



INS1671 Programming

The system software determines the operative conditions (mode selection, clock selection, interface signal control, data format, *et cetera*) of the INS1671 via internal Control Registers 1 and 2. Each of these 8-bit registers can be loaded from the DAL Bus by a Write Operation or read into the DAL Bus by a Read Operation. The contents of Control Register 1 can be changed at any time, while the contents of Control Register 2 (usually loaded first) should be changed only when the Receiver and Transmitter sections of the chip are both in the idle mode. The contents of the two control registers are shown in figures 1 and 2 and are described below.

CONTROL REGISTER 1 (CR1) CONTENTS

Bit 0: Controls the generation of the Data Terminal Ready ($\overline{DTR}$) output. When high (logic 1), enables the Carrier Detector and Data Set Ready interrupts. When low (logic 0), enables only the Ring Indicator On interrupt.

Bit 1: Controls the enabling of the Request to Send ($\overline{RTS}$) output. When high in coincidence with a low-level Clear to Send ($\overline{CTS}$) input, enables the Transmitter section of the chip and allows the generation of Transmitter Holding Register Empty (THRE) interrupts. When low, disables the Transmitter section and disables the Request to Send ($\overline{RTS}$) output. Before the Transmitter section is disabled, any character in the Transmitter Register is completely transferred to the MODEM or data set.

Bit 2: When high, enables the INS1671 to perform the following: (1) transfer a new character into the Receiver Holding Register; (2) update Receiver status bits 1 through 4; and (3) generate Data Received interrupts. When low, disables the Receiver section and clears Receiver status bits 1 through 4.

Bit 3: When high while in the Asynchronous mode, enables a parity check on each received character and the generation of a parity bit for each transmitted character. When high while in the Synchronous mode, enables a parity check on each received character.

Bit 4: When high while the Receiver section is enabled (bit 2 of Control Register 1 is high) and in the Asynchronous mode, causes the INS1671 to enter the Echo mode. In this mode, the Transmitted Data (TDATA) output is obtained directly from the clocked regenerated data (assembled received characters) instead of the transmission characters from the Transmitter Register. Echoing does not start until a character has been received and the Transmitter section is idle. The Transmitter section does not have to be enabled in the Echo mode.

NOTE

Only the first character of a break condition of all zeros (null character) is echoed when a Line Break condition is detected. For all subsequent null characters with low-level Stop bits, a steady Marking (high) condition is transmitted until normal character reception is resumed.

When high while the Receiver section is enabled and in the Synchronous mode, causes stripping of received characters that match the contents of the DLE Register. In addition, parity checking is disabled at this time.

When high while the Receiver section is disabled and in the Synchronous mode, causes the generation of a low-level Miscellaneous ($\overline{MISC}$) output from the chip. (This output may be used as a New Sync signal on a Model 201 Data Set.) With a 32X clock selected, a high-level bit 4 causes the Receiver bit timing to be synchronized on Mark-Space (high-low) transitions.

Bit 5: When high while the Transmitter section is enabled and in the Asynchronous mode, causes a single Stop bit to be transmitted.

When low while the Transmitter section is enabled and in the Asynchronous mode, causes 2 Stop bits to be transmitted for character lengths of 6, 7, or 8 bits and 1½ Stop bits for a character length of 5 bits.

When high while the Transmitter section is disabled and in the Asynchronous mode, causes the generation of a low-level Miscellaneous ($\overline{MISC}$) output from the chip. (This output may be used for a Make Busy signal on a Model 103 Data Set, a Secondary Transmit signal on a Model 202 Data Set, and a Dialing Signal on a CBS Data Coupler.)

When high in coincidence with a high-level bit 6 while in the Synchronous mode, causes the contents of the DLE Register to be transmitted before the loading of the next character in the Transmitter Holding Register, as part of the Transmit Transparent mode.

When high in coincidence with a low-level bit 6 of Control Register 1 while in the Synchronous mode, enables transmit parity. If bit 6 is high or bit 5 is low, no parity is generated.

Bit 6: When high while the Transmitter section is enabled and in the Asynchronous mode, holds the Transmitted Data (TDATA) output of the chip in a Spacing (low) condition, starting at the end of any current transmitted character. In this case, normal transmitter timing continues so that the Transmission Break condition is timed out after the loading of new characters in the Transmitter Holding Register.

When high while in the Synchronous mode, conditions the Transmitter section to the Transmit Transparent mode, which implies that the idle Transmitter time will be filled by DLE-SYN character transmission and that a DLE can be forced ahead of any character in the Transmitter Holding Register by setting bit 5 of Control Register 1 high, prior to loading the THR.

Bit 7: When low, the INS1671 is configured to provide an internal data and control loop (On-line Diagnostic mode), and the Ring Indicator On interrupt is disabled. When high, the chip is in the normal full duplex configuration and the Ring Indicator On interrupt is enabled.

In the On-line Diagnostic mode, the following occur (via internal logic):

1. The TDATA output (pin 37) is connected to the RDATA input (pin 27). The TDATA output is held in the Marking (high) condition and the RDATA input from the MODEM or data set is disregarded.
2. The Transmitter clock is also used as the Receiver clock, when the 1X clock is selected by bits 0 - 2 of Control Register 1.
3. Bit 0 (Data Terminal Ready) of Control Register 1 is connected to the $\overline{DSR}$ input (pin 28). The $\overline{DTR}$ output (pin 16) is held in the Off (high) condition and the $\overline{DSR}$ input from the MODEM or data set is disregarded.
4. Bit 1 (Request to Send) of Control Register 1 is connected to both the $\overline{CTS}$ input (pin 36)

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and the $\overline{CARR}$ input (pin 29). The $\overline{RTS}$ output (pin 38) is held in the Off (high) condition and the $\overline{CTS}$ and $\overline{CARR}$ inputs from the MODEM or data set are disregarded.

5. The $\overline{MISC}$ output (pin 19) is held in the Off (high) condition.

CONTROL REGISTER 2 (CR2) CONTENTS

Bits 0-2: Select clocks for Receiver and Transmitter secitions of the chip as indicated below.

B_2	B_1	B_0	Clock Selected
0	0	0	1XTC and 1XRC inputs for Transmitter and Receiver sections, respectively
0	0	1	R1 (32X) input
0	1	0	R2 (32X) input
0	1	1	R3 (32X) input
1	0	0	R4 (32X) input
1.	0	1	R4 (64X) input ÷2
1	1	0	R4 (128X) input ÷4
1	1	1	R4 (256X) input ÷8

Bit 3: When low while in the Asynchronous mode, selects the R1 (32X) clock input for the Receiver section of the chip. When high, selects the same 32X clock rate for the Receiver section as selected for the Transmitter section.

NOTE

Bit 3 must be high (logic 1) for the 1X clock selection by bits 0-2 of Control Register 2.

When high while in the Synchronous mode, causes stripping of all DLE and SYN characters in the Transmit Transparent mode (selected by bit 6 of Control Register 1) or of all SYN characters in the Transmit Non-Transparent mode. In addition, no Data Received interrupt is generated and the SYN Detect status bit is set high with the reception of the next assembled character.

Bit 4: When high while parity is enabled (bit 3 and/or bit 5 of Control Register 1 are high), selects Odd parity. When low while parity is enabled, selects Even parity.

Bit 5: When high, selects the Synchronous mode for the INS1671. When low, selects the Asynchronous mode for the chip.

Bits 6 and 7: Select the character length as indicated below.

B_7	B_6	Character Length
0	0	8 bits
0	1	7 bits
1	0	6 bits
1	1	5 bits

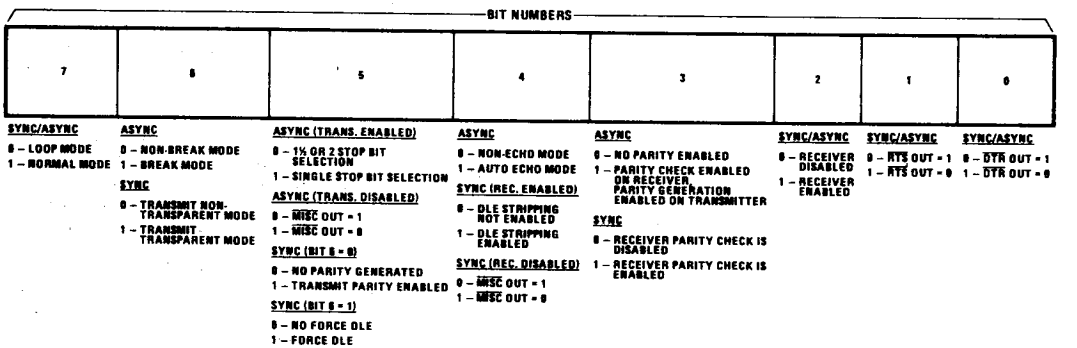


Figure 1. Control Register 1 Contents

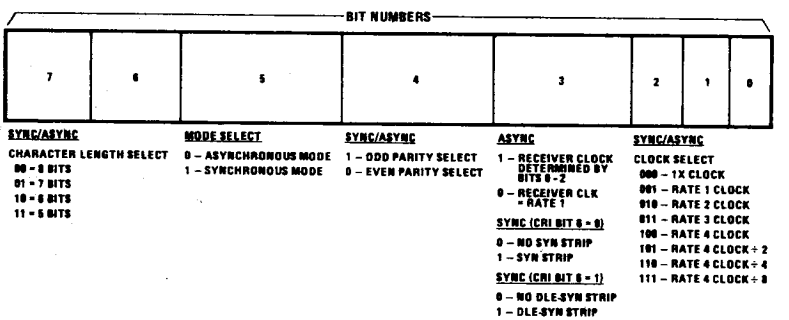


Figure 2. Control Register 2 Contents

INS1671 Status Register

The Status Register of the INS1671 holds information that defines data conditions of the Receiver and Transmitter sections of the chip, and the status of the MODEM or data set. This 8-bit register can be read onto the DAL Bus by a Read operation. The contents of the Status Register are shown in figure 3 and are described below.

Bit 0: When high, indicates that no character is contained in the Transmitter Holding Register while the Transmitter section is enabled. Bit 0 is set high when the contents of the Transmitter Holding Register are transferred to the Transmitter Register. Bit 0 is reset low when the Transmitter Holding Register is loaded from the DAL Bus or when the Transmitter section is disabled by forcing the $\overline{CTS}$ input to a high level.

Bit 1: When high, indicates that the Receiver Holding Register has been loaded from the Receiver Register while the Receiver section is enabled. Bit 1 is reset low when the Receiver Holding Register is read onto the DAL Bus or when the Receiver Section is disabled by forcing bit 2 of Control Register 1 to a low level.

Bit 2: When high, indicates an overrun error that occurs if the previous character in the Receiver Holding Register has not been read onto the DAL Bus and Data Received status bit 0 has not been reset low, at the time a new character is to be transferred to the Receiver Holding Register. Bit 2 is reset low when no overrun error is detected or when the Receiver section is disabled.

Bit 3: When high while DLE stripping is enabled (bit 4 of Control Register 1 is high) and the Receiver section is enabled, indicates that the character previous to the presently assembled character matched the contents of the DLE Register. Bit 3 is reset low when a no match condition exists between the previous character and the contents of the DLE Register.

When high while DLE stripping is disabled, parity checking is enabled (bit 3 of Control Register 1 is high) and the Receiver section is enabled, indicates that the last received character has a parity error. Bit 3 is reset low when a correct parity condition exists.

NOTE

Bit 3 is reset low during DLE stripping or parity error checking when the Receiver section is disabled.

Bit 4: When high while in the Asynchronous mode, indicates that the Received Data (RDATA) input contains a low-level Stop bit after the last bit of the character (framing error), while the Receiver section is enabled. Bit 4 is reset low when the proper high-level Stop bit is detected.

When high while in the Synchronous mode, indicates that the contents of the Receiver Register matched the contents of the SYN Register, while the Receiver section is enabled. Bit 4 remains high for the duration of a full character assembly.

NOTE

Bit 4 is reset low in both modes when the Receiver section is disabled.

Bit 5: Complement of the active low-level Carrier Detector ($\overline{CARR}$) input.

Bit 6: Complement of the active low-level Data Set Ready ($\overline{DSR}$) input. Bit 6 may be used for a Secondary Receive signal on type 202 data sets.

Bit 7: When high, indicates that there is a change in the state of the Data Set Ready ($\overline{DSR}$) or Carrier Detector ($\overline{CARR}$) input to the INS1671, while the internal Data Terminal Ready signal (bit 0 of Control Register 1) is high (On); or that the Ring Indicator ($\overline{RING}$) input is low (On) while the internal Data Terminal Ready signal (bit 0 of Control Register 1) is low (Off). Bit 7 is reset low when the contents of the Status Register are read onto the DAL Bus.

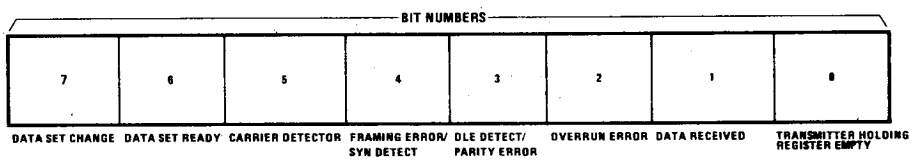


Figure 3. Status Register Contents

D.4

INS1671 Operation

The following describes the operation of the INS1671 chip. Use the functional block diagram on page 5 as necessary to follow these descriptions.

ASYNCHRONOUS MODE

Framing of asynchronous characters is provided by a low-level (logic 0) Start bit at the beginning of a character and a high-level (logic 1) Stop bit at the end of a character. Reception of a character is initiated on recognition of the first Start bit after a preceding Stop bit by a positive transition of the receiver clock. The Start and Stop bits are stripped off while assembling the serial input into a parallel character.

The character assembly is completed by the reception of the Stop bit after reception of the last character bit. If this bit is high, the character is determined to have correct framing and the INS1671 is prepared to receive the next character. If the Stop bit is low, the Framing Error flag (bit 4 of Status Register) is set and the Receiver section assumes this bit to be the Start bit of the next character. Character assembly continues from this point if the input is still low, when sampled at the theoretical center of the assumed Start bit. As long as the Receiver input is a Spacing (low) condition, all zero characters are assembled and error flags and Data Received interrupts are generated so that Line Break conditions can be detected. After a character of all zeroes is assembled along with a zero in the Stop bit location, the first received Marking (high) condition is determined as a Stop bit and this resets the Receiver section to a Ready state for assembly of the next character.

In the Asynchronous mode, the character transmission occurs when information contained in the Transmitter Holding Register is transferred to the Transmitter Register. Transmission is initiated by the insertion of a Start bit, followed by the serial output of the character least significant bit first with parity (if enabled) following the most significant bit; then the insertion of a 1-, 1½-, or 2-bit length Stop condition. If the Transmitter Holding Register is full, the next character transmission starts after the transmission of the Stop bit of the present character in the Transmitter Register. Otherwise, the Marking condition is continuously transmitted until the Transmitter Holding Register is loaded.

In order to allow re-transmission of data received at a slightly faster character rate, means are provided for shortening the Stop bit length to allow transmission of characters to occur at the same rate as the reception of characters. The Stop bit is shortened by 1/16 of a bit period for 1-Stop bit selection and 3/16 of a bit period for 1½- or 2-Stop bit selection, if the next character is ready in the Transmitter Holding Register.

SYNCHRONOUS MODE

Framing of characters is carried out by a special Synchronization (SYN) Character Code transmitted at the beginning of a block of characters. When the Receiver section is enabled, it searches for two continuous characters matching the bit pattern contained in the SYN Register. During the time the Receiver section is searching, data is not transferred to the Receiver Holding Register, status bits are not updated, and the Receiver interrupt is not activated. After the detection of the first SYN character, the Receiver section assembles subsequent bits into characters whose length is determined by the contents of Control Register 2. If, after the first SYN character detection, a second SYN character is present, the Receiver section enters the synchronized state until the Receiver Enable Bit (bit 2 of Control Register 1) is turned Off. If a second successive SYN character is not detected, the Receiver reverts to the Search mode.

In the Synchronous mode, a continuous stream of characters is transmitted once the Transmitter section is enabled. If the Transmitter Holding Register is not loaded at the time the Transmitter Register has completed transmission of a character, this idle time will be filled by a transmission of the character contained in the SYN register in the Transmit Non-Transparent mode, or the characters contained in the DLE and SYN registers respectively while in the Transmit Transparent mode of operation.

DETAILED OPERATION

Receiver Section: The data input to the Receiver section is clocked into the Receiver Register by a 1X Receiver clock from a MODEM or data set, or by a local 32X bit rate clock selected from one of four externally supplied clock inputs. When using the 1X clock, the Received Data (RDATA) input is sampled on the positive transition of the clock in both the Asynchronous and Synchronous modes. When using a 32X clock in the Asynchronous mode, the Receiver sampling clock is phased to the Mark-To-Space transition of the Start bit of the data input and defines, through clock counts, the center of each received data bit within +0%, −3% at the positive transition 16 clock periods later.

In the Synchronous mode, the Receiver sampling clock is phased to all Mark-To-Space transitions of the data inputs when using a 32X clock. Each transition of the data causes an incremental correction of the sampling clock by 1/32 of a bit period. The sampling clock can be immediately phased to every Mark-To-Space data transition by setting bit 4 of Control Register 1 high, while the Receiver section is disabled.

When the complete character has been shifted into the Receiver Register, it is then transferred to the Receiver Holding Register; the unused, higher number bits are filled with zeroes. At this time, the Receiver status bits (Framing Error/SYN Detect, Parity Error/DLE Detect, Overrun Error, and Data Received) are updated in the Status Register and the Data Received interrupt is activated. Parity Error is set, if encountered while the Receiver parity check is enabled in Control Register 1. The Overrun Error flag (bit 2 of Status Register) is set if the Data Received status bit (bit 1) is not cleared through a Read operation by an external device, when a new character is ready to be transferred to the Receiver Holding Register. This error flag indicates that a character has been lost, as new data is lost and the old data and its status flags are saved.

The characters assembled in the Receiver Register that match the contents of the SYN or DLE Register are not

loaded into the Receiver Holding Register, and the Data Received interrupt is not generated, if bit 3 (SYN Strip) of Control Register 2 or bit 4 (DLE Strip) of Control Register 1 are set respectively; the SYN-DET and DLE-DET status bits are set with the next non-SYN or non-DLE character. When both the SYN Strip and DLE Strip bits are set (Transmit Transparent mode), the DLE-SYN combination is stripped. The SYN comparison occurs only with the character received after the DLE character. If two successive DLE characters are received, only the first DLE character is stripped. No parity check is made while in this mode.

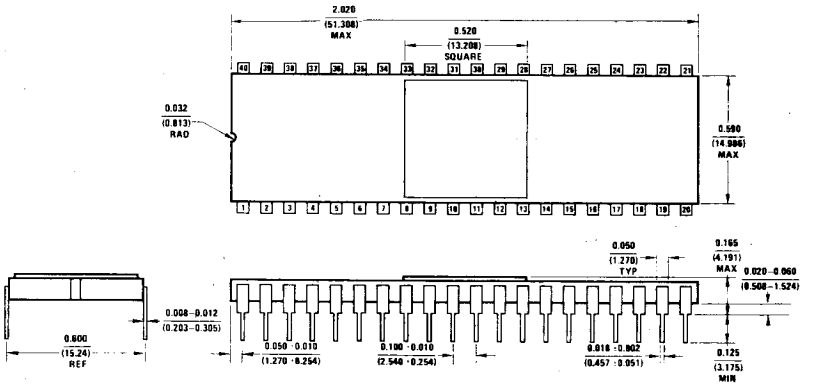
Transmitter Section: Information is transferred to the Transmitter Holding Register by a Write operation. Information can be loaded into this register at any time, even when the Transmitter section is not enabled. Transmission of data is initiated only when the Request to Send ($\overline{RTS}$) bit (bit 1 of Control Register 1) is set high and the Clear to Send ($\overline{CTS}$) input is low. Information is normally transferred from the Transmitter Holding Register to the Transmitter Register when the latter has completed transmission of a character. However, information in the DLE Register may be transferred prior to the information contained in the Transmitter Holding Register if the Force DLE signal condition is enabled (bits 5 and 6 of Control Register 1 set high). The Force DLE control bit (bit 5 of Control Register 1) must be set prior to loading of a new character in the Transmitter Holding Register to ensure forcing the DLE character prior to transmission of the data character. The Transmitter Register output is applied to a flip-flop which delays the output by one clock period. When using the 1X clock generated by the MODEM or data set, the output data changes state on the negative clock transition and the delay is one bit period. When using a local 32X clock, the Transmitter section selects one of the four selected rate inputs and divides the clock down to the baud rate. This clock is phased to the Transmitter Holding Register Empty flag (bit 0 of Status Register) such that transmission of characters occurs within two clock times of the loading of the Transmitter Holding Register, when the Transmitter Register is empty.

When the Transmitter section is enabled, a Transmitter interrupt is generated each time the Transmitter Holding Register is empty. If the Transmitter Holding Register is empty when the Transmitter Register is ready for a new character, the Transmitter section enters an idle state. During this idle time, a high will be presented to the Transmitted Data (TDATA) output in the Anynchronous mode or the contents of the SYN Register will be presented in the Synchronous Transmit Non-Transparent mode. In the Synchronous Transmit Transparent mode (enabled by a high-level bit 6 of Control Register 1), the idle state will be filled by a DLE-SYN character transmission in that order. When entering the Transmit Transparent mode, the DLE-SYN fill will not occur until the first forced DLE.

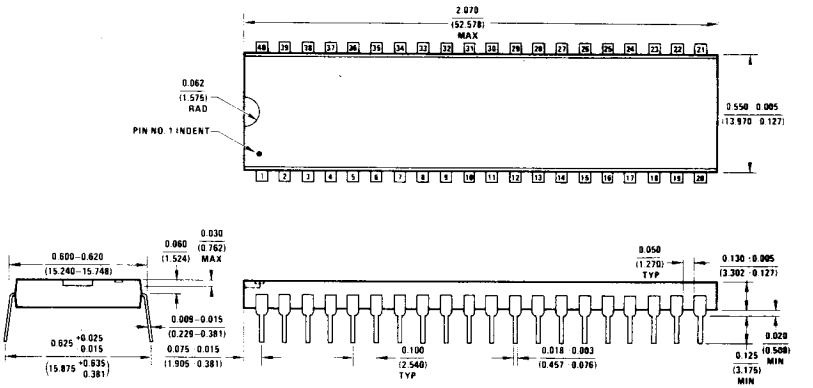
If the Transmitter section is disabled by a reset of the Request to Send control bit, any partially transmitted character is completed before the Transmitter section of the INS1671 is disabled. As soon as the Clear to Send ($\overline{CTS}$) input goes high, the Transmitted Data output will go high.

When the Transmit parity is enabled, the selected Odd or Even parity bit is inserted into the last bit of the character in place of the last bit of the Transmitter Register. This limits transfer of character information to a maximum of seven bits plus parity or eight bits without parity. Parity cannot be enabled in the Synchronous Transmit Transparent mode.

Physical Dimensions



Ceramic Dual-In-Line Package (D)
Order Number INS1671D



Plastic Dual-In-Line Package (N)
Order Number INS1671N

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693248

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