

## Linear Systems Ultra Low Leakage Low Drift Monolithic Dual JFET

The LS840 is a high-performance monolithic dual JFET featuring extremely low noise, tight offset voltage and low drift over temperature specifications, and is targeted for use in a wide range of precision instrumentation applications. The LS840 features a 5-mV offset and 5- $\mu\text{V}/^\circ\text{C}$  drift.

The 8 Pin P-DIP and 8 Pin SOIC provide ease of manufacturing, and the symmetrical pinout prevents improper orientation.

(See Packaging Information).

### LS840 Applications:

- Wideband Differential Amps
- High-Speed, Temp-Compensated Single-Ended Input Amps
- High-Speed Comparators
- Impedance Converters and vibrations detectors.

### FEATURES

LOW DRIFT	$ V_{GS1-2}/T  \leq 5\mu\text{V}/^\circ\text{C}$	
LOW LEAKAGE	$I_G = 10\text{pA TYP.}$	
LOW NOISE	$e_n = 8\text{nV}/\sqrt{\text{Hz}} \text{ TYP.}$	
LOW OFFSET VOLTAGE	$ V_{GS1-2}  = 2\text{mV TYP.}$	
<b>ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)</b>		
<b>Maximum Temperatures</b>		
Storage Temperature	-65°C to +150°C	
Operating Junction Temperature	+150°C	
<b>Maximum Voltage and Current for Each Transistor – Note 1</b>		
-V <sub>GSS</sub>	Gate Voltage to Drain or Source	60V
-V <sub>DSO</sub>	Drain to Source Voltage	60V
-I <sub>G(f)</sub>	Gate Forward Current	50mA
<b>Maximum Power Dissipation</b>		
Device Dissipation @ Free Air – Total	400mW @ +125°C	

### MATCHING CHARACTERISTICS @ 25°C UNLESS OTHERWISE NOTED

SYMBOL	CHARACTERISTICS	VALUE	UNITS	CONDITIONS
$ V_{GS1-2}/T  \text{ max.}$	DRIFT VS. TEMPERATURE	5	$\mu\text{V}/^\circ\text{C}$	$V_{DG}=20\text{V}, I_D=200\mu\text{A}$ $T_A=-55^\circ\text{C to }+125^\circ\text{C}$
$ V_{GS1-2}  \text{ max.}$	OFFSET VOLTAGE	5	mV	$V_{DG}=20\text{V}, I_D=200\mu\text{A}$

### ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN.	TYP.	MAX.	UNITS	CONDITIONS
BV <sub>GSS</sub>	Breakdown Voltage	60	60	--	V	$V_{DS} = 0$ $I_D=1\text{nA}$
BV <sub>GGO</sub>	Gate-To-Gate Breakdown	60	--	--	V	$I_G = 1\text{nA}$ $I_D = 0$ $I_S = 0$
<b>TRANSCONDUCTANCE</b>						
Y <sub>FSS</sub>	Full Conduction	1000	--	4000	$\mu\text{mho}$	$V_{DG}=20\text{V}$ $V_{GS}=0\text{V}$ $f=1\text{kHz}$
Y <sub>FS</sub>	Typical Operation	500	--	1000	$\mu\text{mho}$	$V_{DG}=20\text{V}$ $I_D=200\mu\text{A}$
$ Y_{FS1-2}/Y_{FS} $	Mismatch	--	0.6	3	%	
<b>DRAIN CURRENT</b>						
I <sub>DSS</sub>	Full Conduction	0.5	2	5	mA	$V_{DG}=20\text{V}$ $V_{GS}=0\text{V}$
$ I_{DSS1-2}/I_{DSS} $	Mismatch at Full Conduction	--	1	5	%	
<b>GATE VOLTAGE</b>						
V <sub>GS(off)</sub> or V <sub>p</sub>	Pinchoff voltage	1	2	4.5	V	$V_{DS}=20\text{V}$ $I_D=1\text{nA}$
V <sub>GS(on)</sub>	Operating Range	0.5	--	4	V	$V_{DS}=20\text{V}$ $I_D=200\mu\text{A}$
<b>GATE CURRENT</b>						
-I <sub>Gmax.</sub>	Operating	--	10	50	pA	$V_{DG}=20\text{V}$ $I_D=200\mu\text{A}$
-I <sub>Gmax.</sub>	High Temperature	--	--	50	nA	$T_A = +125^\circ\text{C}$
-I <sub>Gmax.</sub>	Reduced V <sub>DG</sub>	--	5	--	pA	$V_{DG}=10\text{V}$ $I_D=200\mu\text{A}$
-I <sub>GSSmax.</sub>	At Full Conduction	--	--	100	pA	$V_{DG}=20\text{V}, V_{DS}=0$
<b>OUTPUT CONDUCTANCE</b>						
Y <sub>OSS</sub>	Full Conduction	--	--	10	$\mu\text{mho}$	$V_{DG}=20\text{V}$ $V_{GS}=0\text{V}$
Y <sub>OS</sub>	Operating	--	0.1	1	$\mu\text{mho}$	$V_{DG}=20\text{V}$ $I_D=200\mu\text{A}$
$ Y_{OS1-2} $	Differential	--	0.01	0.1	$\mu\text{mho}$	
<b>COMMON MODE REJECTION</b>						
CMR	$-20 \log  V_{GS1-2}/V_{DS} $	--	100	--	dB	$\Delta V_{DS} = 10 \text{ to } 20\text{V}$ $I_D=200\mu\text{A}$
	$-20 \log  V_{GS1-2}/V_{DS} $	--	75	--	dB	$\Delta V_{DS} = 5 \text{ to } 10\text{V}$ $I_D=200\mu\text{A}$
<b>NOISE</b>						
NF	Figure	--	--	0.5	dB	$V_{DS}=20\text{V}$ $V_{GS}=0\text{V}$ $R_G=10\text{M}\Omega$ $f=100\text{Hz}$ $\text{NBW}=6\text{Hz}$
e <sub>n</sub>	Voltage	--	--	10	nV/ $\sqrt{\text{Hz}}$	$V_{DS}=20\text{V}$ $I_D=200\mu\text{A}$ $f=1\text{kHz}$ $\text{NBW}=1\text{Hz}$
		--	--	15		$V_{DS}=20\text{V}$ $I_D=200\mu\text{A}$ $f=10\text{Hz}$ $\text{NBW}=1\text{Hz}$
<b>CAPACITANCE</b>						
C <sub>ISS</sub>	Input	--	4	10	pF	$V_{DS}=20\text{V}, I_D=200\mu\text{A}$
C <sub>RSS</sub>	Reverse Transfer	--	1.2	5		
C <sub>DD</sub>	Drain-to-Drain	--	0.1	--		

Note 1 – These ratings are limiting values above which the serviceability of any semiconductor may be impaired

### Available Packages:

LS840 / LS840 in PDIP & SOIC  
LS840 / LS840 available as bare die  
Please contact [Micross](http://www.micross.com) for full package and die dimensions

### PDIP & SOIC (Top View)

