

## Section 9 Electrical Characteristics

### 9.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Power supply voltage	$V_{CC}$	-0.3 to +7.0	V
Input voltage	$V_i$	-0.3 to $V_{CC} + 0.3$	V
Operating temperature	$T_{opr}$	0 to +70	°C
Storage temperature	$T_{stg}$	-55 to +150	°C
Power dissipation	$P_d$	3.0	W

$V_{SS} = 0V$

### 9.2 Recommended Operating Conditions

Item	Symbol	Pin	Standard			Unit
			Min.	Typ.	Max.	
Power supply voltage	$V_{CC}$		4.75	5.00	5.25	V
High-level input voltage	$V_{IH}$	Other than CLK	2.2	—	$V_{CC} + 0.3$	V
		CLK	$0.8 \cdot V_{CC}$	—	$V_{CC} + 0.3$	V
Low-level input voltage	$V_{IL}$	Other than CLK	-0.3	—	0.8	V
		CLK	-0.3	—	$0.2 \cdot V_{CC}$	V
Operating temperature	$T_{opr}$		0	25	70	°C

$V_{SS} = 0V$

## 9.3 Electrical Characteristics

### 9.3.1 DC Characteristics

$V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $70^\circ C$

Item	Symbol	Pin	Measuring Condition	Standard Value		Unit
				Min.	Max.	
High-level input voltage	$V_{IH}$	Other than CLK		2.2	$V_{CC} + 0.3$	V
		CLK		$0.8 \cdot V_{CC}$	$V_{CC} + 0.3$	V
Low-level input voltage	$V_{IL}$	Other than CLK		-0.3	0.8	V
		CLK		-0.3	$0.2 \cdot V_{CC}$	V
High-level output voltage	$V_{OH}$	Other than $\overline{DONE}$ , $\overline{IRQ}$ and $\overline{XIRQ}$	$I_{OH} = -400 \mu A$	2.4	—	V
Low-level output voltage	$V_{OL}$	$\overline{DONE}$ , $\overline{IRQ}$ and $\overline{XIRQ}$	$I_{OL} = 3.2 \text{ mA}$	—	0.5	V
		$\overline{DONE}$ , $\overline{IRQ}$ and $\overline{XIRQ}$	$I_{OL} = 6.4 \text{ mA}$	—	0.5	V
Input leak current	$I_{LI}$		$V_I = 0$ to $V_{CC}$	-10	10	$\mu A$
Output leak current	$I_{LO}$	Tristate Output pin	$V_I = 0$ to $V_{CC}$ tristate	-10	10	$\mu A$
		$\overline{DONE}$ , $\overline{IRQ}$ and $\overline{XIRQ}$	$V_I = 0$ to $V_{CC}$ open drain off	-10	10	$\mu A$
Input capacitance	$C_i$		$f = 1 \text{ MHz}$	—	20	pF
Output capacitance	$C_o$		$f = 1 \text{ MHz}$	—	20	pF
I/O capacitance	$C_{I/O}$		$f = 1 \text{ MHz}$	—	20	pF
Power dissipation	$P_d$		$f = 20 \text{ MHz}$ , no load (operating frequency)	—	1.2	W

### 9.3.2 AC Characteristics

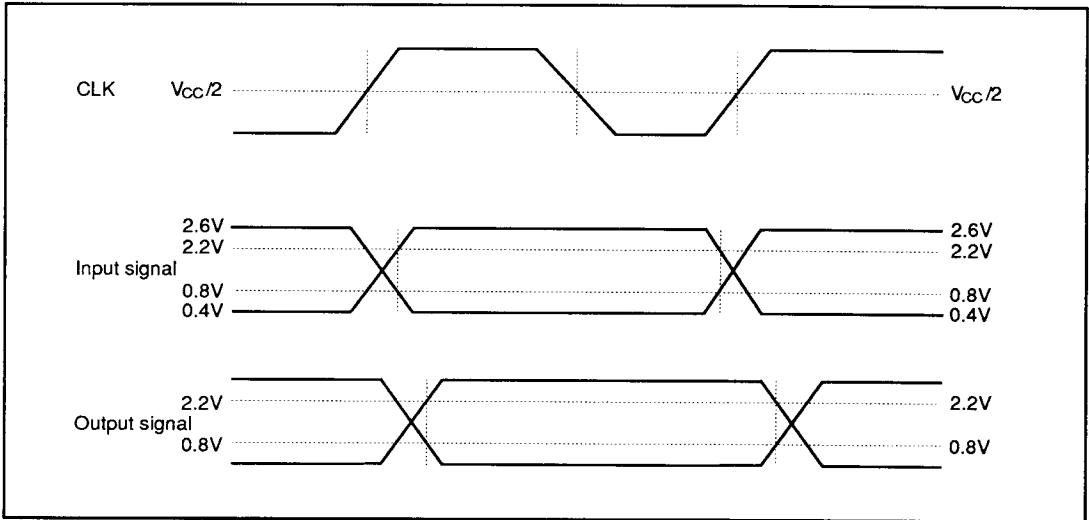
$$V_{CC} = 5V \pm 5\%, V_{SS} = 0V, T_a = 0 \text{ to } 70^\circ \text{C}$$

No.	Item	Symbol	Standard		Unit	Notes
			Min.	Max.		
1	Clock cycle time	$t_c$	50	250	ns	Figure 9-4
2	Clock high-level time	$t_w(\text{CH})$	20	—	ns	
3	Clock low-level time	$t_w(\text{CL})$	20	—	ns	
4	Clock rise time	$t_r(\text{C})$	—	5	ns	
5	Clock fall time	$t_f(\text{C})$	—	5	ns	
6	BAT, A0 to A29, $\overline{\text{BC}}$ , $\overline{\text{BLOCK}}$ delay time	$t_d(\text{CH-A})$	—	30	ns	Figure 9-5
7	BAT, A0 to A29, $\overline{\text{BC}}$ , $\overline{\text{BLOCK}}$ hold time	$t_h(\text{CH-A})$	0	—	ns	
8	BAT, A0 to A29, $\overline{\text{BC}}$ , $\overline{\text{BLOCK}}$ float delay time (bus master)	$t_d(\text{CH-AZ}) \text{ M}$	—	25	ns	
9	Read data setup time (bus master)	$t_{su}(\text{RD-CL}) \text{ M}$	7	—	ns	
10	Read data hold time (bus master)	$t_h(\text{CL-RD}) \text{ M}$	13	—	ns	
11	Read data hold time for $\overline{\text{DS}}$ negation (bus master)	$t_h(\text{DS-RD}) \text{ M}$	0	—	ns	
12	Write data delay time (bus master)	$t_d(\text{CH-WD}) \text{ M}$	—	30	ns	
13	Write data hold time (bus master)	$t_h(\text{CH-WD}) \text{ M}$	0	—	ns	
14	Write data float delay time	$t_d(\text{CH-WDZ}) \text{ M}$	—	25	ns	
15	$\overline{\text{CSTR}}$ delay time	$t_d(\text{CH-CST})$	—	30	ns	
16	$\overline{\text{AS}}$ delay time	$t_d(\text{CL-AS})$	—	30	ns	
17	$\overline{\text{DS}}$ delay time	$t_d(\text{C-DS})$	—	30	ns	
18	R/W delay time (bus master)	$t_d(\text{CH-RW}) \text{ M}$	—	30	ns	
19	R/W hold time (bus master)	$t_h(\text{CH-RW}) \text{ M}$	0	—	ns	
20	$\overline{\text{DBEN}}$ delay time (bus master)	$t_d(\text{CH-DE}) \text{ M}$	—	30	ns	
21	$\overline{\text{DIN}}$ delay time (bus master)	$t_d(\text{CL-DI}) \text{ M}$	—	30	ns	
22	$\overline{\text{DC}}$ and $\overline{\text{IORDY}}$ setup time	$t_{su}(\text{DC-CH})$	7	—	ns	
23	$\overline{\text{DC}}$ and $\overline{\text{IORDY}}$ hold time for $\overline{\text{DS}}$ negation	$t_h(\text{DS-DC})$	0	—	ns	
24	$\overline{\text{ACK}}$ delay time	$t_d(\text{C-AK})$	—	30	ns	
25	$\overline{\text{DONE}}$ delay time (output)	$t_d(\text{CH-DO}) \text{ O}$	—	30	ns	
26	$\overline{\text{DONE}}$ float delay time (output)	$t_d(\text{CH-DOZ}) \text{ O}$	—	25	ns	
27	$\overline{\text{DONE}}$ setup time (input)	$t_{su}(\text{DO-CH}) \text{ I}$	7	—	ns	
28	$\overline{\text{DONE}}$ hold time for $\overline{\text{DS}}$ negation	$t_h(\text{DS-DO}) \text{ I}$	0	—	ns	
29	$\overline{\text{DONE}}$ setup time for $\overline{\text{DC}}$ negation	$t_{su}(\text{DO-DC}) \text{ I}$	10	—	ns	
30	$\overline{\text{BERR}}$ and $\overline{\text{RERUN}}$ setup time	$t_{su}(\text{BR-CL})$	20	—	ns	
31	$\overline{\text{BERR}}$ and $\overline{\text{RERUN}}$ hold time	$t_h(\text{CL-BE})$	13	—	ns	
32	$\overline{\text{HREQ}}$ delay time	$t_d(\text{CL-HR})$	—	30	ns	Figure 9-6
33	$\overline{\text{HACK}}$ setup time	$t_{su}(\text{HA-CL})$	7	—	ns	

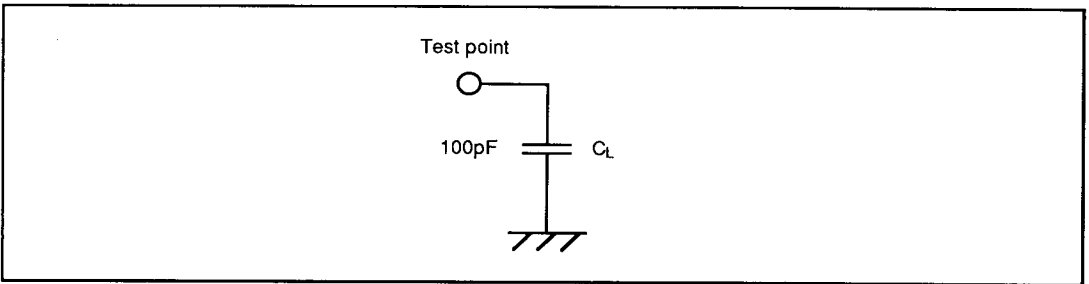
### 9.3.2 AC Characteristics (cont)

$V_{CC} = 5V \pm 5\%$ ,  $V_{SS} = 0V$ ,  $T_a = 0$  to  $70^\circ C$

No.	Item	Symbol	Standard		Unit	Notes
			Min.	Max.		
34	$\overline{ABEN}$ , $\overline{AIN}$ , $\overline{DBEN}$ , $\overline{DIN}$ valid delay time (bus master)	$t_{d(CH-AEV)} M$	—	30	ns	Figure 9-6
35	$\overline{AS}$ , $\overline{DS}$ , R/W valid delay time (bus master)	$t_{d(CL-AEZ)} M$	—	25	ns	
36	$\overline{ABEN}$ , $\overline{AIN}$ , $\overline{DBEN}$ , $\overline{DIN}$ float delay time (bus master)	$t_{d(CH-ASV)} M$	—	30	ns	
37	$\overline{AS}$ , $\overline{DS}$ , R/W float delay time (bus master)	$t_{d(CH-ASZ)} M$	—	25	ns	
38	$\overline{REQ}$ setup time (burst mode)	$t_{su(CL-RQ)} B$	7	—	ns	
39	$\overline{CS}$ , $\overline{IACK}$ setup time	$t_{su}(CS-CL)$	7	—	ns	Figure 9-7
40	$\overline{ABEN}$ , $\overline{AIN}$ , $\overline{DBEN}$ , $\overline{DIN}$ valid delay (bus slave)	$t_{d(CH-AEV)} S$	—	30	ns	
41	$\overline{ABEN}$ , $\overline{AIN}$ , $\overline{DBEN}$ , $\overline{DIN}$ float delay (bus slave)	$t_{d(CH-AEZ)} S$	—	25	ns	
42	$\overline{ABEN}$ delay time (bus slave)	$t_{d(CH-AE)} S$	—	30	ns	
43	$\overline{AIN}$ delay time (bus slave)	$t_{d(CL-AI)} S$	—	30	ns	
44	$\overline{DBEN}$ delay (bus slave)	$t_{d(CH-DE)} S$	—	30	ns	
45	$\overline{DBEN}$ delay time for $\overline{CS}$ , $\overline{IACK}$ negation	$t_{d}(CS-DE)$	—	35	ns	
46	Read data delay time (bus slave)	$t_{d}(CH-RD) S$	—	30	ns	
47	Data float delay time for $\overline{CS}$ , $\overline{IACK}$ negation	$t_{d}(CS-RDZ) S$	—	30	ns	
48	$\overline{DC}$ delay time	$t_{d}(CH-DC)$	—	30	ns	
49	$\overline{DC}$ delay time for $\overline{CS}$ , $\overline{IACK}$ negation	$t_{d}(CS-DC)$	—	35	ns	
50	$\overline{DC}$ high-level width	$t_w(DCH)$	0	—	ns	
51	A23 to A29, $\overline{BC}$ setup time	$t_{su}(AD-CH) S$	7	—	ns	
52	R/W setup time	$t_{su}(RW-CL) S$	7	—	ns	
53	$\overline{DIN}$ delay time (bus slave)	$t_{d}(CL-DI) S$	—	30	ns	Figure 9-8
54	Write data setup time (bus slave)	$t_{su}(WD-CL) S$	7	—	ns	
55	Write data hold time (bus slave)	$t_h(CL-WD) S$	13	—	ns	
56	$\overline{DHREQ}$ setup time	$t_{su}(DR-CL)$	7	—	ns	Figure 9-9
57	$\overline{DHACK}$ delay time	$t_{d}(CL-DA)$	—	30	ns	
58	$\overline{PCL}$ delay time (output)	$t_{d}(CH-PC) O$	—	30	ns	Figure 9-10
59	$\overline{PCL}$ setup time (input)	$t_{su}(PC-CL) I$	7	—	ns	
60	$\overline{IRQ}$ delay time (input)	$t_{d}(CL-IR)$	—	30	ns	
61	$\overline{IRQ}$ float delay time	$t_{d}(CL-IRZ)$	—	25	ns	
62	$\overline{REQ}$ setup time (cycle steal mode)	$t_{su}(CL-RQ)$	7	—	ns	Figure 9-11
63	$\overline{REQ}$ pulse width (cycle steal mode)	$t_w(RQ) C$	50	—	ns	
64	$\overline{REQ}$ valid time for $\overline{ACK}$ assert (cycle steal mode)	$t_v(AK-RQ) C$	0	—	ns	



**Figure 9-1 Measuring Conditions**



**Figure 9-2 Test Load Circuit (All Output Pins)**

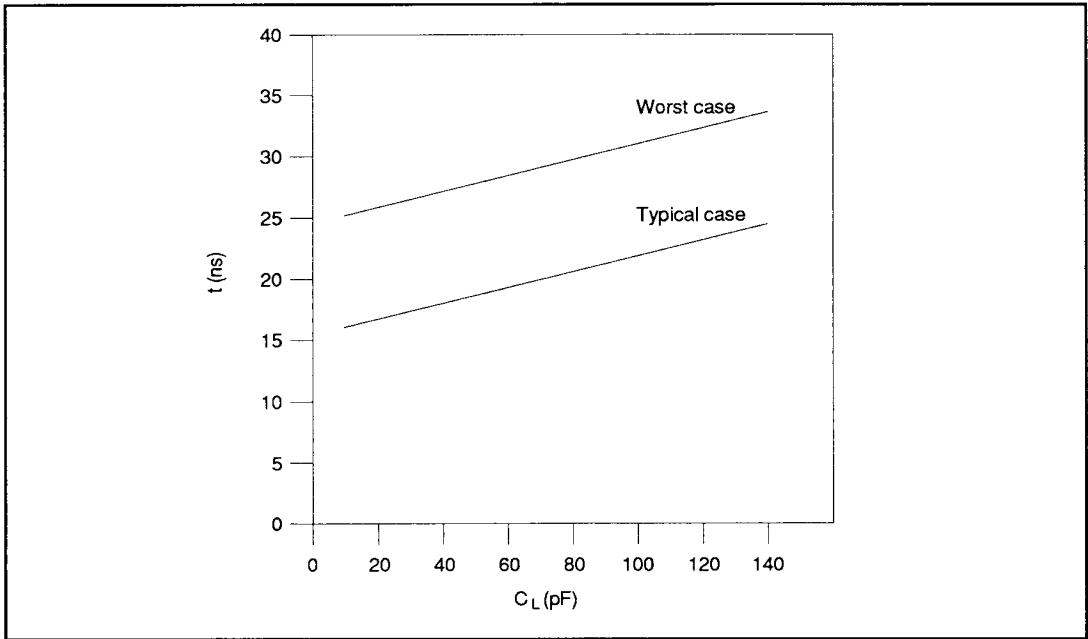


Figure 9-3 Example of Output Delay Load Capacitance for CLK Input (Excluding Output Float Delay for CLK Input)

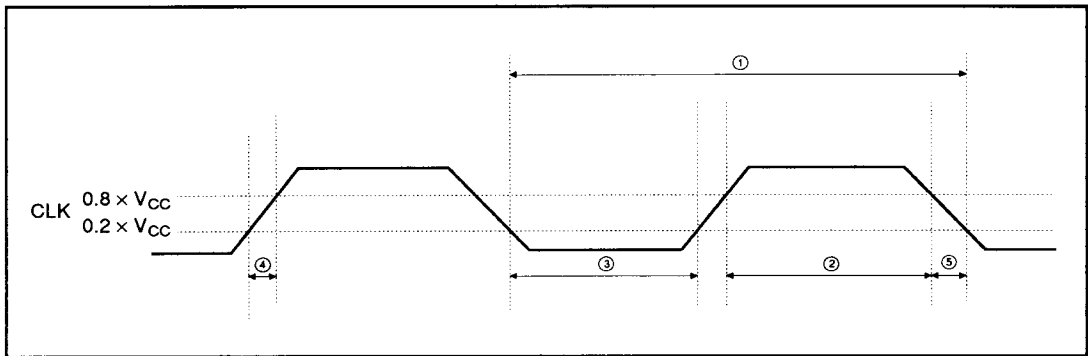


Figure 9-4 Clock

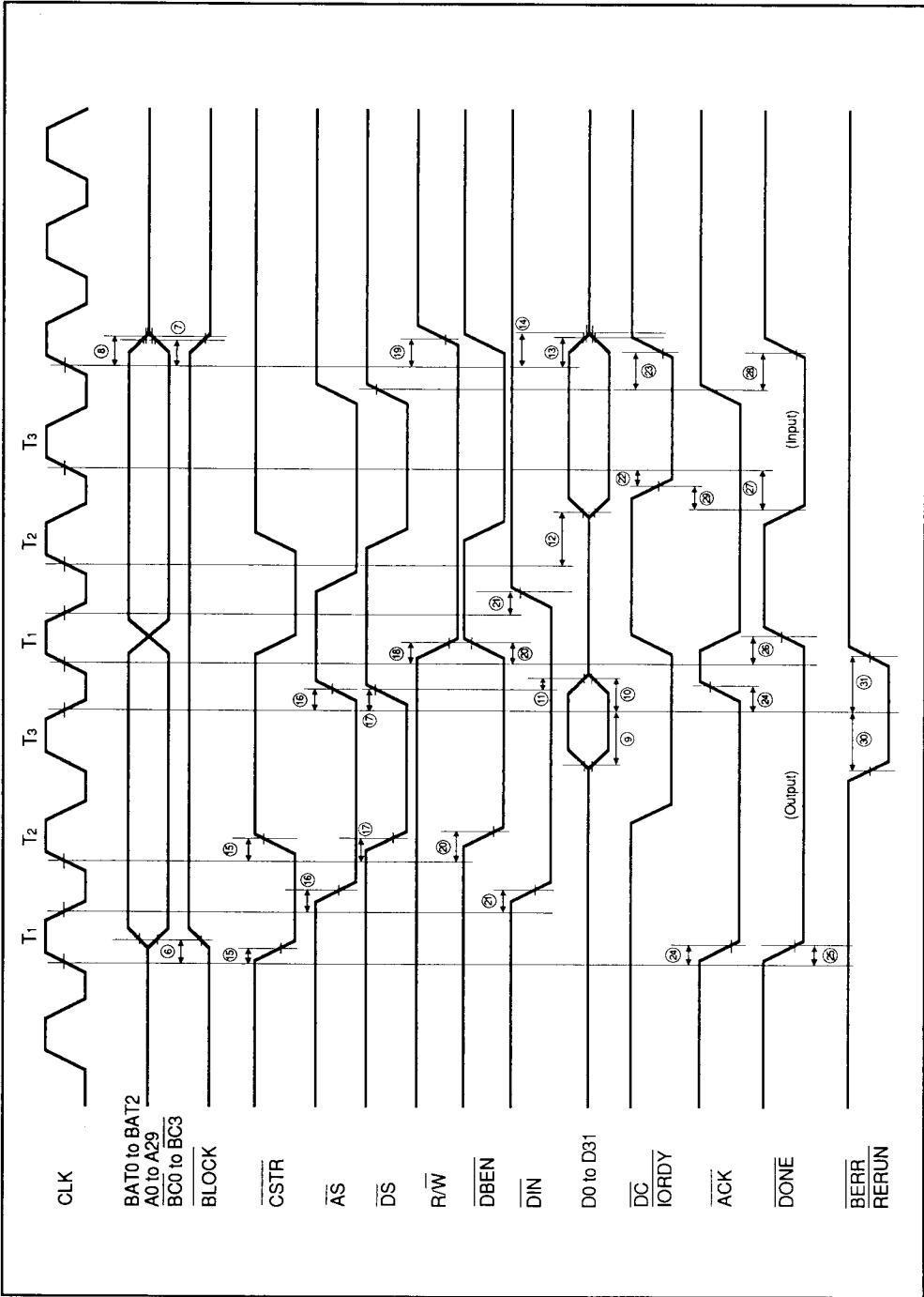


Figure 9-5 Read/Write Cycle

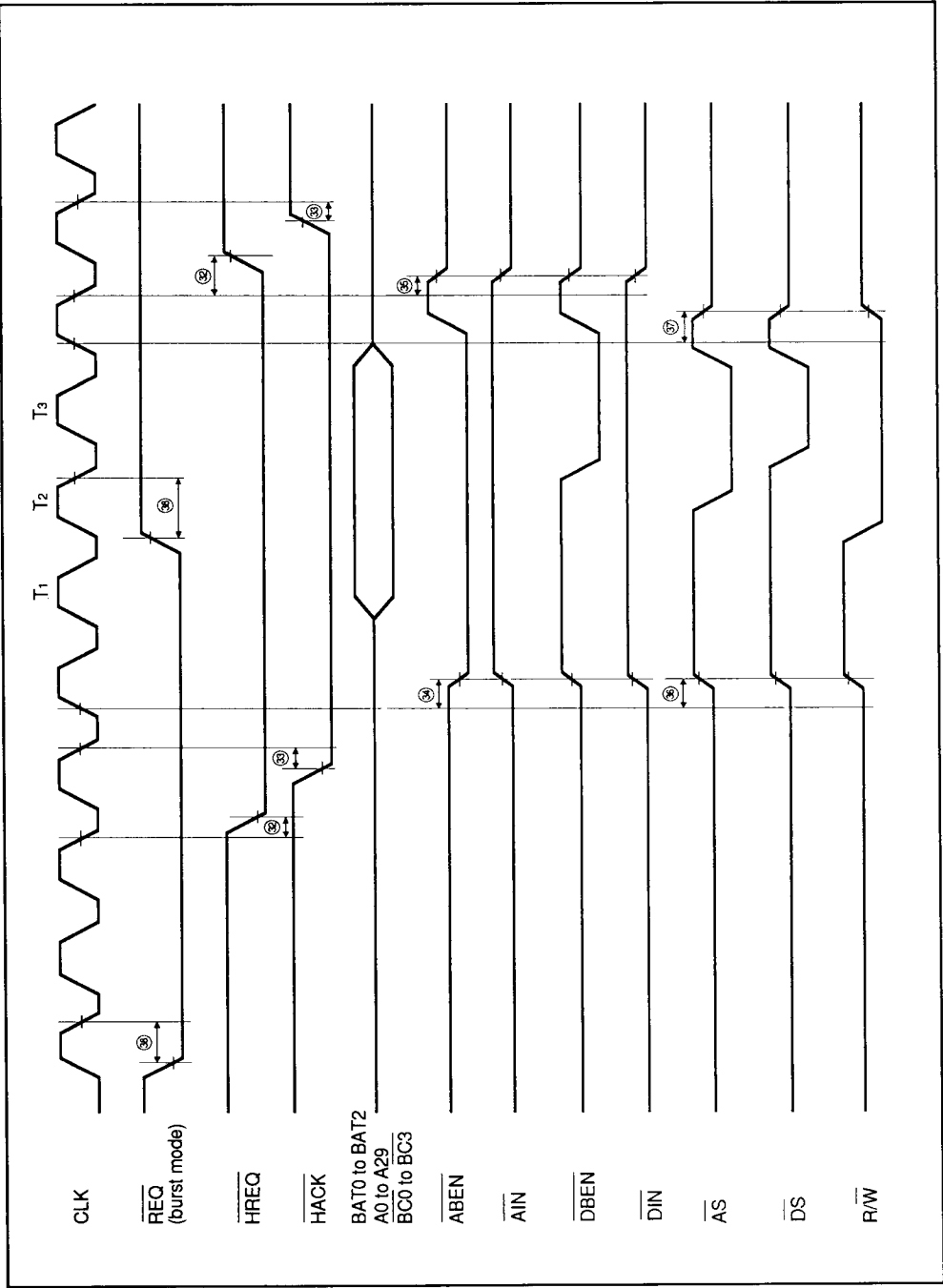


Figure 9-6 Bus Arbitration



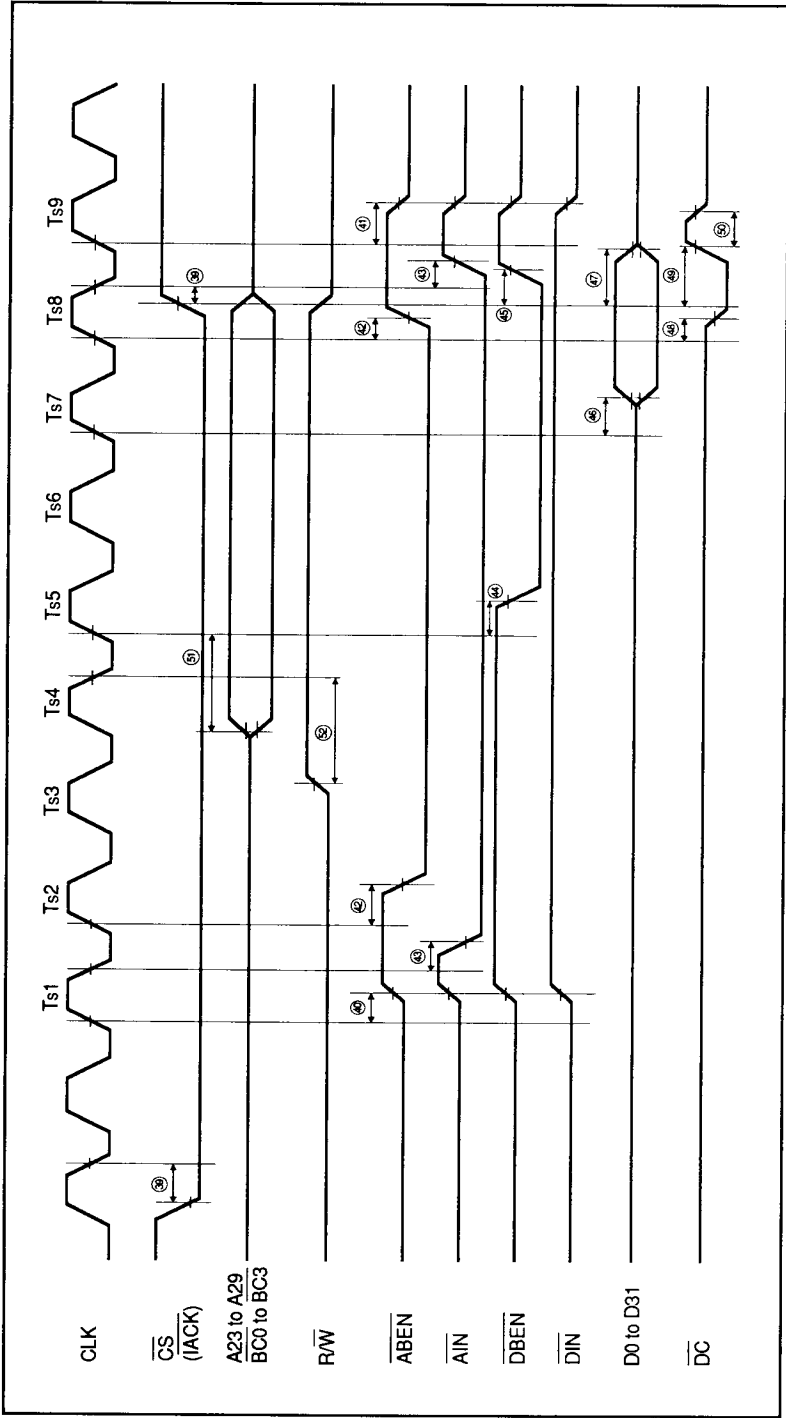


Figure 9-7 Slave Read Cycle

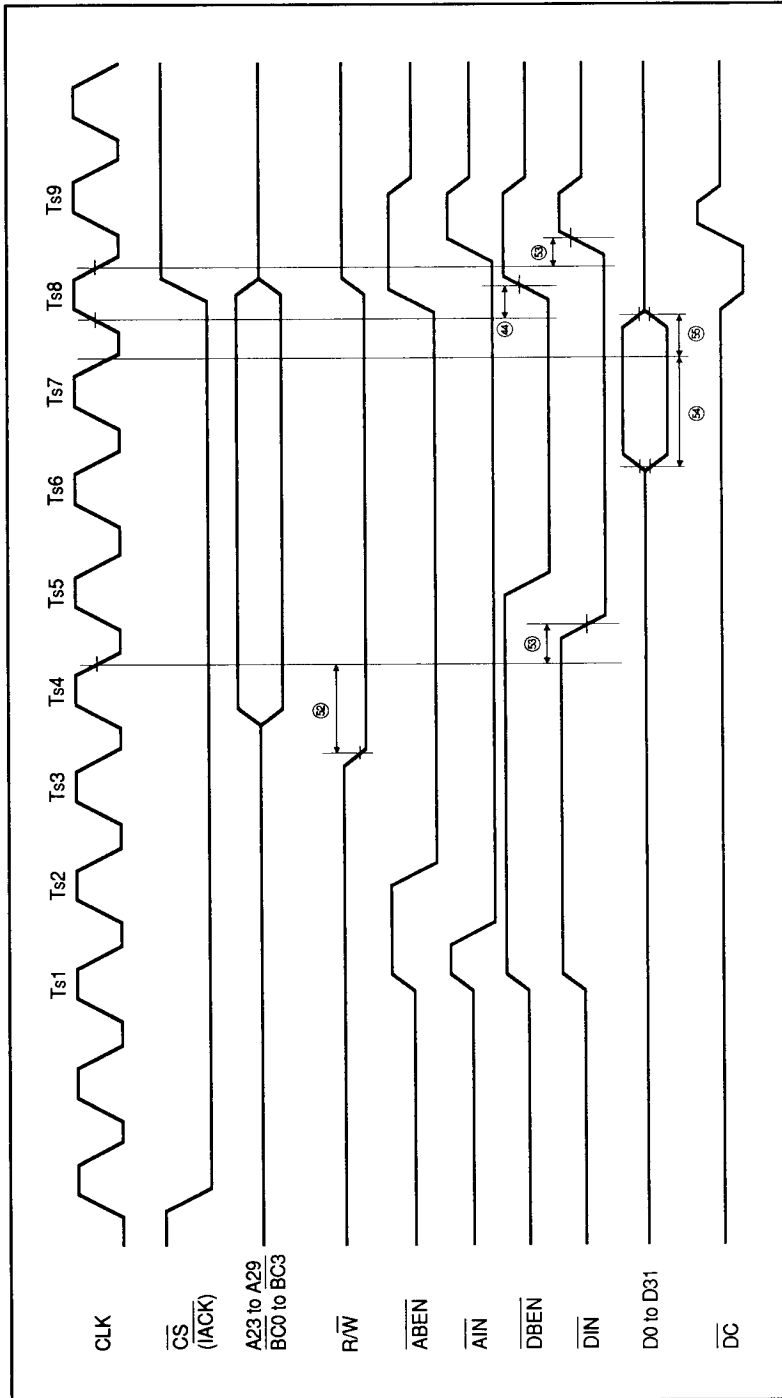


Figure 9-8 Slave Write Cycle

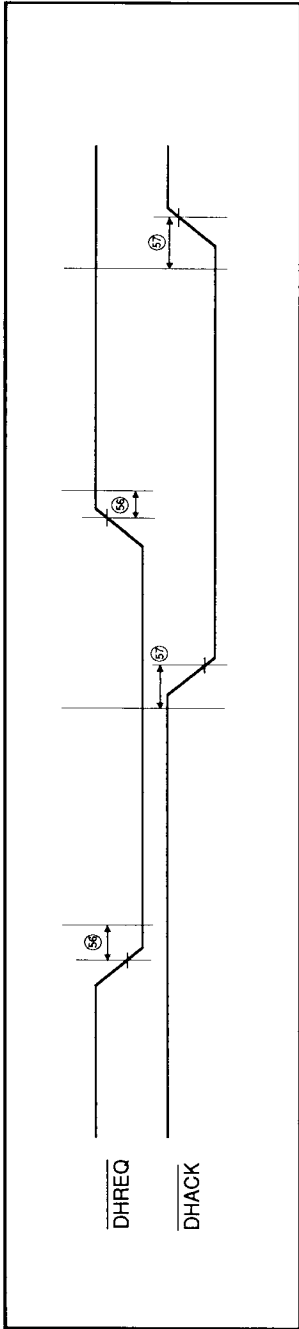


Figure 9-9 Halt Operation

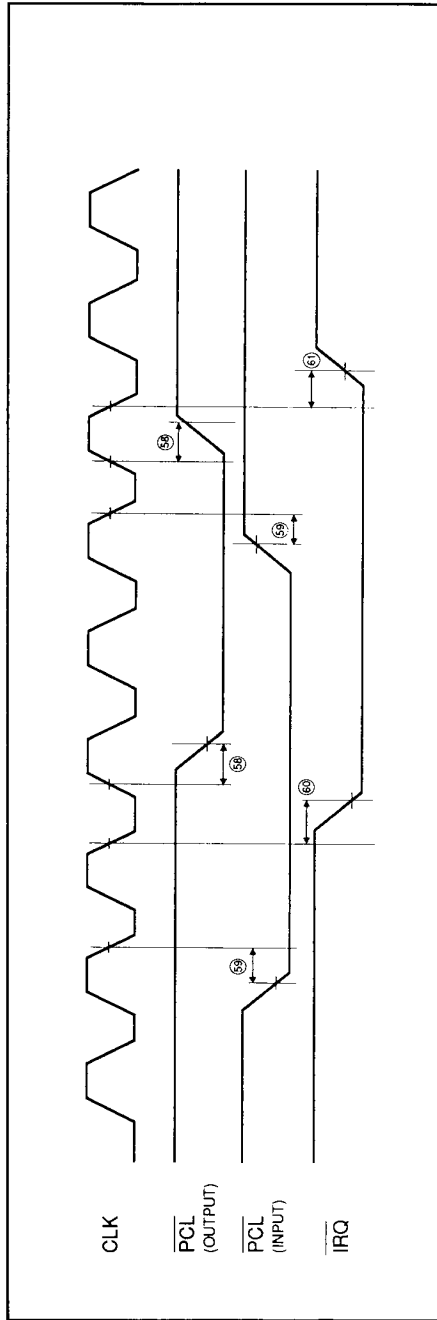


Figure 9-10 PCL and IRQ

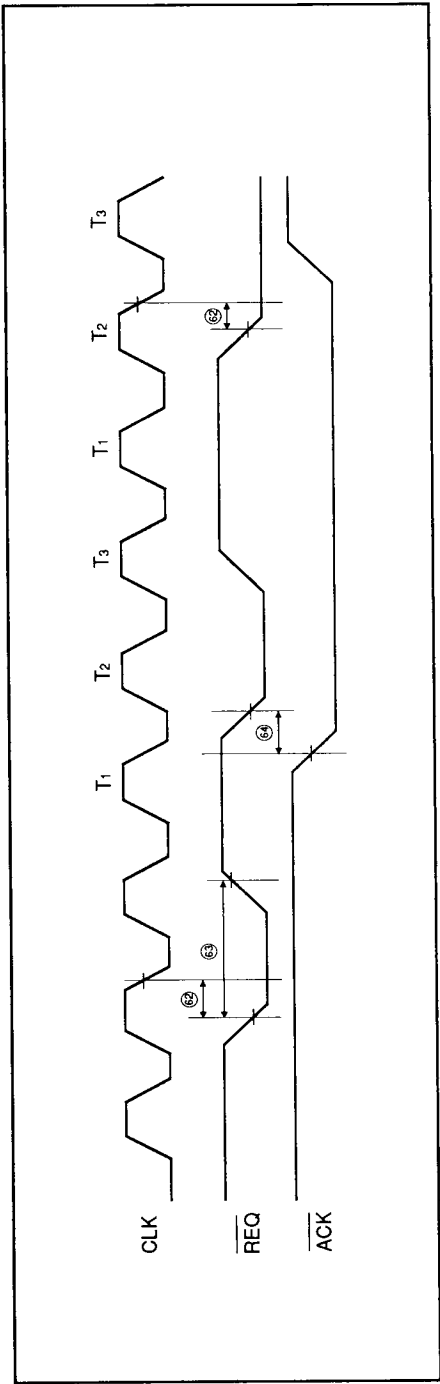


Figure 9-11 REQ# (Cycle Steal Mode)

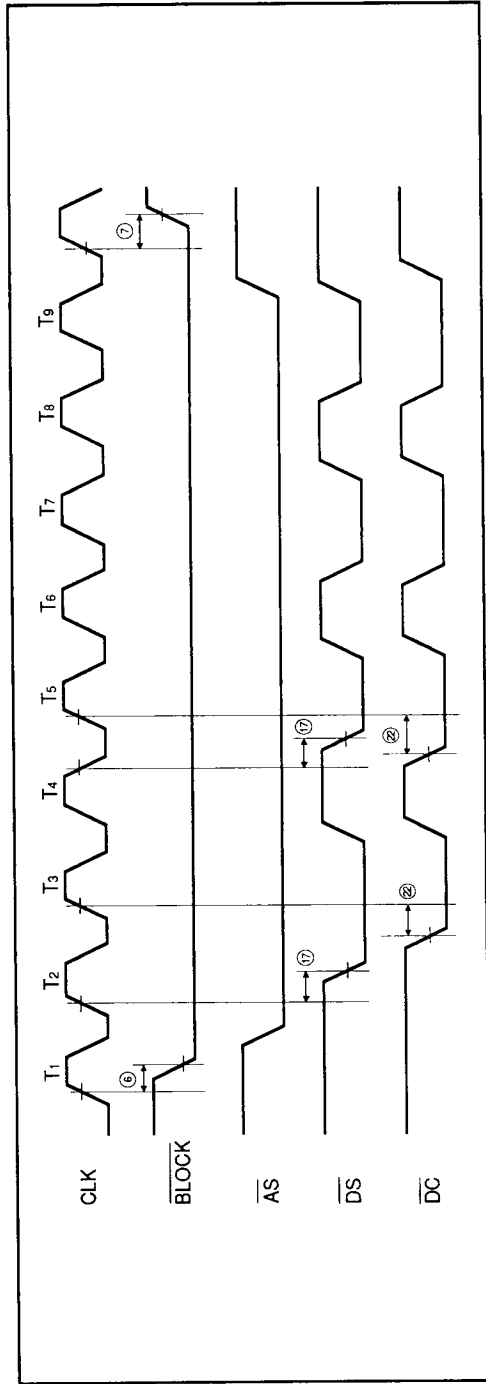


Figure 9-12 Block Transfer