

# MC14017B

## Decade Counter

The MC14017B is a five-stage Johnson decade counter with built-in code converter. High speed operation and spike-free outputs are obtained by use of a Johnson decade counter design. The ten decoded outputs are normally low, and go high only at their appropriate decimal time period. The output changes occur on the positive-going edge of the clock pulse. This part can be used in frequency division applications as well as decade counter or decimal decode display applications.

### Features

- Fully Static Operation
- DC Clock Input Circuit Allows Slow Rise Times
- Carry Out Output for Cascading
- Divide-by-N Counting
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement for CD4017B
- Triple Diode Protection on All Inputs
- These Devices are Pb-Free and are RoHS Compliant
- NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable

### MAXIMUM RATINGS (Voltages Referenced to V<sub>SS</sub>)

Symbol	Parameter	Value	Unit
V <sub>DD</sub>	DC Supply Voltage Range	-0.5 to +18.0	V
V <sub>in</sub> , V <sub>out</sub>	Input or Output Voltage Range (DC or Transient)	-0.5 to V <sub>DD</sub> + 0.5	V
I <sub>in</sub> , I <sub>out</sub>	Input or Output Current (DC or Transient) per Pin	±10	mA
P <sub>D</sub>	Power Dissipation, per Package (Note 1)	500	mW
T <sub>A</sub>	Ambient Temperature Range	-55 to +125	°C
T <sub>stg</sub>	Storage Temperature Range	-65 to +150	°C
T <sub>L</sub>	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

#### 1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range V<sub>SS</sub> ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>DD</sub>.

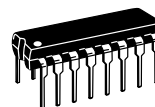
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>). Unused outputs must be left open.



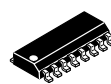
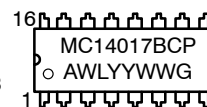
ON Semiconductor®

<http://onsemi.com>

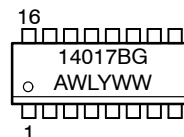
### MARKING DIAGRAMS



PDIP-16  
P SUFFIX  
CASE 648



SOIC-16  
D SUFFIX  
CASE 751B



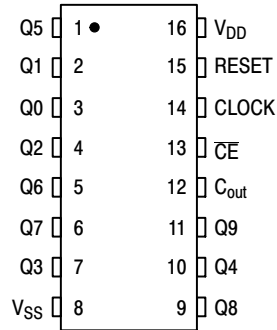
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G = Pb-Free Indicator

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

# MC14017B

## PIN ASSIGNMENT

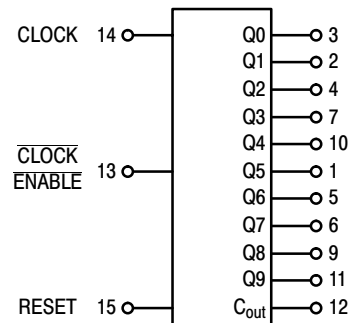


## FUNCTIONAL TRUTH TABLE (Positive Logic)

Clock	Clock Enable	Reset	Decode Output=n
0	X	0	n
X	1	0	n
X	X	1	Q0
↗	0	0	n+1
↘	X	0	n
X	↗	0	n
1	↘	0	n+1

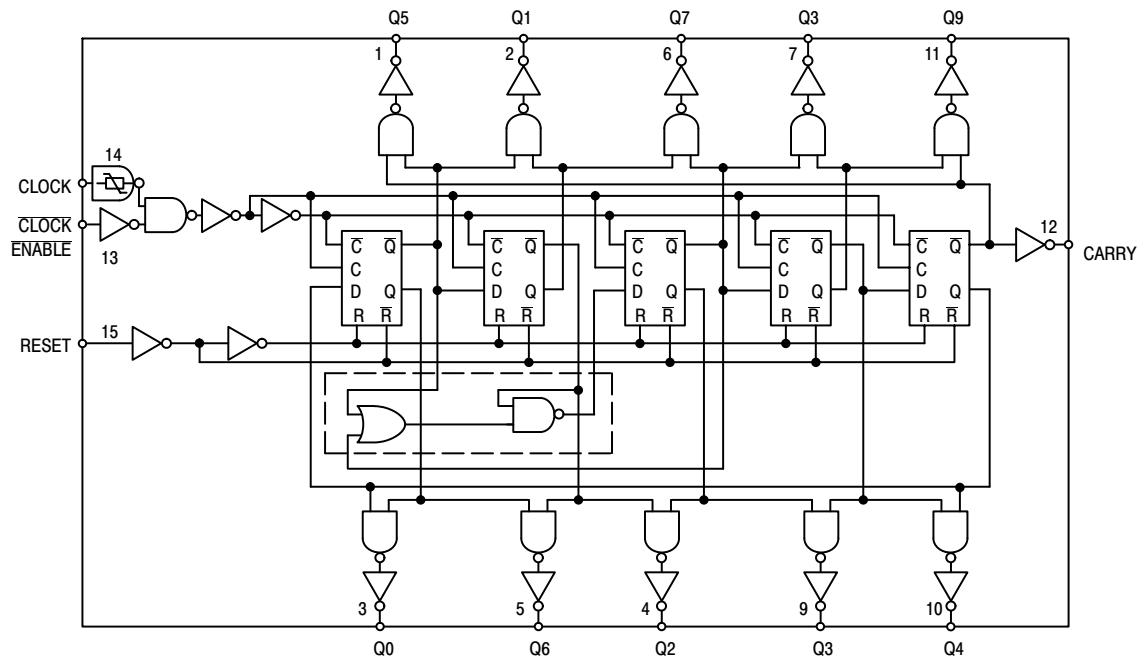
X = Don't Care. If n < 5 Carry = "1",  
Otherwise = "0".

## BLOCK DIAGRAM



V<sub>DD</sub> = PIN 16  
V<sub>SS</sub> = PIN 8

## LOGIC DIAGRAM



# MC14017B

## ELECTRICAL CHARACTERISTICS (Voltages Referenced to V<sub>SS</sub>)

Characteristic	Symbol	V <sub>DD</sub> Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V <sub>in</sub> = V <sub>DD</sub> or 0  V <sub>in</sub> = 0 or V <sub>DD</sub>	"0" Level V <sub>OL</sub>	5.0	—	0.05	—	0	0.05	—	0.05	Vdc	
		10	—	0.05	—	0	0.05	—	0.05		
		15	—	0.05	—	0	0.05	—	0.05		
	"1" Level V <sub>OH</sub>	5.0	4.95	—	4.95	5.0	—	4.95	—		Vdc
		10	9.95	—	9.95	10	—	9.95	—		
		15	14.95	—	14.95	15	—	14.95	—		
Input Voltage "0" Level (V <sub>O</sub> = 4.5 or 0.5 Vdc) (V <sub>O</sub> = 9.0 or 1.0 Vdc) (V <sub>O</sub> = 13.5 or 1.5 Vdc)  "1" Level (V <sub>O</sub> = 0.5 or 4.5 Vdc) (V <sub>O</sub> = 1.0 or 9.0 Vdc) (V <sub>O</sub> = 1.5 or 13.5 Vdc)	V <sub>IL</sub>	5.0	—	1.5	—	2.25	1.5	—	1.5	Vdc	
		10	—	3.0	—	4.50	3.0	—	3.0		
		15	—	4.0	—	6.75	4.0	—	4.0		
	V <sub>IH</sub>	5.0	3.5	—	3.5	2.75	—	3.5	—		Vdc
		10	7.0	—	7.0	5.50	—	7.0	—		
		15	11	—	11	8.25	—	11	—		
Output Drive Current (V <sub>OH</sub> = 2.5 Vdc) (V <sub>OH</sub> = 4.6 Vdc) (V <sub>OH</sub> = 9.5 Vdc) (V <sub>OH</sub> = 13.5 Vdc)  (V <sub>OL</sub> = 0.4 Vdc) (V <sub>OL</sub> = 0.5 Vdc) (V <sub>OL</sub> = 1.5 Vdc)	Source I <sub>OH</sub>	5.0	-3.0	—	-2.4	-4.2	—	-1.7	—	mAdc	
		5.0	-0.64	—	-0.51	-0.88	—	-0.36	—		
		10	-1.6	—	-1.3	-2.25	—	-0.9	—		
		15	-4.2	—	-3.4	-8.8	—	-2.4	—		
	Sink I <sub>OL</sub>	5.0	0.64	—	0.51	0.88	—	0.36	—		mAdc
		10	1.6	—	1.3	2.25	—	0.9	—		
		15	4.2	—	3.4	8.8	—	2.4	—		
Input Current	I <sub>in</sub>	15	—	± 0.1	—	± 0.00001	± 0.1	—	± 1.0	μAdc	
Input Capacitance (V <sub>in</sub> = 0)	C <sub>in</sub>	—	—	—	—	5.0	7.5	—	—	pF	
Quiescent Current (Per Package)	I <sub>DD</sub>	5.0	—	5.0	—	0.005	5.0	—	150	μAdc	
		10	—	10	—	0.010	10	—	300		
		15	—	20	—	0.015	20	—	600		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C <sub>L</sub> = 50 pF on all outputs, all buffers switching)	I <sub>T</sub>	5.0	I <sub>T</sub> = (0.27 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.55 μA/kHz) f + I <sub>DD</sub> I <sub>T</sub> = (0.83 μA/kHz) f + I <sub>DD</sub>							μAdc	

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) Vfk$$

where: I<sub>T</sub> is in μA (per package), C<sub>L</sub> in pF, V = (V<sub>DD</sub> - V<sub>SS</sub>) in volts, f in kHz is input frequency, and k = 0.0011.

## ORDERING INFORMATION

Device	Package	Shipping†
MC14017BCPG	PDIP-16 (Pb-Free)	500 Units / Rail
MC14017BDG	SOIC-16	48 Units / Rail
NLV14017BDG*		
MC14017BDR2G	SOIC-16 (Pb-Free)	2500 Units / Tape & Reel
NLV14017BDR2G*		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

\*NLV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q100 Qualified and PPAP Capable.

# MC14017B

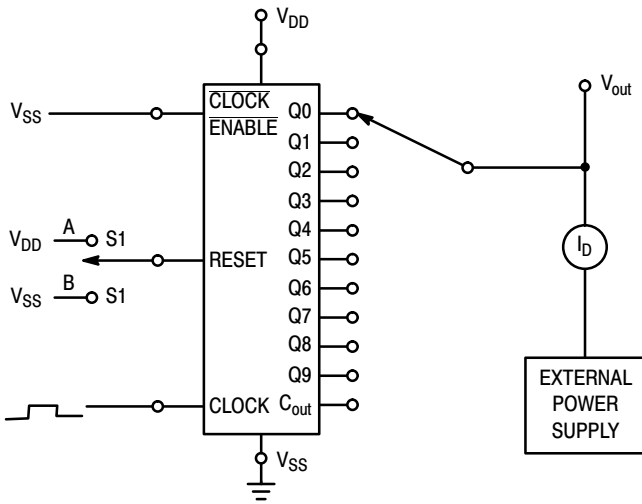
## SWITCHING CHARACTERISTICS (Note 5) ( $C_L = 50$ pF, $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise and Fall Time $t_{TLH}, t_{THL} = (1.5 \text{ ns/pF}) C_L + 25 \text{ ns}$ $t_{TLH}, t_{THL} = (0.75 \text{ ns/pF}) C_L + 12.5 \text{ ns}$ $t_{TLH}, t_{THL} = (0.55 \text{ ns/pF}) C_L + 9.5 \text{ ns}$	$t_{TLH},$ $t_{THL}$	5.0 10 15	— — —	100 50 40	200 100 80	ns
Propagation Delay Time Reset to Decode Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Propagation Delay Time Clock to $C_{out}$ $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Propagation Delay Time Clock to Decode Output $t_{PLH}, t_{PHL} = (1.7 \text{ ns/pF}) C_L + 415 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.66 \text{ ns/pF}) C_L + 197 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.5 \text{ ns/pF}) C_L + 150 \text{ ns}$	$t_{PLH},$ $t_{PHL}$	5.0 10 15	— — —	500 230 175	1000 460 350	ns
Turn-Off Delay Time Reset to $C_{out}$ $t_{PLH} = (1.7 \text{ ns/pF}) C_L + 315 \text{ ns}$ $t_{PLH} = (0.66 \text{ ns/pF}) C_L + 142 \text{ ns}$ $t_{PLH} = (0.5 \text{ ns/pF}) C_L + 100 \text{ ns}$	$t_{PLH}$	5.0 10 15	— — —	400 175 125	800 350 250	ns
Clock Pulse Width	$t_{w(H)}$	5.0 10 15	250 100 75	125 50 35	— — —	ns
Clock Frequency	$f_{cl}$	5.0 10 15	— — —	5.0 12 16	2.0 5.0 6.7	MHz
Reset Pulse Width	$t_{w(H)}$	5.0 10 15	500 250 190	250 125 95	— — —	ns
Reset Removal Time	$t_{rem}$	5.0 10 15	750 275 210	375 135 105	— — —	ns
Clock Input Rise and Fall Time	$t_{TLH},$ $t_{THL}$	5.0 10 15	No Limit			—
Clock Enable Setup Time	$t_{su}$	5.0 10 15	350 150 115	175 75 52	— — —	ns
Clock Enable Removal Time	$t_{rem}$	5.0 10 15	420 200 140	260 100 70	— — —	ns

5. The formulas given are for the typical characteristics only at  $25^\circ\text{C}$ .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

# MC14017B



	Output Sink Drive	Output Source Drive
Decode Outputs	(S1 to A)	Clock to desired outputs (S1 to B)
Carry	Clock to 5 thru 9 (S1 to B)	S1 to A
$V_{GS} =$	$V_{DD}$	$-V_{DD}$
$V_{DS} =$	$V_{out}$	$V_{out} - V_{DD}$

Figure 1. Typical Output Source and Output Sink Characteristics Test Circuit

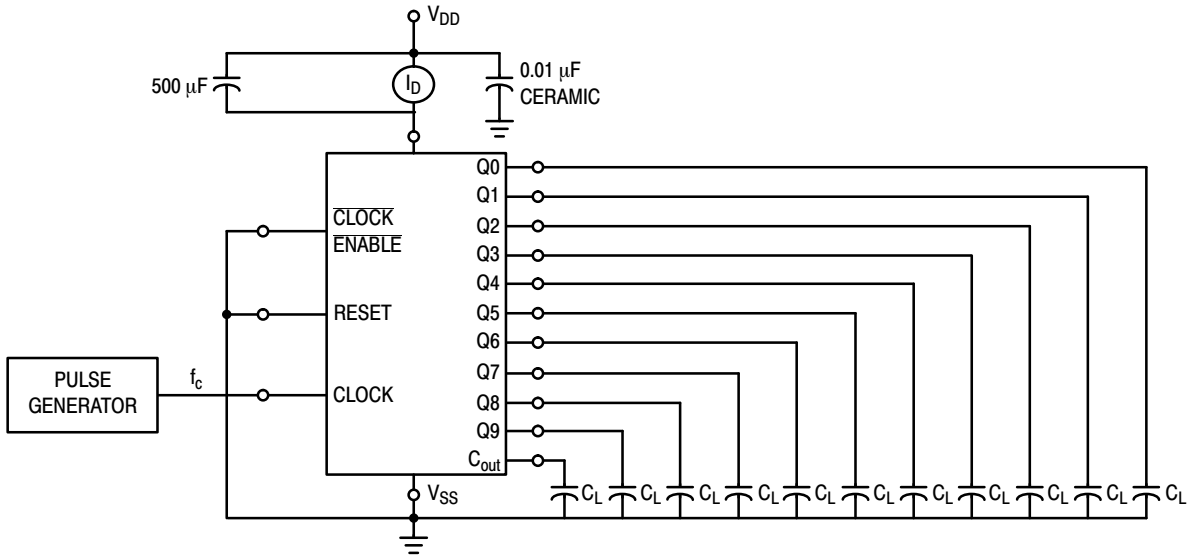


Figure 2. Typical Power Dissipation Test Circuit

# MC14017B

## APPLICATIONS INFORMATION

Figure 3 shows a technique for extending the number of decoded output states for the MC14017B. Decoded outputs are sequential within each stage and from stage to stage, with no dead time (except propagation delay).

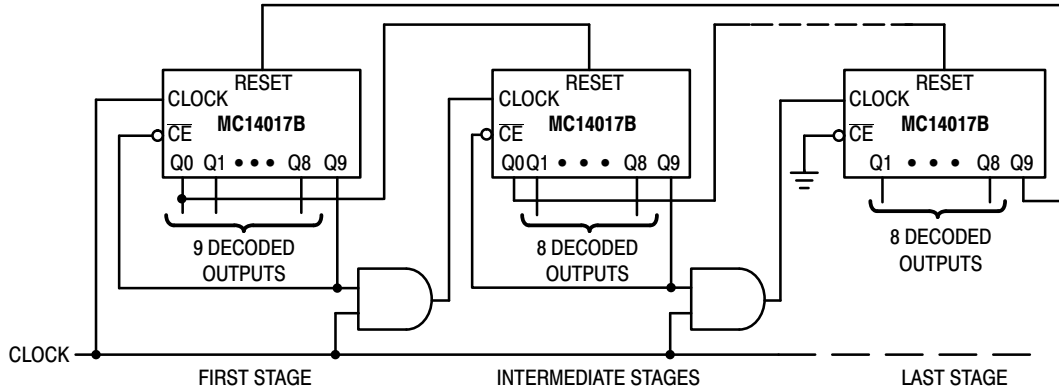


Figure 3. Counter Expansion

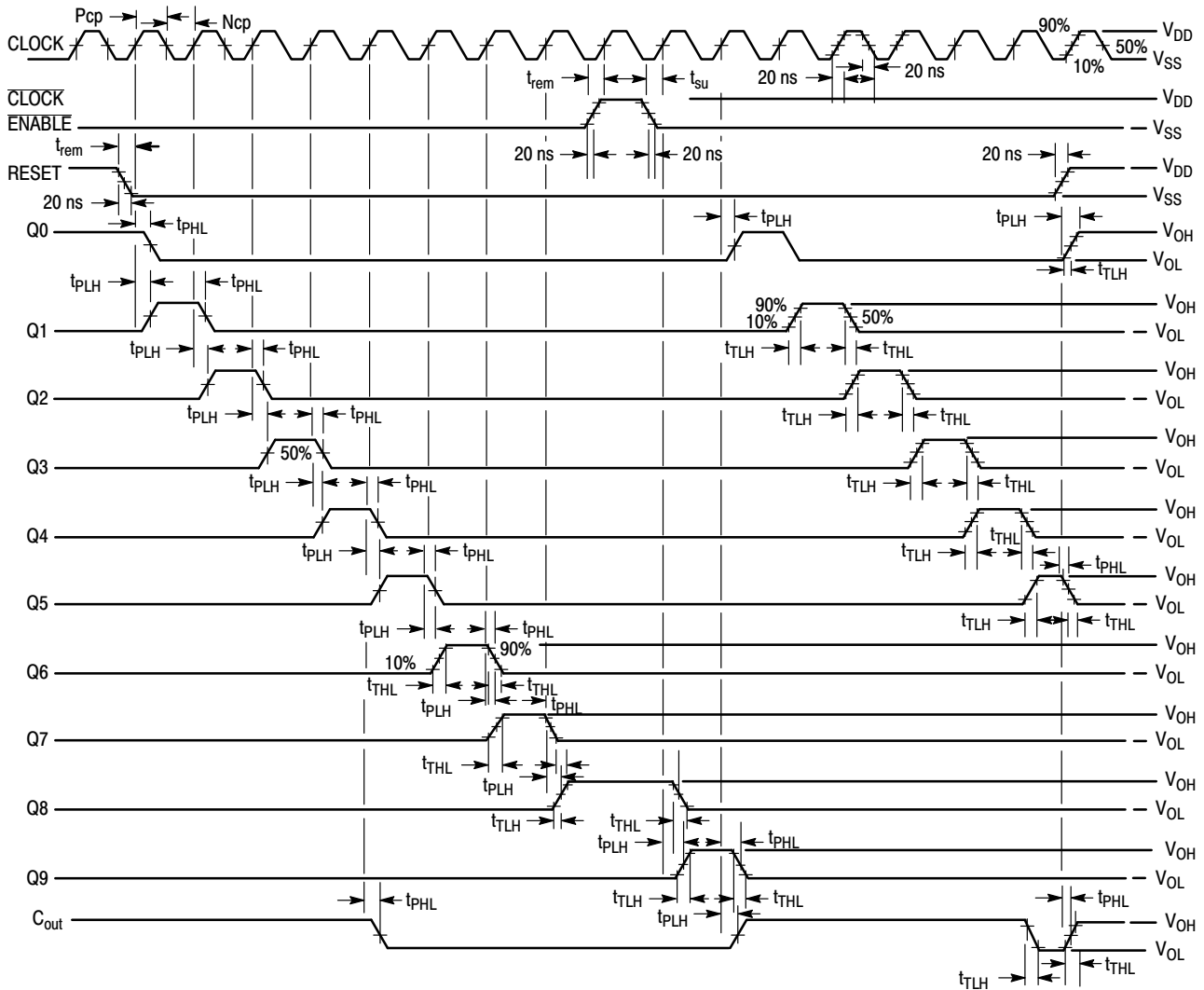
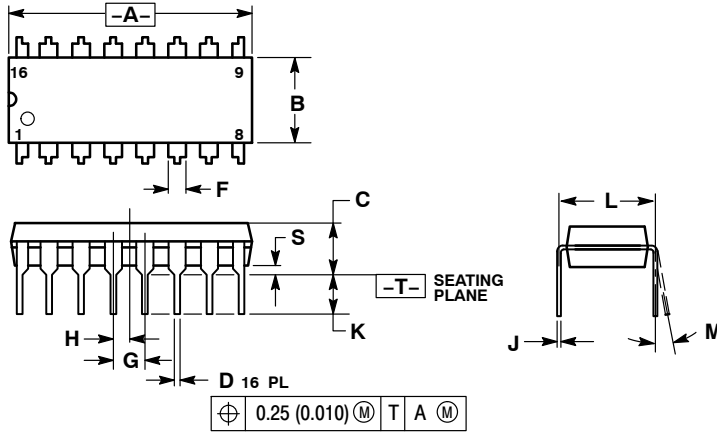


Figure 4. AC Measurement Definition and Functional Waveforms

# MC14017B

## PACKAGE DIMENSIONS

PDIP-16  
P SUFFIX  
PLASTIC DIP PACKAGE  
CASE 648-08  
ISSUE T



NOTES:

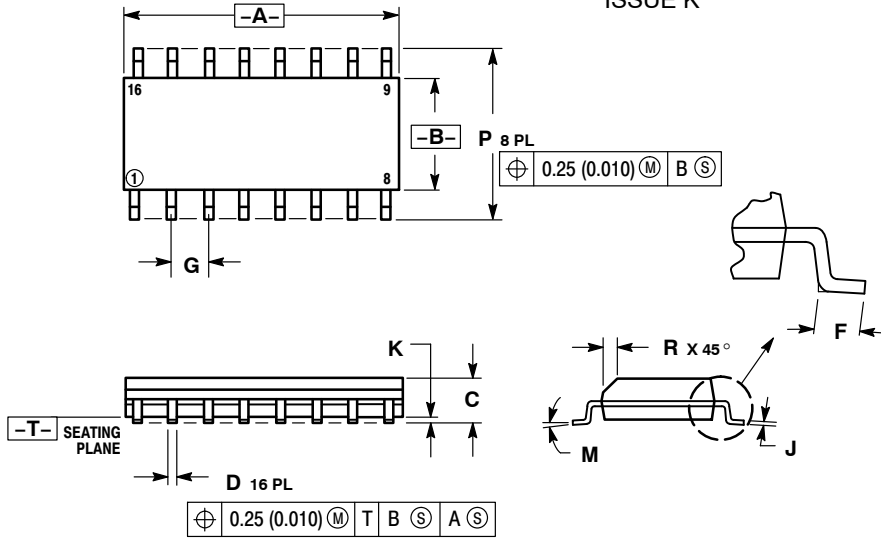
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.740	0.770	18.80	19.55
B	0.250	0.270	6.35	6.85
C	0.145	0.175	3.69	4.44
D	0.015	0.021	0.39	0.53
F	0.040	0.70	1.02	1.77
G	0.100 BSC		2.54 BSC	
H	0.050 BSC		1.27 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.130	2.80	3.30
L	0.295	0.305	7.50	7.74
M	0° 10°		0° 10°	
S	0.020	0.040	0.51	1.01

# MC14017B

## PACKAGE DIMENSIONS

SOIC-16  
D SUFFIX  
PLASTIC SOIC PACKAGE  
CASE 751B-05  
ISSUE K

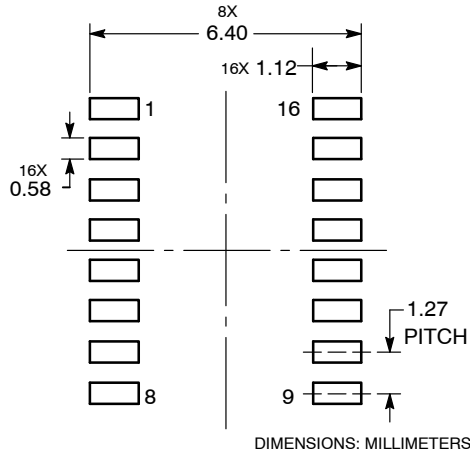


### NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	9.80	10.00	0.386	0.393
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

### SOLDERING FOOTPRINT



ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

#### LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: [orderlit@onsemi.com](mailto:orderlit@onsemi.com)

N. American Technical Support: 800-282-9855 Toll Free  
USA/Canada  
Europe, Middle East and Africa Technical Support:  
Phone: 421 33 790 2910  
Japan Customer Focus Center  
Phone: 81-3-5817-1050

ON Semiconductor Website: [www.onsemi.com](http://www.onsemi.com)

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative