

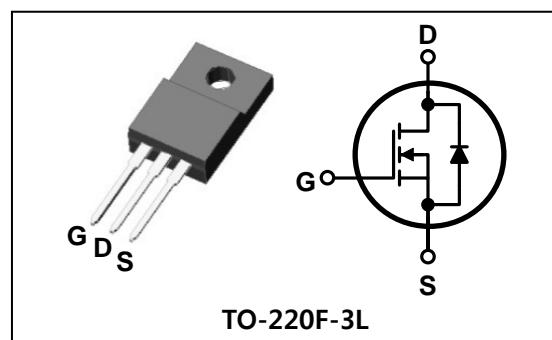
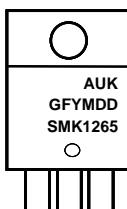
## SWITCHING REGULATOR APPLICATIONS

**Features**

- High Voltage :  $BV_{DSS}=650V$ (Min.)
- Low  $C_{rss}$  :  $C_{rss}=14.6pF$ (Typ.)
- Low gate charge :  $Q_g=41nC$ (Typ.)
- Low  $R_{DS(on)}$  :  $R_{DS(on)}=0.8\Omega$ (Max.)

**Ordering Information**

Type No.	Marking	Package Code
SMK1265FD	SMK1265	TO-220F-3L

**PIN Connection**

**Marking Diagram**


Column 1 : Manufacturer

Column 2 : Production Information

e.g.) GFYMDD

- . G : Option Code (H : Halogen Free)

- . F : Factory Management Code

- . YMDD : Date Code (Year, Month, Date)

Column 3 : Device Code

**Absolute maximum ratings ( $T_c=25^\circ C$  unless otherwise noted)**

Characteristic	Symbol	Rating	Unit
Drain-source voltage	$V_{DSS}$	650	V
Gate-source voltage	$V_{GSS}$	$\pm 30$	V
Drain current (DC) *	$I_D$	$T_c=25^\circ C$	A
		$T_c=100^\circ C$	A
Drain current (Pulsed) *	$I_{DM}$	48	A
Power dissipation	$P_D$	48	W
Avalanche current (Single) ②	$I_{AS}$	12	A
Single pulsed avalanche energy ②	$E_{AS}$	140	mJ
Avalanche current (Repetitive) ①	$I_{AR}$	12	A
Repetitive avalanche energy ①	$E_{AR}$	7.6	mJ
Junction temperature	$T_J$	150	$^\circ C$
Storage temperature range	$T_{stg}$	-55~150	

\* Limited by maximum junction temperature

Characteristic	Symbol	Typ.	Max.	Unit
Thermal resistance	$R_{th(J-C)}$	-	2.6	$^\circ C/W$
	$R_{th(J-A)}$	-	62.5	

## Electrical Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Drain-source breakdown voltage	$\text{BV}_{\text{DSS}}$	$I_D=250\mu\text{A}, V_{GS}=0\text{V}$	650	-	-	V
Gate threshold voltage	$V_{GS(\text{th})}$	$I_D=250\mu\text{A}, V_{DS}=V_{GS}$	2.0	-	4.0	V
Drain-source cut-off current	$I_{\text{DSS}}$	$V_{DS}=650\text{V}, V_{GS}=0\text{V}$	-	-	1	$\mu\text{A}$
Gate leakage current	$I_{\text{GSS}}$	$V_{DS}=0\text{V}, V_{GS}=\pm 30\text{V}$	-	-	$\pm 100$	nA
Drain-source on-resistance <sup>(④)</sup>	$R_{DS(\text{on})}$	$V_{GS}=10\text{V}, I_D=6.0\text{A}$	-	0.68	0.80	$\Omega$
Forward transfer conductance <sup>(④)</sup>	$g_{fs}$	$V_{DS}=10\text{V}, I_D=6.0\text{A}$	-	10	-	S
Input capacitance	$C_{iss}$	$V_{GS}=0\text{V}, V_{DS}=25\text{V}$ $f=1\text{ MHz}$	-	2162	2882	pF
Output capacitance	$C_{oss}$		-	183	244	
Reverse transfer capacitance	$C_{rss}$		-	14.6	19.4	
Turn-on delay time	$t_{d(\text{on})}$	$V_{DD}=300\text{V}, I_D=12\text{A}$ $R_G=25\Omega$	-	30	-	ns
Rise time	$t_r$		-	85	-	
Turn-off delay time	$t_{d(\text{off})}$		-	140	-	
Fall time	$t_f$		-	90	-	
Total gate charge	$Q_g$	$V_{DS}=520\text{V}, V_{GS}=10\text{V}$ $I_D=12\text{A}$	-	43	65	nC
Gate-source charge	$Q_{gs}$		-	13	-	
Gate-drain charge	$Q_{gd}$		-	10.5	-	

## Source-Drain Diode Ratings and Characteristics ( $T_C=25^\circ\text{C}$ unless otherwise noted)

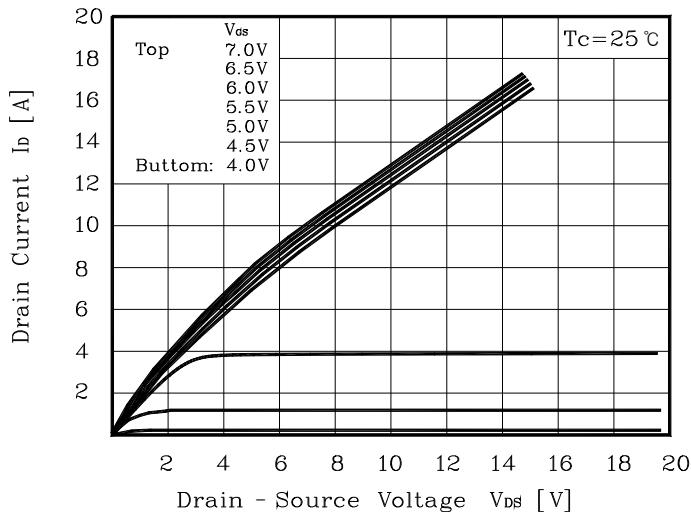
Characteristic	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Source current (DC)	$I_S$	Integral reverse diode in the MOSFET	-	-	12	A
Source current (Pulsed) <sup>(①)</sup>	$I_{SM}$		-	-	48	
Forward voltage <sup>(④)</sup>	$V_{SD}$	$V_{GS}=0\text{V}, I_S=12\text{A}$	-	-	1.4	V
Reverse recovery time	$t_{rr}$	$I_S=12\text{A}, V_{GS}=0\text{V}$ $dI_F/dt=100\text{A}/\mu\text{s}$	-	500	-	ns
Reverse recovery charge	$Q_{rr}$		-	4.3	-	$\mu\text{C}$

Note :

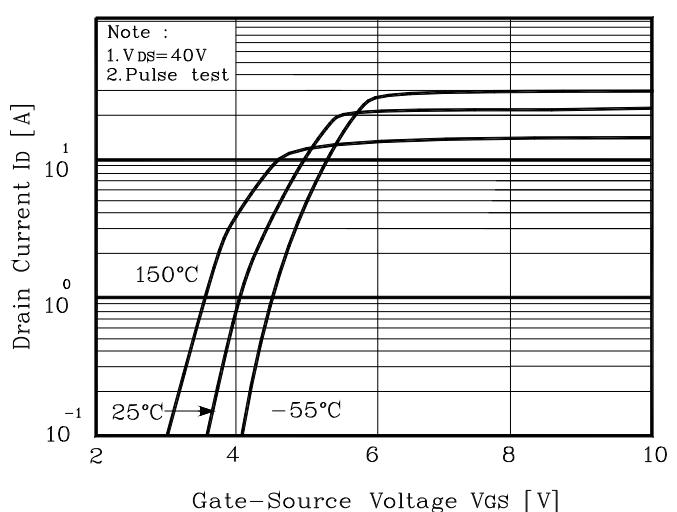
- ① Repetitive rating : Pulse width limited by maximum junction temperature
- ②  $L=1.8\text{mH}, I_{AS}=12\text{A}, V_{DD}=50\text{V}, R_G=25\Omega$ , Starting  $T_J=25^\circ\text{C}$
- ③ Pulse Test : Pulse width  $\leq 300\text{us}$ , Duty cycle  $\leq 2\%$
- ④ Essentially independent of operating temperature

## Electrical Characteristic Curves

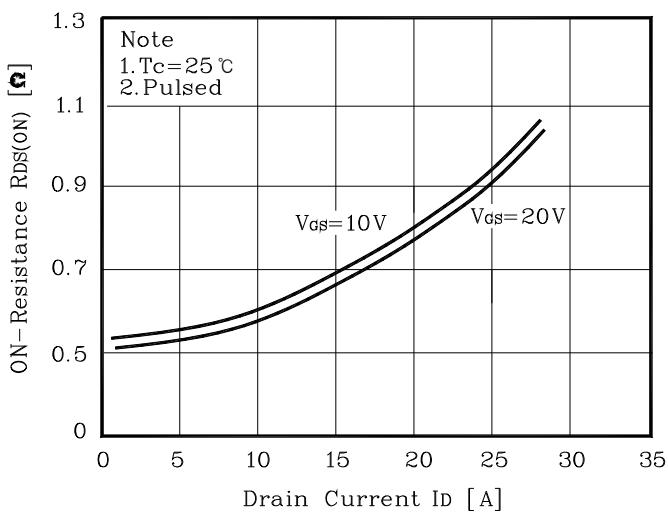
**Fig. 1**  $I_D$  -  $V_{DS}$



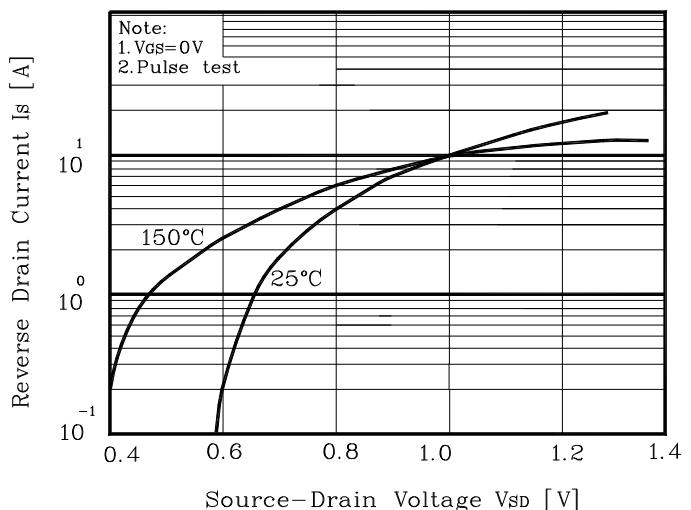
**Fig. 2**  $I_D$  -  $V_{GS}$



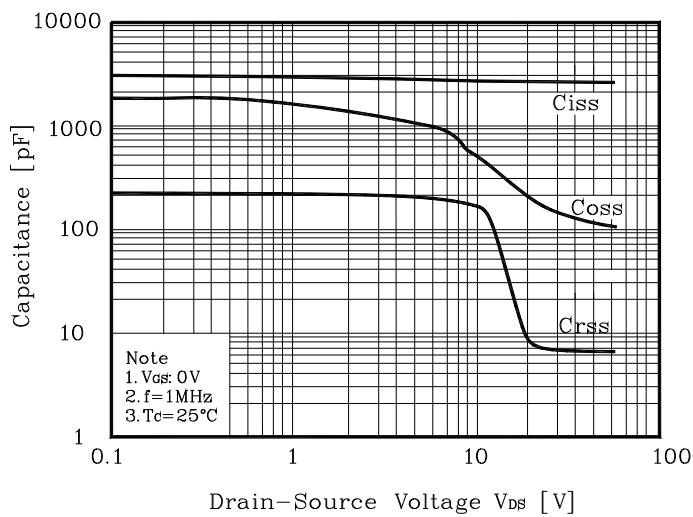
**Fig. 3**  $R_{DS(on)}$  -  $I_D$



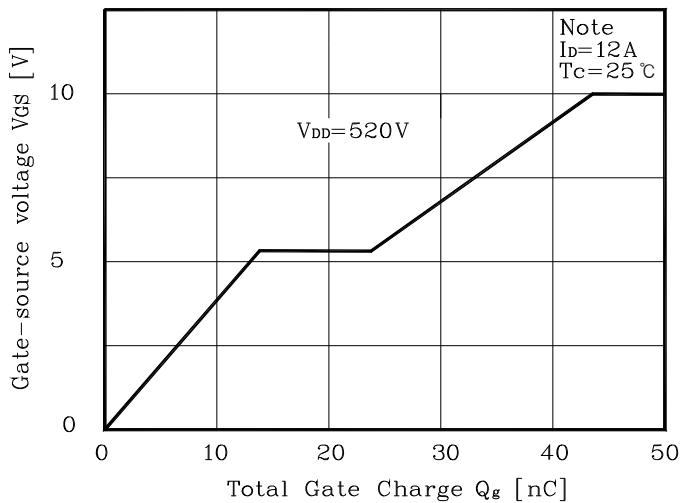
**Fig. 4**  $I_S$  -  $V_{SD}$



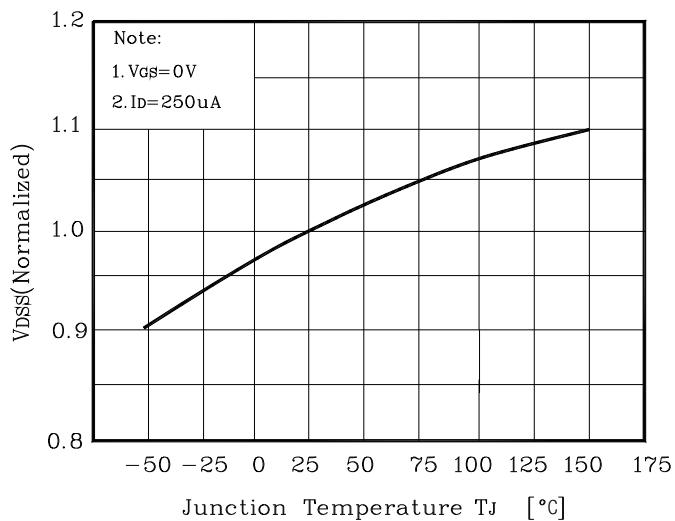
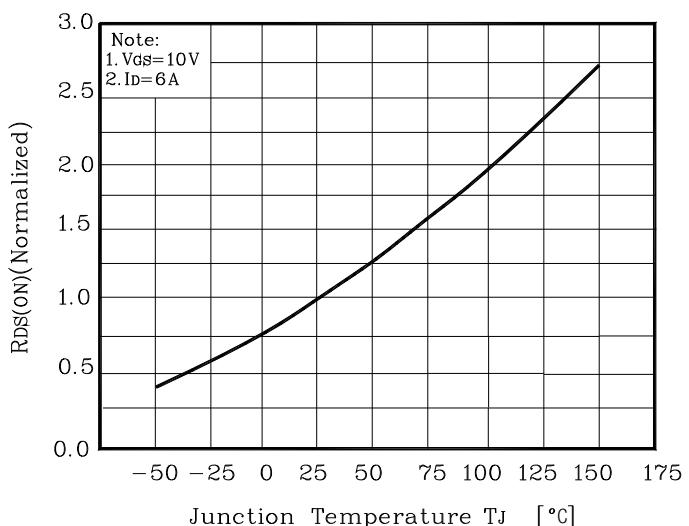
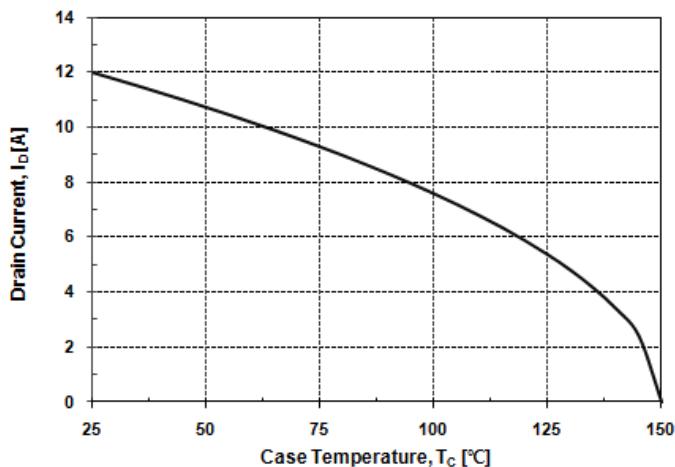
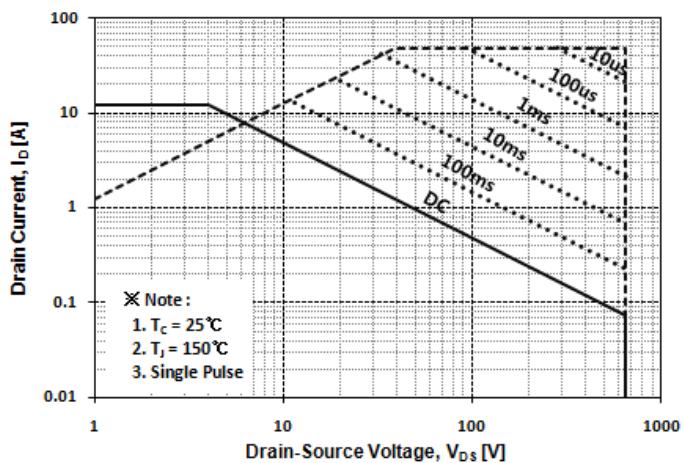
**Fig. 5** Capacitance -  $V_{DS}$



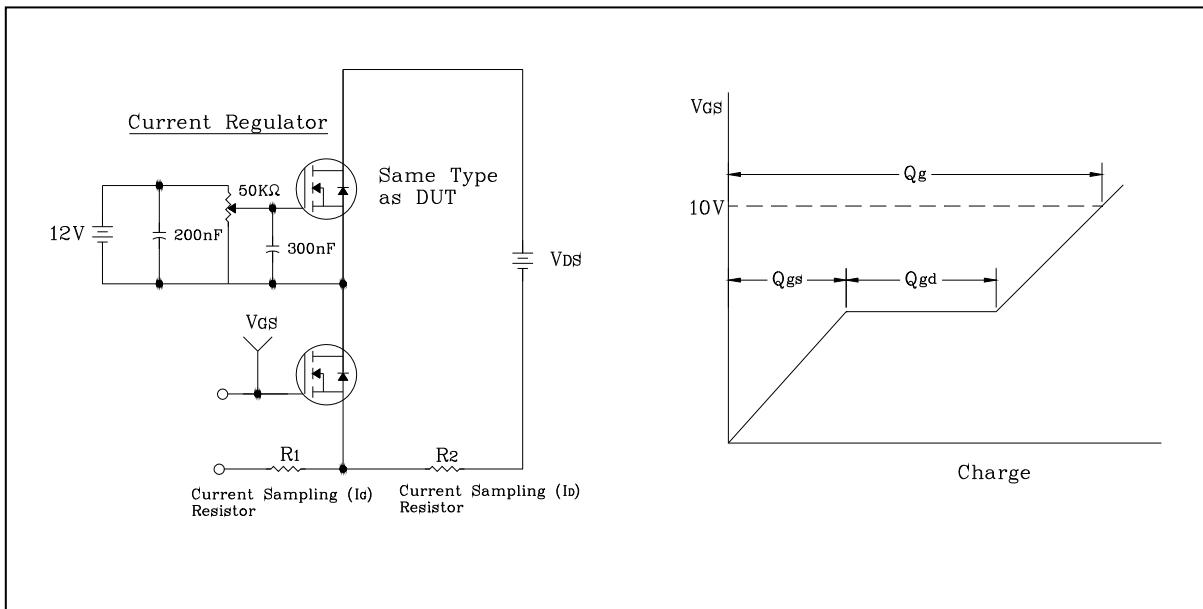
**Fig. 6**  $V_{GS}$  -  $Q_G$



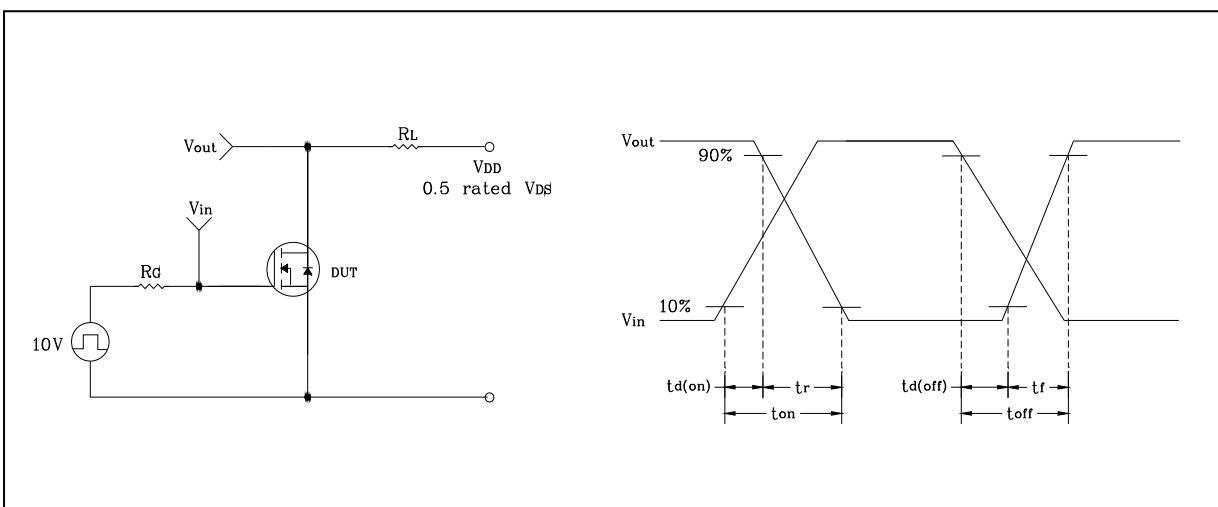
## Electrical Characteristic Curves

**Fig. 7  $V_{DSS}$  -  $T_J$** **Fig.8  $R_{DS(on)}$  -  $T_J$** **Fig. 9  $I_D$  -  $T_C$** **Fig. 10 Safe Operating Area**

**Fig. 11 Gate Charge Test Circuit & Waveform**



**Fig. 12 Resistive Switching Test Circuit & Waveform**



**Fig. 13 E<sub>AS</sub> Test Circuit & Waveform**

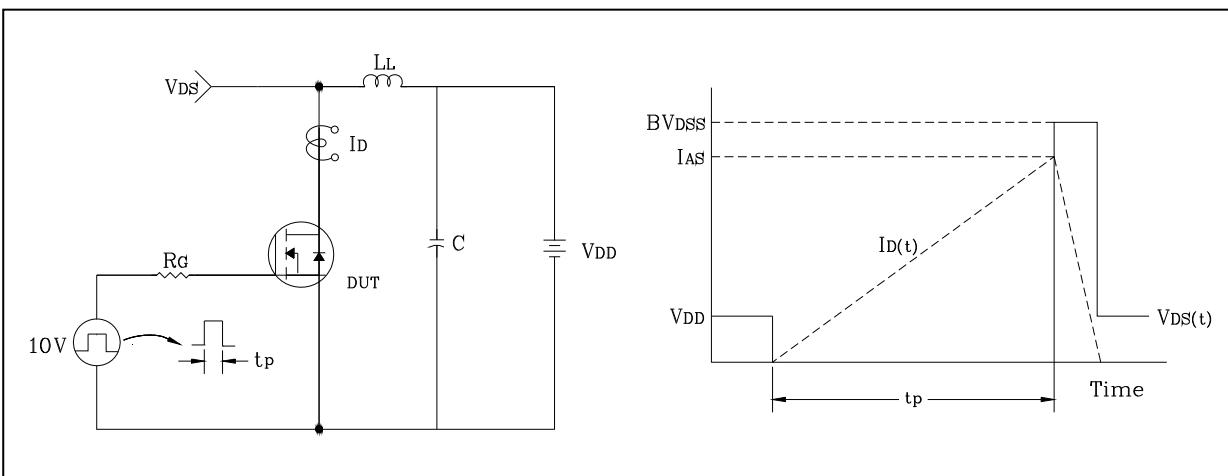
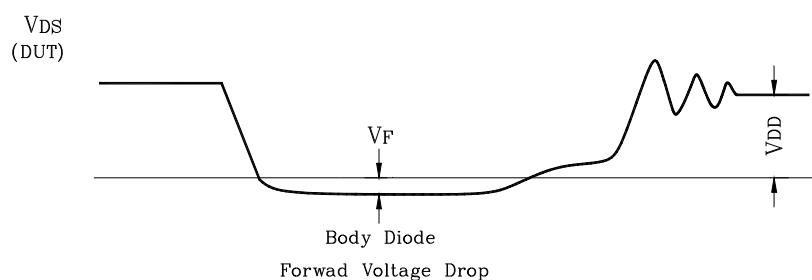
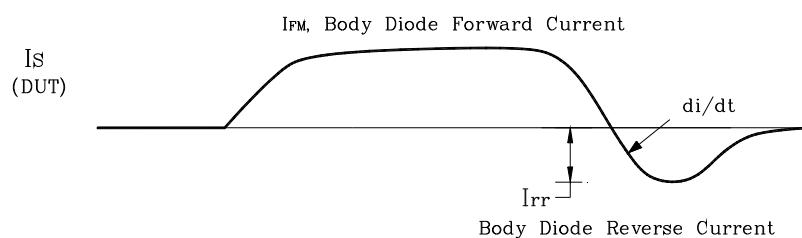
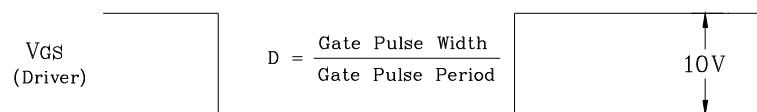
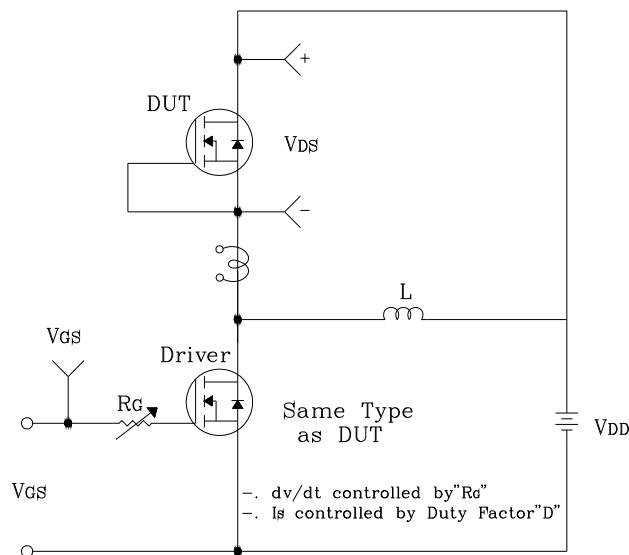
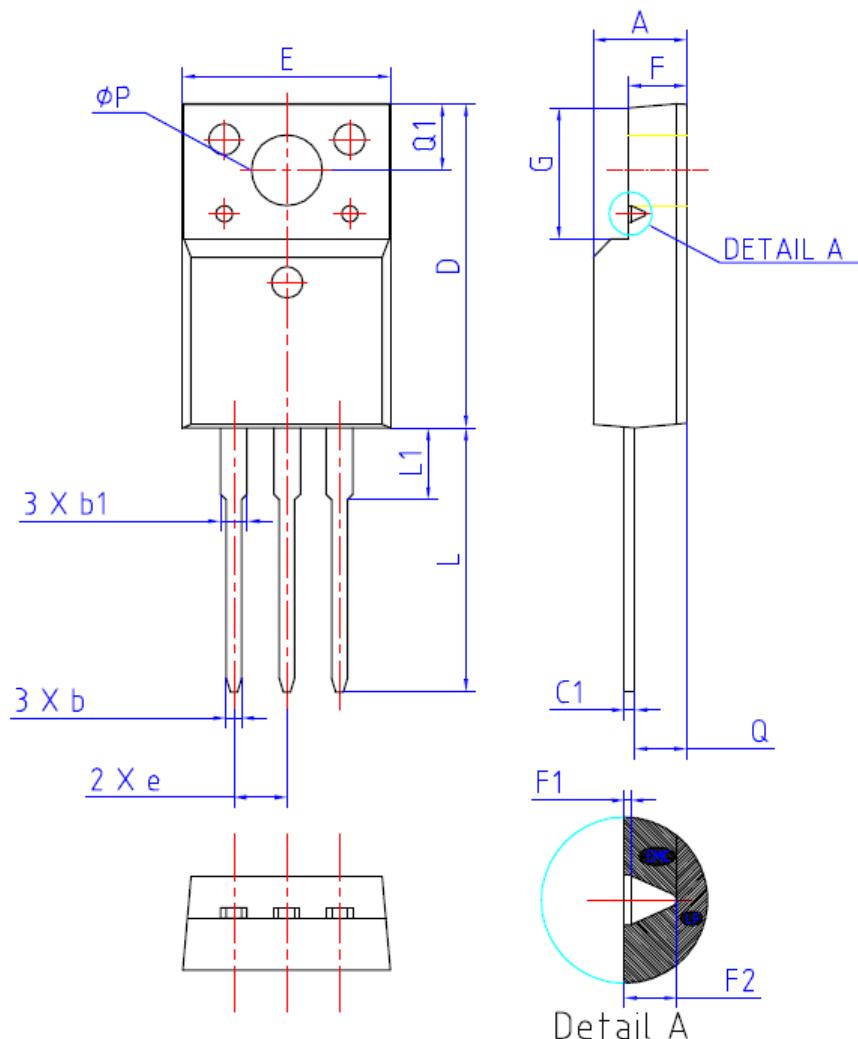


Fig. 14 Diode Reverse Recovery Time Test Circuit & Waveform



**Outline Dimension**

unit: mm



SYMBOL	MILLIMETERS			NOTE
	MINIMUM	NOMINAL	MAXIMUM	
A	4.50	4.70	4.90	
b	0.70	0.80	0.90	
b1	1.33	1.40	1.47	
C1	0.45	0.50	0.60	
D	15.67	15.87	16.07	
E	9.96	10.16	10.36	
e	2.54BSC			
F	2.34	2.54	2.74	
F1	(0.10 REF)			
F2	(0.84 REF)			
G	6.48	6.68	6.88	
L	12.78	12.98	13.18	
L1	3.03	3.23	3.43	
Q	2.56	2.76	2.96	
Q1	3.10	3.30	3.50	
ØP	3.08	3.18	3.28	

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