

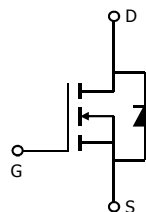
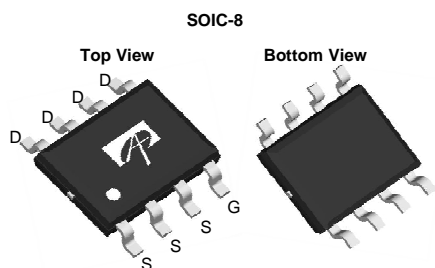
General Description

The AO4452 is fabricated with SDMOS™ trench technology that combines excellent $R_{DS(ON)}$ with low gate charge. The result is outstanding efficiency with controlled switching behavior. This universal technology is well suited for PWM, load switching and general purpose applications.

Product Summary

V_{DS}	100V
I_D (at $V_{GS}=10V$)	8A
$R_{DS(ON)}$ (at $V_{GS}=10V$)	< 25mΩ
$R_{DS(ON)}$ (at $V_{GS} = 7V$)	< 31mΩ

100% UIS Tested
 100% R_g Tested



Absolute Maximum Ratings $T_A=25^\circ C$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	±25	V
Continuous Drain Current	I_D	$T_A=25^\circ C$	8
		$T_A=70^\circ C$	6.5
Pulsed Drain Current ^C	I_{DM}	57	A
Avalanche Current ^C	I_{AR}	28	A
Repetitive avalanche energy $L=0.1mH$ ^C	E_{AR}	39	mJ
Power Dissipation ^B	P_D	$T_A=25^\circ C$	3.1
		$T_A=70^\circ C$	2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	31	40	°C/W
Maximum Junction-to-Ambient ^{A, D}		Steady-State	59	75
Maximum Junction-to-Lead	$R_{\theta JL}$	16	24	°C/W

Electrical Characteristics (T _J =25°C unless otherwise noted)						
Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =250μA, V _{GS} =0V	100			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =100V, V _{GS} =0V T _J =55°C			10 50	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±25V			100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =250μA	2	3.2	4	V
I _{D(ON)}	On state drain current	V _{GS} =10V, V _{DS} =5V	60			A
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =8A		20.5	25	mΩ
		T _J =125°C		36	43	
		V _{GS} =7V, I _D =6.5A		25	31	mΩ
g _{FS}	Forward Transconductance	V _{DS} =5V, I _D =8A		23		S
V _{SD}	Diode Forward Voltage	I _S =1A, V _{GS} =0V		0.66	1	V
I _S	Maximum Body-Diode Continuous Current				5	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =50V, f=1MHz	1400	1770	2200	pF
C _{oss}	Output Capacitance		115	165	215	pF
C _{riss}	Reverse Transfer Capacitance		33	55	80	pF
R _g	Gate resistance	V _{GS} =0V, V _{DS} =0V, f=1MHz	0.3	0.65	1.0	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =10V, V _{DS} =50V, I _D =8A	14	28	42	nC
Q _{gs}	Gate Source Charge		4	9	14	nC
Q _{gd}	Gate Drain Charge		6	10	14	nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =10V, V _{DS} =50V, R _L =6Ω, R _{GEN} =3Ω		12		ns
t _r	Turn-On Rise Time			4		ns
t _{D(off)}	Turn-Off DelayTime			17		ns
t _f	Turn-Off Fall Time			5		ns
t _{rr}	Body Diode Reverse Recovery Time	I _F =8A, dI/dt=500A/μs	11	16	21	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =8A, dI/dt=500A/μs	42	60	78	nC
t _{rr}	Body Diode Reverse Recovery Time	I _F =8A, dI/dt=100A/μs	21	27	33	ns
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =8A, dI/dt=100A/μs	20	28	36	nC

A. The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any given application depends on the user's specific board design.

B. The power dissipation P_D is based on T_{J(MAX)}=150° C, using ≤ 10s junction-to-ambient thermal resistance.

C. Repetitive rating, pulse width limited by junction temperature T_{J(MAX)}=150° C. Ratings are based on low frequency and duty cycles to keep initial T_J=25° C.

D. The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300μs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-ambient thermal impedance which is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, assuming a maximum junction temperature of T_{J(MAX)}=150° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

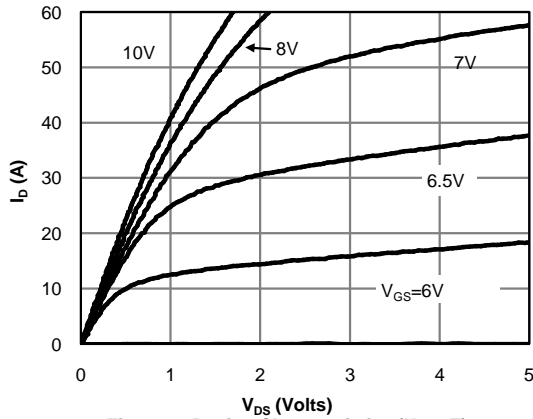


Figure 1: On-Region Characteristics (Note E)

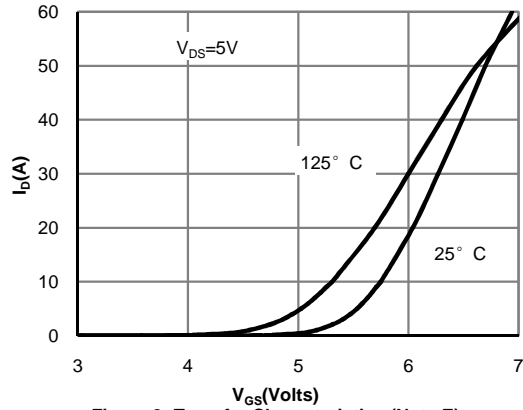


Figure 2: Transfer Characteristics (Note E)

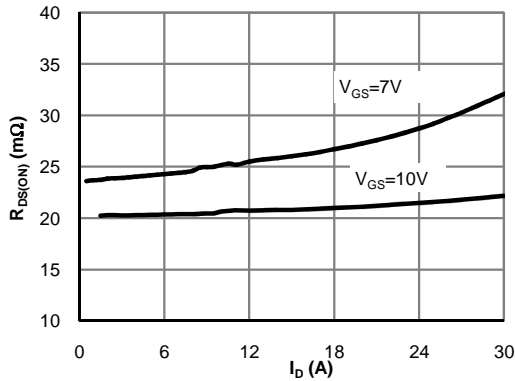


Figure 3: On-Resistance vs. Drain Current and Gate Voltage (Note E)

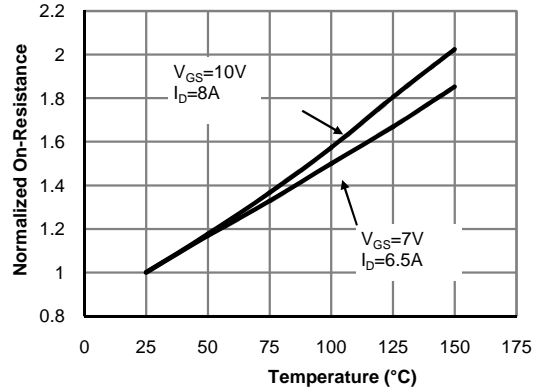


Figure 4: On-Resistance vs. Junction Temperature (Note E)

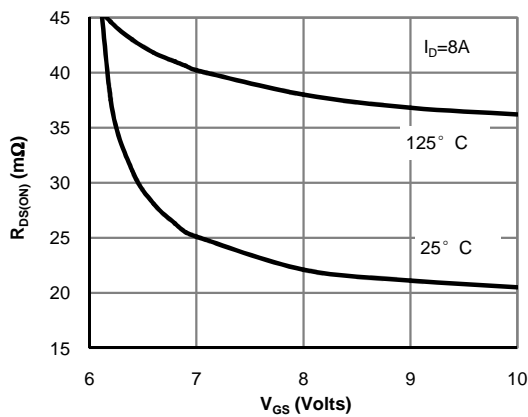


Figure 5: On-Resistance vs. Gate-Source Voltage (Note E)

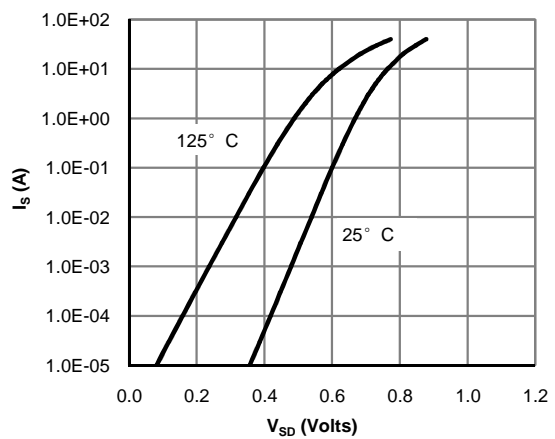


Figure 6: Body-Diode Characteristics (Note E)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

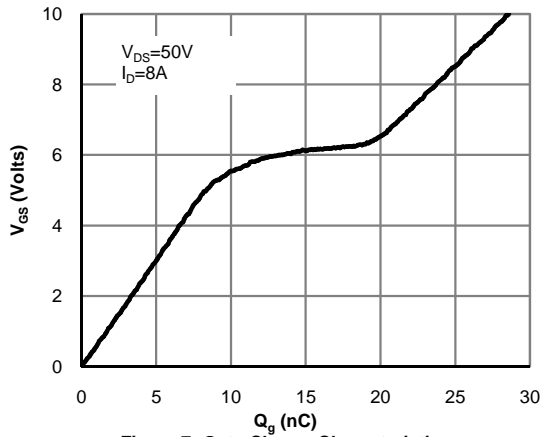


Figure 7: Gate-Charge Characteristics

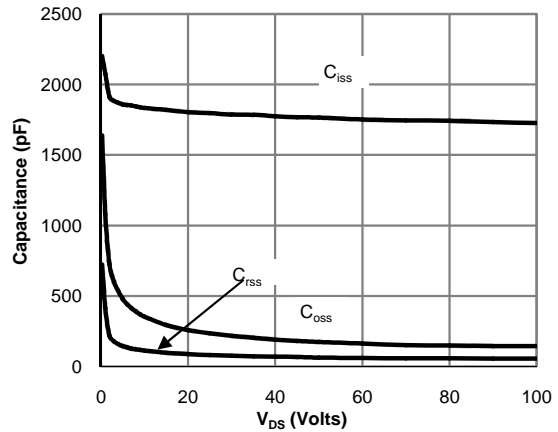


Figure 8: Capacitance Characteristics

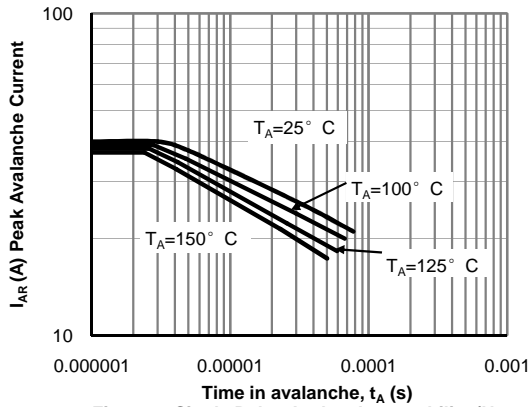


Figure 9: Single Pulse Avalanche capability (Note C)

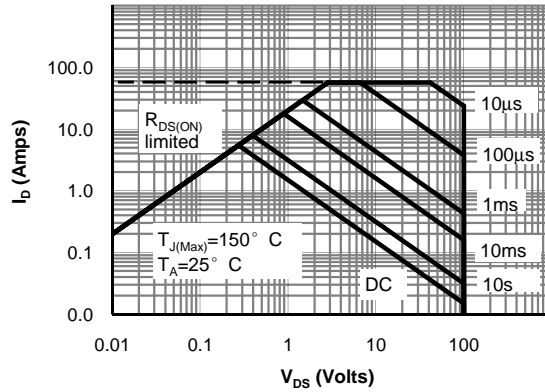


Figure 10: Maximum Forward Biased Safe Operating Area (Note F)

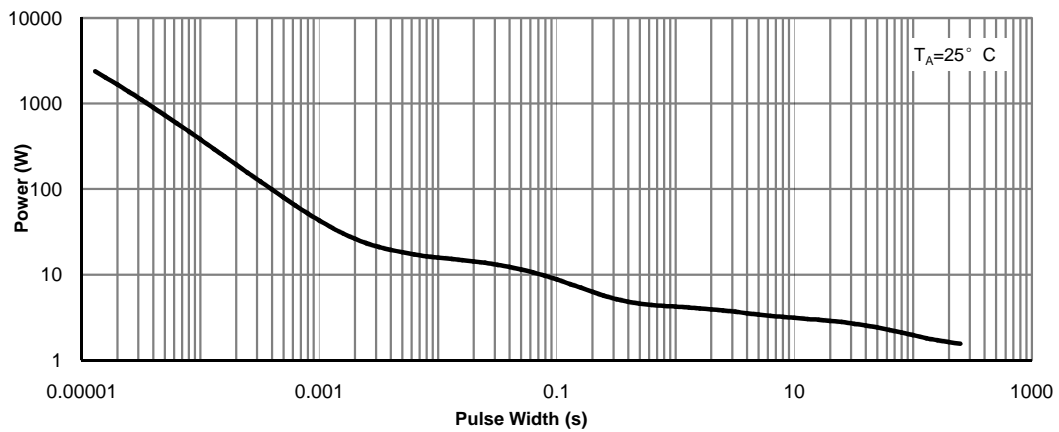


Figure 11: Single Pulse Power Rating Junction-to-Ambient (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

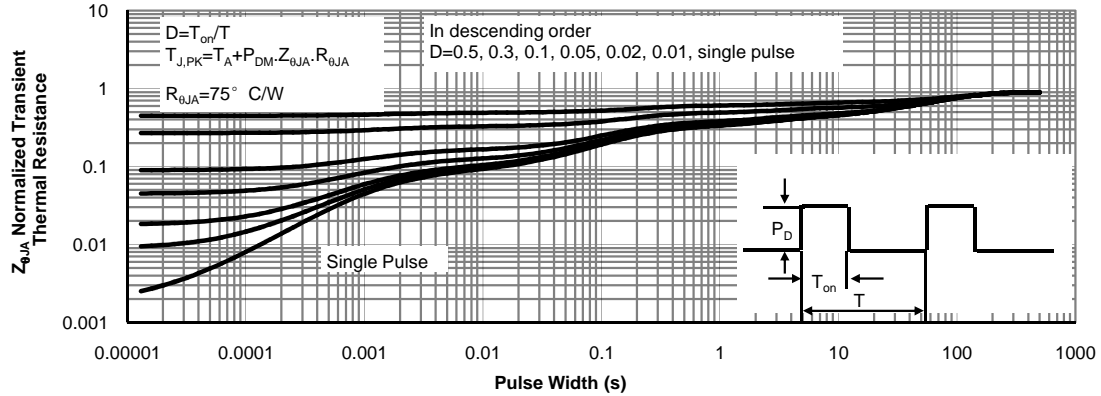


Figure 12: Normalized Maximum Transient Thermal Impedance (Note F)

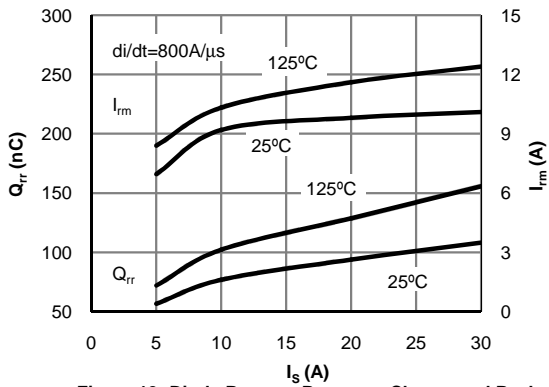


Figure 13: Diode Reverse Recovery Charge and Peak Current vs. Conduction Current

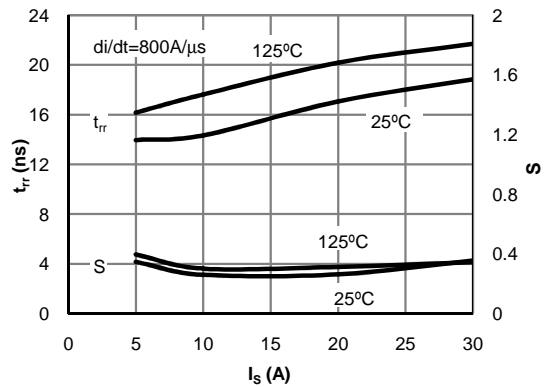


Figure 14: Diode Reverse Recovery Time and Softness Factor vs. Conduction Current

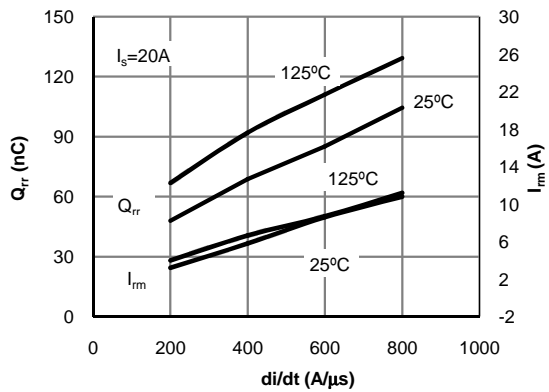


Figure 15: Diode Reverse Recovery Charge and Peak Current vs. di/dt

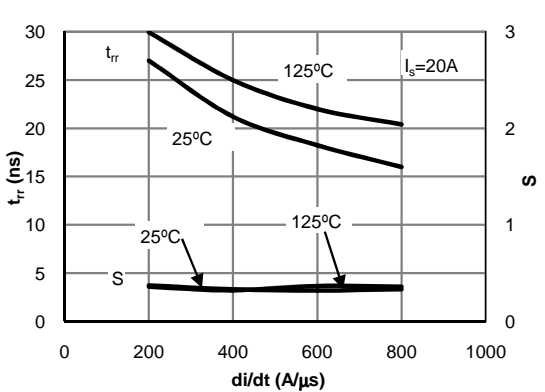
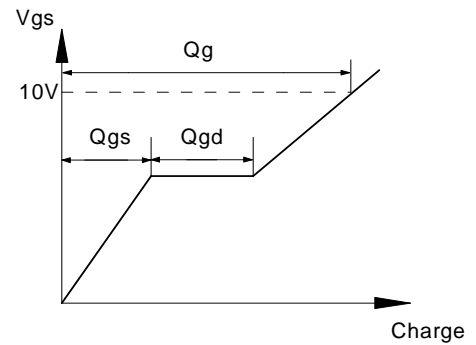
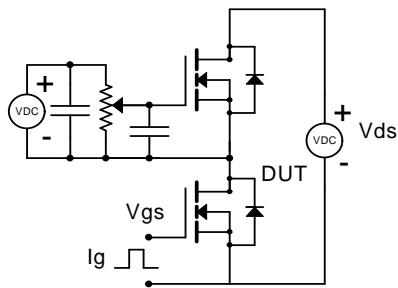
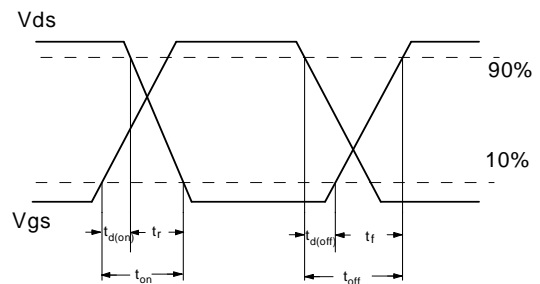
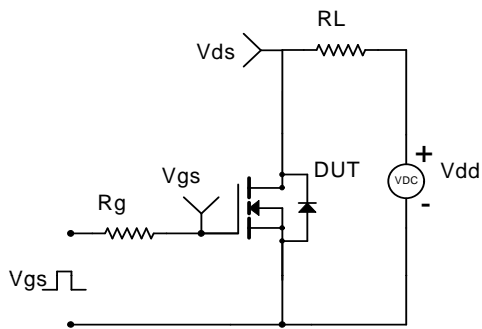


Figure 16: Diode Reverse Recovery Time and Softness Factor vs. di/dt

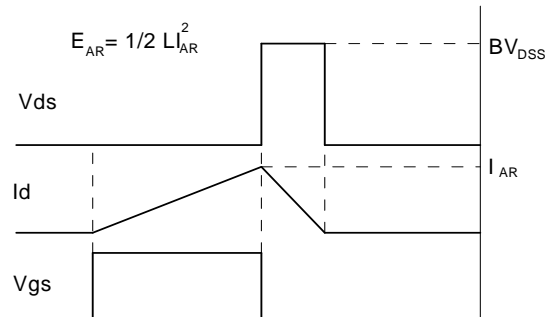
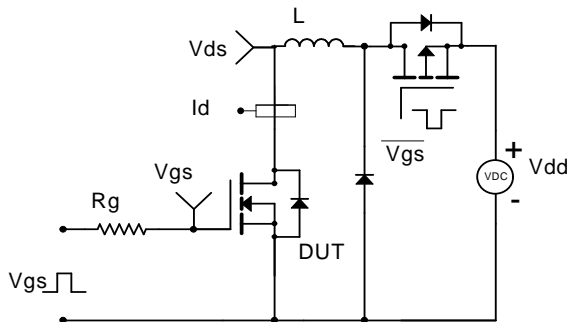
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms

