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S1C33L17

CMOS 32-bit Application Specific Controller

- **32-bit RISC CPU-Core Optimized for SoC (EPSON S1C33 PE)**
- **Dual AMBA Bus System for CPU and LCDC**
- **Built-in PLL (Multiplication rate: ×1 to ×16)**
- **Advanced CPU Instruction Queue Buffer**
- **Built-in 8KB RAM**
- **SDRAM Controller with Burst Control**
- **Generic DMA Controller (HSDMA/IDMA)**
- **4-ch. PWM Control Timer/Counter**
- **Supports Several Interfaces**
  SIO with FIFO (IrDA1.0, ISO7816-3), SPI, I^2S and USB
- **5-ch. ADC for Analog Input**
- **Built-in LCD Controller with 12KB IVRAM**
  Supports Up to QVGA (320 × 240) Display in 1 bpp Mode (black and white) by Single Chip
  Supports UMA VRAM
  Supports VGA (640 × 480) and 64K Color
- **NAND Flash Interface**
- **Provides 32-bit MAC API**

■ DESCRIPTIONS

The S1C33L17 is a high cost performance 32-bit RISC controller for specific applications that require a lot of general-purpose I/O, a powerful PWM Timer/Counter function, several serial interfaces including USB-FS device controller, an ADC and a LCD display system, such as middle range electronic dictionaries and educational products with voice/music playback function. The S1C33L17 consists of a 32-bit RISC CPU-Core, generic DMA controller, USB-FS device controller, PWM control Timer/Counter, several interfaces (SIO including IrDA1.0 and ISO7816-3 protocol, SPI and I^2S), ADC, RAM/Shared IVRAM, RTC and NAND Flash interface implemented by EPSON SoC design technology using 0.18 µm Mixed Analog Low CMOS Process.

■ FEATURES

● Technology

- 0.18 µm AL-4-Layers mixed analog low power CMOS process technology

● CPU

- EPSON original C33 PE 32-bit RISC CPU-Core with AMBA bus optimized for SoC
- Max. 66 MHz operation
- Internal 2-stage pipeline and 4 instruction queues
- Instruction set: 128 instructions (16-bit fixed length)
- Basic instructions are compatible with the S1C33 32-bit RISC Cores.
- Dual AMBA bus system for CPU and LCDC

● Internal Memories

- 8KB RAM
- 12KB IVRAM (used as general-purpose RAM, VRAM)
- 2KB DST RAM (used as general-purpose RAM or IDMA descriptor table RAM)

● Oscillator Circuit / PLL

OSC3 Oscillator Circuit

- Crystal oscillation: 5 MHz min. to 48 MHz max.
- Ceramic oscillation: 5 MHz min. to 48 MHz max.
- External clock input: 5 MHz min. to 48 MHz max

∗ A 48 MHz clock source with 0.25% of accuracy should be connected for using the USB function.
When using a ceramic resonator, please be sure to contact Murata Manufacturing Co., Ltd. for further information on conditions of use for ceramic resonators.

PLL

- PLL input frequency: 5 MHz min. to 50 MHz max.
- PLL output frequency: 25 MHz min. to 90 MHz max.
- Multiplication rate: ×1 to ×16

OSC1 Oscillator Circuit

- Crystal oscillation: 32.768 kHz typ.
- External clock input: 32.768 kHz typ.

● High Speed Bus (HB) Modules

SRAMC (SRAM Controller)

- 25-bit address lines and 8/16-bit selectable data bus
- UP to a 32M-byte (A[24:0]) address space is provided for each chip enable signal.
- Max. 8 chip enable signals are available to connect external devices.
- Programmable bus wait cycle (0 to 7 cycles)
- Supports external wait signals.
- 4GB physical address space is available.
  - The physical address space is divided into 23 areas
  - Areas 0 to 3 and Area 6 are system reserved.
- Supports only Little-Endian access to each area.
- Memory mapped I/O
- Supports both A0 and BS (Bus Strobe) access type external devices.
- SRAM, ROM, and Flash ROM direct access interfaces are built in.

SDRAMC (SDRAM Controller with SDRAM APP and AHB Local Bus Arbiter)

- Supports SDRAM direct interface.
- Supports only SDRAM devices with 16-bit data bus.
  - Minimum configuration: 16M bits (2MB), 16-bit SDRAM × 1
  - Maximum configuration: 512M bits (64MB), 16-bit SDRAM × 1
- CAS latency: 1, 2, or 3 programmable
- Supports burst and single read/write.
- Supports DQM (byte write) function.
- Supports max. 4 SDRAM banks and bank active mode.
- Incorporates a 12-bit auto-refresh counter.
- Intelligent self-refresh function for low power operation
- 2-stage × 32-bit data buffer and 8-stage × 32-bit × 2-slot instruction buffer built-in
- Supports up to max. 90 MHz SDRAM clock.
  - When the CPU clock is 48 MHz, the SDRAM clock can be set to max. 48 MHz.
  - When the CPU clock is 45 MHz, the SDRAM clock can be set to max. 90 MHz using the PLL.
- Arbitrates ownership of the external bus between the CPU, DMAC, LCDC and SRAMC.

DMAC (Direct Memory Access Controller)

- 4-ch. high speed hardware DMA
- 128-ch. intelligent DMA (variable data transfer controller) with specific control table

IVRAMARB (Internal Video RAM Arbiter)

- Contains a 12KB SRAM (3,072 words × 16 bits × 2).
- Arbitrates accesses from the LCDC and CPU.
- Allows the CPU and LCDC to access IVRAM in minimum 2 cycles by 32-bit access.
- Supports UMA (Unified Memory Access) for display.
- IVRAM is configurable as a 12KB general-purpose RAM in Area 0 using a control register if it is not used as a video RAM.

● Peripheral Bus (SAPB) Modules

TCU (Timer/Counter Unit with PWM Outputs)

- 4-ch. 16-bit timer/counter
- Supports PWM outputs with DA16 (Digital D/A) mode.
- Contains a prescaler, which can divide the peripheral clock by 1 to 4,096, to generate the operating clock for each channel.
- Possible to invoke DMA transfer.

WDT (Watchdog Timer)
- 30-bit watchdog timer to generate an NMI interrupt
- The watchdog timer overflow cycle (NMI interrupt cycle) is programmable.
- The watchdog timer overflow signal can be output outside the IC.

ADC (A/D Converter)
- 5-ch. 10-bit A/D converter
- Upper/lower limit interrupt is available.
- Each ADC channel includes a data buffer.
- Contains a prescaler, which can divide the peripheral clock by 2 to 256, to generate the operating clock for ADC.

ITC (Interrupt Controller)
- Possible to invoke DMA transfer
- DMAC interrupt: 5 types
- Input interrupt: 18 types
- TCU interrupt: 8 types
- EFSIO interrupt: 9 types
- ADC interrupt: 2 types
- RTC interrupt: 1 type
- SPI interrupt: 3 types
- USB interrupt: 2 types
- I^2S interrupt: 1 type
- LCDC interrupt: 1 type

GPIO (General-Purpose I/O Ports)
- Max. 82 ports in the QFP24-144pin model.
  ∗ The S1C33L17 GPIO ports are shared with other peripheral function pins (EFSIO, PWM etc.). Therefore, the number of GPIO ports depends on the peripheral functions used.

USB (Universal Serial Bus 2.0 compliant Full-Speed Device Controller)
- Supports USB2.0 full speed (12M bps) mode.
- Supports auto negotiation function.
- Supports control, bulk, isochronous and interrupt transfers.
- Supports 4 general-purpose end points and end point 0 (control).
- Embedded 1K-byte programmable FIFO
- Supports 8-bit local bus DMA port.
- Possible to invoke DMA transfer.
- Supports Async. DMA transfer.
- Supports DMA slave mode.
- Fixed 48 MHz clock for USB-FS.
- Supports snooze mode.

RTC (Real Time Clock)
- Contains time counters (seconds, minutes, and hours) and calendar counters (days, days of the week, months, and year).
- BCD data can be read from and written to both counters.
- Capable of controlling the starting and stopping of time clocks.
- 24-hour or 12-hour mode can be selected.
- A 30-second correction function can be implemented in software.
- Periodic interrupts are possible.

CARD (Serial Input/Output with Direction Control)
- Provides SmartMedia I/F signals (#SMRE, #SMWE).
- Provides 8-bit NAND Flash I/F signals.

EFSIO (Extended Serial Interface with FIFO Buffer)
- 3-ch. clock sync./async. serial interface (Ch.2 supports only async.)
- Contains FIFO data buffers.
  - Ch.0, 1: 4-byte receive data buffer and 2-byte transmit data buffer are available.
  - Ch.2: 2-byte receive data buffer and 1-byte transmit data buffer are available.

- Supports IrDA1.0 interface (only Ch.0 and Ch.1).
- Contains a baud-rate generator (12-bit programmable timer).
- Ch.1 only supports ISO7816 mode.
  - Alternative MSB or LSB
  - Memory card interface compatible with ISO7816-3 T=0 & T=1 protocol
  - Programmable baud-rate and guard-time generation
  - ISO7816 acknowledge and automatically repeat transmission
- Possible to invoke DMA transfer.

SPI (Serial Peripheral Interface)

- 1 ch. SPI that operates in either master or slave mode.
- Supports 1- to 32-bit data transfer.
- Data transfer timing (clock phase and polarity variations) is selectable from among 4 types.
- A 1 to 65,536 clocks of delay can be inserted between transfers.
- Generates transmit data register empty and receive data register full interrupts.
- Supports card medias such as MMC.
- Possible to invoke DMA transfer.

EGPIO (Extended GPIO)

- Max. 17 configurable GPIO ports are available in addition to the standard GPIO ports. In die form, max. 91 ports are available.
  * The EGPIO ports are shared with other peripheral function pins. Therefore, the number of EGPIO ports depends on the peripheral functions used.
- Most ports have a pull-up resistor that can be enabled/disabled with the control register.
- Possible to drive the ports low.

CMU (Extended Clock Management Unit)

- Controls clock supply to each peripheral module (static).
- Manages reset and NMI inputs.
- Switches the system clock source (MCLK, SDRAMCLK, or RTCCLK).
- Controls the MCLK and RTCCLK oscillator circuits.
- Turns on/off and controls frequency multiplication rate of the PLL.
- Controls clocks according to the standby mode (SLEEP and HALT).
- Controls divide ratios of the LCDC clock.
- Manages the external bus clock.

MISC (Misc. Setting Register)

- USB/RTC wait configuration registers
- Supports pull-up and low-drive control for each signals.

I^2S (Inter-IC Sound Bus Interface)

- 16-bit/24-bit resolution selectable for input/output channels
- I^2S master clock is software selectable from either internal or external clock.
- Supports stereo, mono (L and R) and mute output mode.
- Clock polarity is software configurable.
- Data shift direction (MSB first/LSB first) is software selectable.
- Issues I^2S interrupt requests and DMA requests.
- Contains a 24 bits $\times$2 ch. $\times$4 of transmit FIFO.

LCDC (STN/TFT LCD Controller with AMBA Bus)

VRAM:

- Built-in a 12KB RAM usable as a display buffer or general-purpose RAM (register selectable)
- Supports the UMA method allowing LCDC to access SDRAM (external VRAM) or IVRAM (internal VRAM).
- The external VRAM map (SDRAM) is configurable.
- The sub window area can be located in IVRAM or external VRAM regardless of whether it contains the main window area or not.

Display Support:

- 4- or 8-bit monochrome LCD interface
- 4- or 8-bit color LCD interface
- Single-panel, single-drive passive displays

- 12/16-bit Generic HR-TFT interface
- Typical resolutions
  - 320 × 240 (1-bpp mode, external VRAM is required) bpp = bits per pixel
  - 640 × 480 (16-bpp mode)

  * Note that the panel width must be a multiple of 16 ÷ bits per pixel.

Display Modes:

- Due to frame rate modulation, grayscale display is possible in up to 16 shades of gray when a monochrome passive LCD panel is used.
  - Two-shade display in 1-bpp mode
  - Four-shade display in 2-bpp mode
  - 16-shade display in 4-bpp mode
- A maximum of 64K colors can be simultaneously displayed on a color passive LCD panel.
  - 256-color display in 8-bpp mode
  - 4K-color display in 12-bpp mode
  - 64K-color display in 16-bpp mode
- A maximum of 65,535 colors can be simultaneously displayed on a TFT panel.
  - Two-color display in 1-bpp mode
  - Four-color display in 2-bpp mode
  - 16-color display in 4-bpp mode
  - 256-color display in 8-bpp mode
  - 4K-color display in 12-bpp mode
  - 64K-color display in 16-bpp mode
- The look up table can be bypassed

Display Features:

- Picture-in-Picture Plus (PIP+)
  Picture-in-Picture Plus enables a secondary window (or sub-window) within the main display window. The sub-window may be positioned anywhere within the main window and is controlled through registers. The sub-window retains the same color depth as the main window. The speed of generating a sub-window by hardware is faster than software. By using this PIP+ function, it can greatly speed the GUI performance and CPU can have more performance to assign other processing. (e.g. Voice etc.)
- 12/16-bit Generic HR-TFT I/F
  The 12/16-bit Generic HR-TFT interface supports HR-TFT and TFT panels up to VGA (640 × 480) or QVGA (320 × 240). Because the timing of FPFRAM, FPLINE, and TFT_CTL0–3 are not fixed for TFT panels, they can be controlled by register setting. By different register settings, you can get your specified TFT I/F signal timing.
- Clock source
  The LCDC clock can be internally divided 48 MHz by 1 to 16. The clock division register is located in CMU part.

● Operating Voltage

- V_{DD} (Core): 1.70 to 1.90 V (typ. 1.8 V) when a ceramic resonator is used for the USB clock
- V_{DD} (Core): 1.65 to 1.95 V (typ. 1.8 V) when a crystal is used or an external clock is input
- PLV_{DD}: 1.65 to 1.95 V (typ. 1.8 V)
- V_{DDH} (I/O): 2.70 to 3.60 V when the USB is not used (5-V tolerant I/O not supported)
- V_{DDH} (I/O): 3.00 to 3.60 V (typ. 3.3 V) when the USB is used (5-V tolerant I/O not supported)

● Operating Frequency

- CPU: 66 MHz max.
- USB: 48 MHz fixed
- SDRAMC: 90 MHz max.
- LCDC: 66 MHz max.
- Other peripheral circuits: 66 MHz max.

● Operating Temperatures

- -40 to 85°C (0 to 75°C when a ceramic resonator is used for the USB clock)

● Current Consumption

- During SLEEP: 0.3 µA (typ.)
- During HALT: 3.2 mA (typ.)
- During execution: 22.0 mA (typ.)

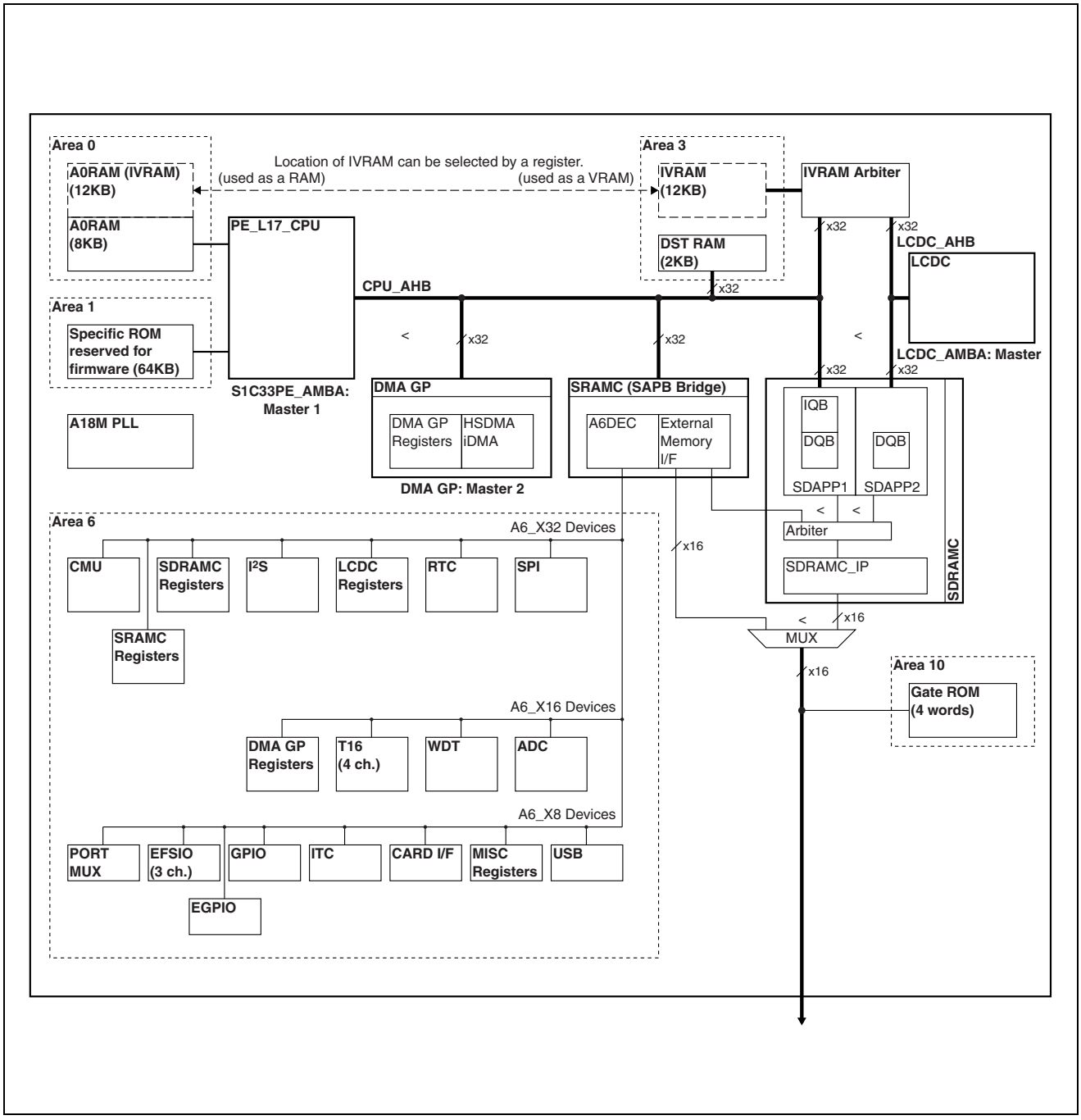
∗ When MCLK = 48 MHz and SDCLK = 48 MHz

By controlling the CPU clock through the Clock-Gear (CMU), current consumption can be reduced.

● Shipping Form

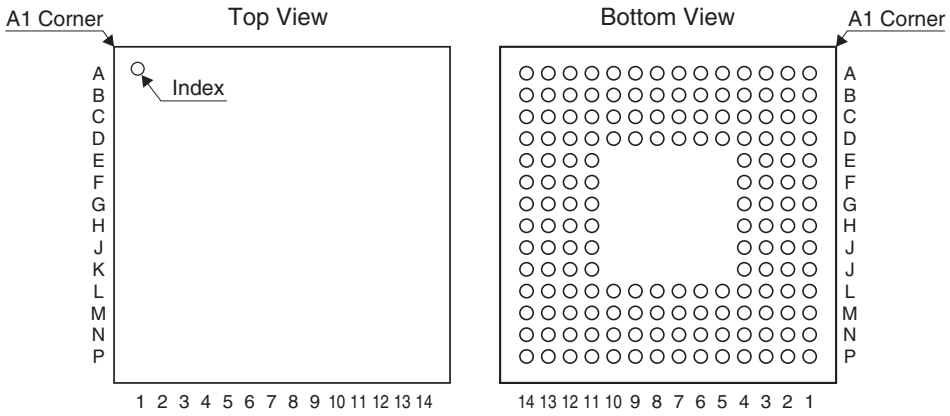
- Package: QFP24-144pin (16 mm × 16 mm × 1.0 mm and 0.4 mm pin pitch)
  PFBGA-180pin (12 mm × 12 mm × 1.2 mm and 0.8 mm ball pitch)
- Chip: 168 pads with pad pitch 90 µm

■ BLOCK DIAGRAM



■ PIN LAYOUT DIAGRAM

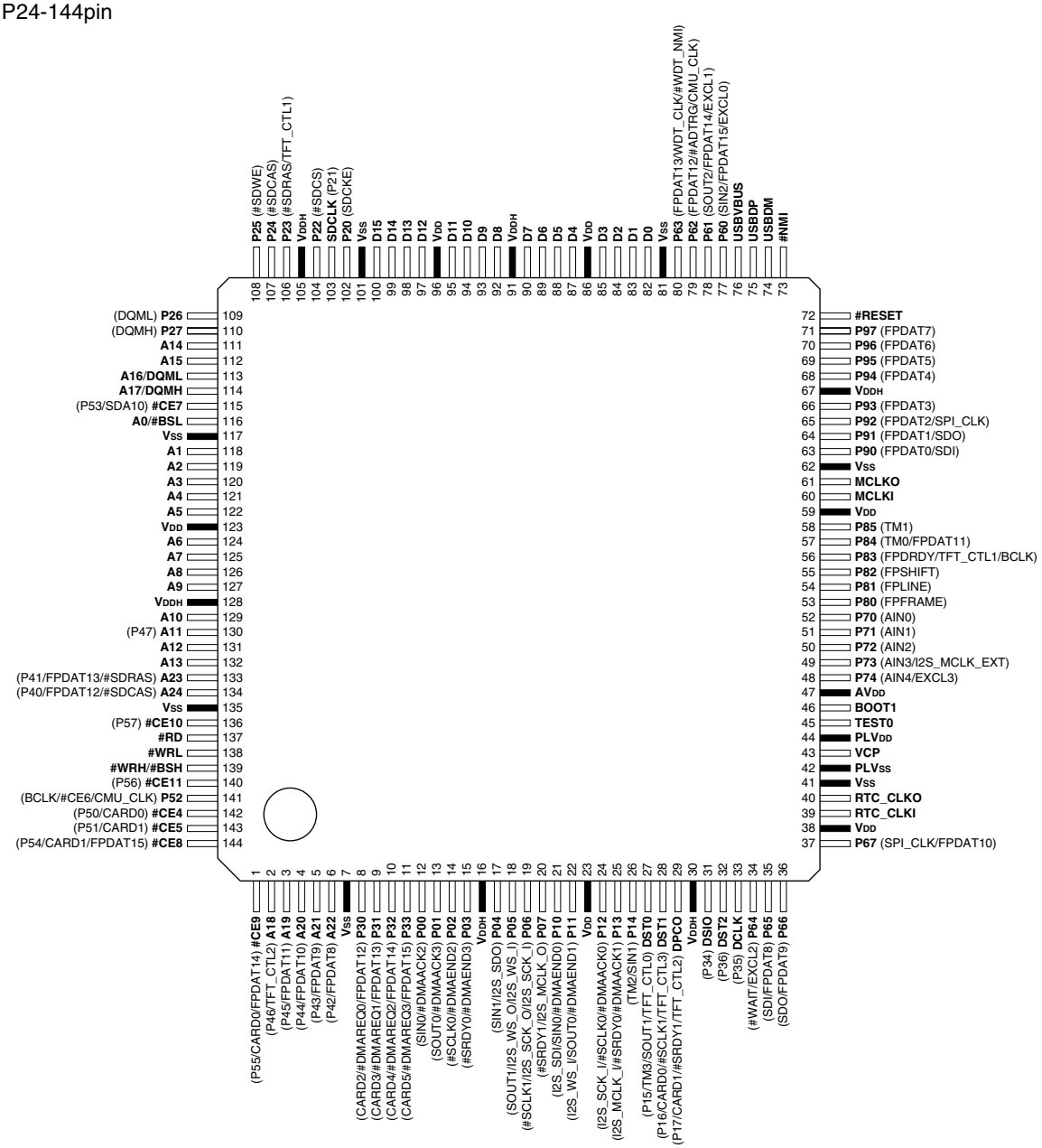
PFBGA-180pin



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	N.C.	**#CE8** P54 CARD1 FPDAT15	**#CE4** P50 CARD0	**#CE11** P56	**#RD**	**A23** P41 FPDAT13 #SDRAS	**A11** P47	**A8**	**A4**	**#CE7** P53 SDA10	**A15**	**A14**	**P26** DQML	N.C.	A
B	**A18** P46 TFT_CTL2	**#CE9** P55 CARD0 FPDAT14	**#CE5** P51 CARD1	**#WRH/** **#BSH**	**#CE10** P57	**A13**	**A10**	**A6**	**A2**	**A17/** **DQMH**	**A0/** **#BSL**	**P27** DQMH	**P25** #SDWE	**P24** #SDCAS	B
C	**A22** P42 FPDAT8	**A20** P44 FPDAT10	**A21** P43 FPDAT9	**P52** BCLK #CE6 CMU_CLK	**#WRL**	**A24** P40 FPDAT12 #SDCAS	**A12**	**A9**	**A3**	**A1**	**A16/** **DQML**	**D14**	**P23** #SDRAS TFT_CTL1	**P22** #SDCS	C
D	**P30** CARD2 #DMAREQ0 FPDAT12	**A19** P45 FPDAT11	**P31** CARD3 #DMAREQ1 FPDAT13	**VSS**	**VSS**	**VSS**	**VDD**	**VDDH**	**A7**	**A5**	**VSS**	**D13**	**P20** SDCKE	**SDCLK** P21	D
E	**P33** CARD5 #DMAREQ3 FPDAT15	**P00** SIN0 #DMAACK2	**P02** #SCLK0 #DMAEND2	**P32** CARD4 #DMAREQ2 FPDAT14	**VSS**	**VDD**	**VDD**	**VDDH**	**VDDH**	**VSS**	**VSS**	**D10**	**D12**	**D15**	E
F	**P03** #SRDY0 #DMAEND3	**P01** SOUT0 #DMAACK3	**P05** SOUT1 I2S_WS_O I2S_WS_I	**VDDH**	**VDDH**					**VDD**	**VDD**	**D11**	**D9**	**D8**	F
G	**P06** #SCLK1 I2S_SCK_O I2S_SCK_I	**P04** SIN1 I2S_SDO	**P07** #SRDY1 I2S_MCLK_O	**VDD**	**VDDH**					**VDDH**	**VDD**	**D5**	**D7**	**D6**	G
H	**P10** I2S_SDI SIN0 #DMAEND0	**P11** I2S_WS_I SOUT0 #DMAEND1	**P14** TM2 SIN1	**VDD**	**VDD**					**VDDH**	**VDDH**	**D2**	**D3**	**D4**	H
J	**DST0** P15 TM3 SOUT1 TFT_CTL0	**P13** I2S_MCLK_I #SRDY0 #DMAACK1	**DST1** P16 CARD0 #SCLK1 TFT_CTL3	**P12** I2S_SCK_I #SCLK0 #DMAACK0	**VSS**					**VSS**	**VSS**	**P62** FPDAT12 #ADTRG CMU_CLK	**D0**	**D1**	J
K	**DSIO** P34	**DPCO** P17 CARD1 #SRDY1 TFT_CTL2	**P64** #WAIT EXCL2	**DST2** P36	**VSS**	**VSS**	**VDD**	**VDDH**	**VDDH**	**VSS**	**VSS**	**P61** SOUT2 FPDAT14 EXCL1	**BOOT0**	**P63** FPDAT13 WDT_CLK #WDT_NMI	K
L	**DCLK** P35	**PB0** FPDAT12 I2S_SDO CARD2	**PB2** FPDAT14 I2S_SCK CARD4	**PB1** FPDAT13 I2S_WS_O CARD3	**BOOT1**	**P81** FPLINE	**P82** FPSHIFT	**P84** TM0 FPDAT11	**VDDH**	**P90** FPDAT0 SDI	**P91** FPDAT1 SDO	**PA2** FPDAT9 TFT_CTL1 I2S_SCK_I	**P60** SIN2 FPDAT15 EXCL0	**USBVBUS**	L
M	**PB3** FPDAT15 I2S_MCLK_O CARD5	**P65** SDI FPDAT8	**P66** SDO FPDAT9	**TEST0**	**P73** AIN3 I2S_MCLK_EXT	**P71** AIN1	**P83** FPDRDY TFT_CTL1 BCLK	**P85** TM1	**BURNIN**	**P93** FPDAT3	**P94** FPDAT4	**P97** FPDAT7	**#NMI**	**USBDP**	M
N	**P67** SPI_CLK FPDAT10	**VDD**	**VSS**	**VCP**	**P74** AIN4 EXCL3	**P70** AIN0	**P72** AIN2	**VDD**	**VSS**	**P95** FPDAT5	**PA1** FPDAT8 TFT_CTL0 I2S_WS_I	**P96** FPDAT6	**#RESET**	**USBDM**	N
P	N.C.	**RTC_CLKI**	**RTC_CLKO**	**PLVSS**	**PLVDD**	**AVDD**	**P80** FPFRAME	**MCLKI**	**MCLKO**	**P92** FPDAT2 SPI_CLK	**PA0** TFT_CTL0 I2S_SDI	**PA3** FPDAT10 TFT_CTL2 I2S_MCLK_I	**PA4** FPDAT11 TFT_CTL3 I2S_MCLK_EXT	N.C.	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Top View

QFP24-144pin



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