LD1022

16 Channel Constant Current LED Driver

Ver. 1.0 / Mar. 2009

LDT Inc. Mplaza 3F, 538, Dujeong-dong, Seobuk-gu, Cheonan, Chungnam, 331-958, Korea
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LD1022 Revision History

Version	Contents	Transfer Date
1.0	- First Version	2009.03.05

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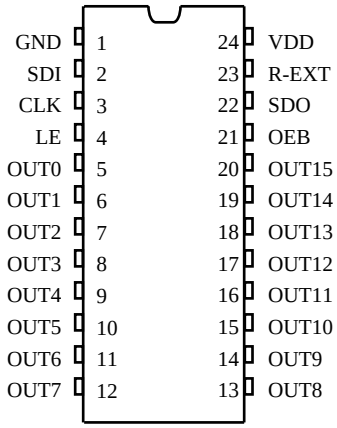
DESCRIPTION

LD1022 is designed for LED displays with output current gain control. LD1022 contains a serial buffer and data latches, which convert serial input data into parallel output format. At LD1022 output stage, sixteen regulated current ports are designed to provide constant current sinks for driving LEDs within a wide range of Vf variations.

FEATURES

- **16 constant current output channels**
- **Constant current output range: 5mA ~ 70mA**
- **Output current adjustable through an external resistor**
- **8-bit programmable output current control**
- **Output current accuracy:**
  - **between channels: ±1.0% (25mA < Iout < 70mA)**
    ±1.3% (3mA < Iout < 24mA)
  - **between ICs : ±3.0%**
- **25MHz clock frequency**
- **Fast response of output current, Pulse width: 50nS**
- **3V ~ 5V supply voltage**
- **Pb-free Package: SSOP24 (150) with two kinds of pin assignments**

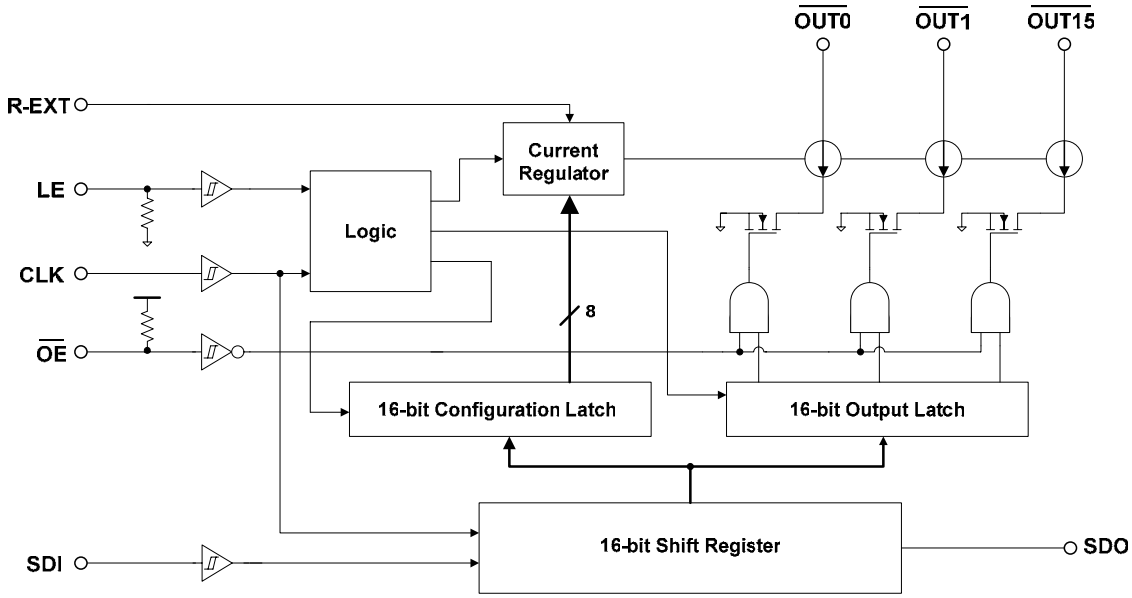
PIN CONNECTION (TOP VIEW)



ORDERING INFORMATION

PART NUMBER	PACKAGE	TA
LD1022-SS	24 SSOP	-40°C to 85 °C
LD1022-SP	24 SOP	-40°C to 85 °C

BLOCK DIAGRAM



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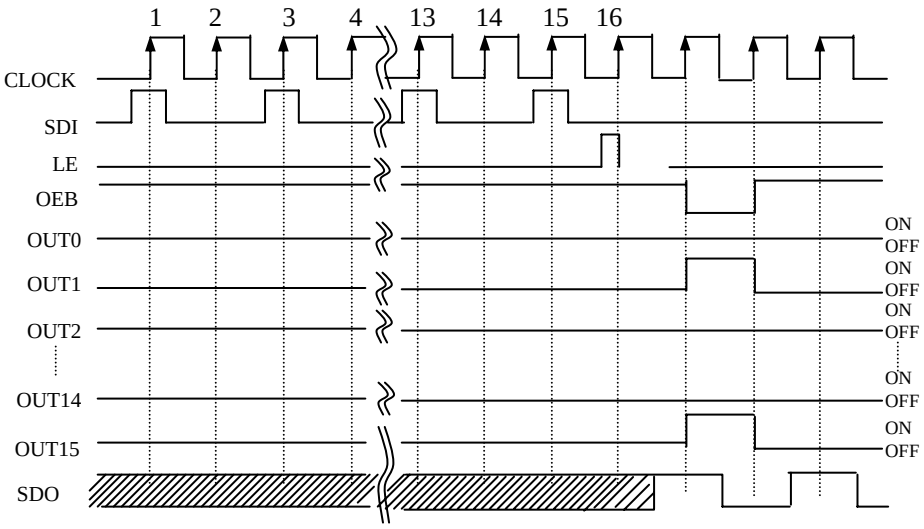
TIMING DIAGRAM



NORMAL MODE TRUTH TABLE

CLK	LE	OE	SDI	OUT0 … OUT7 … OUT15	SDO
↑§	H	L	D_n	Dn …Dn-7 ... Dn-15	D_{n-15} Φ
X	L	L	D_{n+1}	No change	D_{n-14} Φ
↑§	H	L	D_{n+2}	Dn+2 …Dn-5 ... Dn-13	D_{n-13} Φ
X	X¥	L	D_{n+3}	Dn+2 …Dn-5 ... Dn-13	D_{n-13}
X	X¥	H	D_{n+4}	OFF	D_{n-12} Φ

§ When LE is high at the rising edge of the 16th CLK, data from SDI will latch into the 16-bit output latch at the falling edge of LE

¥ The operation of is independent to the interface signals (CLK, SDI, SDO), an unstable period of t_{pLH2} or t_{pHL2} will appear at when new 16-bit data is latched with valid LE (see timing diagram for Normal mode)

Φ New data appear at SDO will have delay time of t_{pLH} or t_{pHL} from rising edge of CLK only

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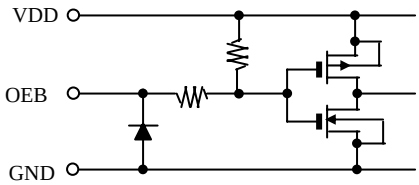
TERMINAL DESCRIPTION

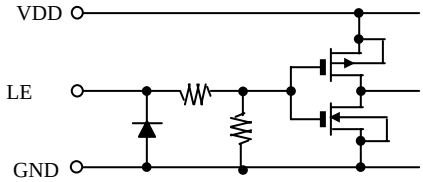
Pin No.	Pin Name	Function
1	GND	Ground terminal for control logic and current sink
2	SDI	Serial-data input to the Shift Register
3	CLK	Clock input terminal for data shift on rising edge
4	LE	Data strobe input terminal Serial data is latched at the falling edge of LE Also, a control signal input for Current Adjust mode
5~20	IOUT0 ~ IOUT15	Constant current output terminals
21	OEB	Output enable terminal When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked).
22	SDO	Serial-data output to the following SDI of next driver IC
23	R-EXT	Input terminal used to connect an external resistor for setting up all output current
24	VDD	5V supply voltage terminal

EQUIVALENT CIRCUIT OF INPUTS AND OUTPUTS

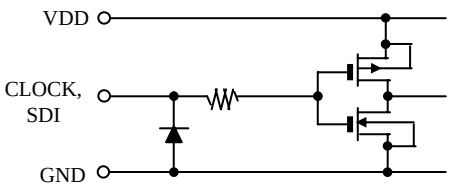
OEB terminal



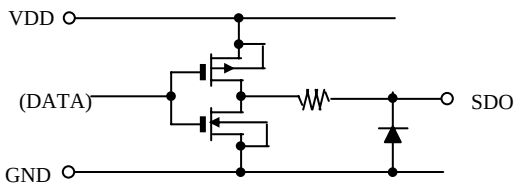
2. LE terminal



3. CLK, SDI terminal



4. SDO terminal



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MAXIMUM RATINGS

(Ta = 25ºC unless otherwise noted)

Characteristic		Symbol	Rating	Unit
Supply Voltage		V_{DD}	0 ~ 7.0	V
Output Voltage		V_{OUT}	-0.5 ~ 7.0	V
Output Current		I_{OUT}	80	mA
Input Voltage		V_{IN}	-0.4 ~ V_{DD} + 0.4	V
GND Terminal Current		I_{GND}	1120	mA
CLOCK Frequency		F_{CLK}	25	MHz
Power Dissipation (On PCB, TA = 25 ℃)	SOP	P_D	1.67	W
	SSOP		1.48	
Thermal Resistance (On PCB, TA = 25 ℃)	SOP	$R_{th(j-a)}$	75	℃/W
	SSOP		85	
Operation Temperature		T_{opr}	-40 ~ 85	℃
Storage Temperature		T_{stg}	-55 ~ 150	℃

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ELECTRICAL CHARACTERISTICS

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Characteristic	Symbol	Condition	Min.	Typ.	Max.	Unit
Supply Voltage	VDD		3.0	5.0	5.5	V
Output Voltage	VDS	~			5.5	V
Output Current	IOUT	Refer to DC Test Circuit	3		50	mA
	IOH	SDO			-1.0	mA
	IOL	SDO			1.0	mA
Input Voltage	VIH	CLK, , LE and SDI	0.8VDD		VDD+ 0.3V	V
	VIL	CLK,, LE and SDI	-0.3		0.3*VDD	V
LE Pulse Width	tw(L)	Normal Mode VDD=4.5 ~ 5.5V	20			ns
Pulse Width	tw(OE)		50			ns
CLK Pulse Width	tw(CLK)		20			ns
Setup Time for SDI	tsu(D)		5			ns
Hold Time for SDI	th(D)		10			ns
Setup Time for LE	tsu(L)		15			ns
Hold Time for LE	th(L)		15			ns
CLK Pulse Width	tw(CLK)	Current Adjust Mode VDD=4.5 ~ 5.5V	20			ns
Setup Time for LE	tsu(CA)		15			ns
Hold Time for LE	th(CA)		15			ns
Clock Frequency	FCLK	Cascade Operation			25.0	MHz
Power Dissipation	PD	Ta=85°C			tbd	W

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SWITCHING CHARACTERISTICS (V_{DD}=5.0V)

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Characteristic		Symbol	Condition	Min.	Typ.	Max.	Unit
Propagation Delay Time ("L" to "H")	CLK -	tpLH1	VDD=5.0 V VDS=1.5 V VIH=VDD VIL=GND R-ext=360 Ω VL=4.0 V RL=50 Ω CL=10 pF		50	100	ns
	LE -	tpLH2			50	100	ns
	-	tpLH3			40	45	ns
	CLK - SDO	tpLH		15	20		ns
Propagation Delay Time ("H" to "L")	CLK -	tpHL1			100	150	ns
	LE -	tpHL2			100	150	ns
	-	tpHL3			40	45	ns
	CLK - SDO	tpHL		15	20		ns
Pulse Width	CLK	tw(CLK)		20			ns
	LE	tw(L)		20			ns
		tw(OE)		50			ns
		twH(OE)		50			ns
Delay time	LE –	tLEOE		200			ns
Hold Time for LE (Normal Mode)		th(L)		10			ns
Setup Time for LE (Normal Mode)		tsu(L)		10			ns
Setup Time for LE (Current Adjust Mode)		tfall		10			ns
Maximum CLK Rise Time		tr**				500	ns
Maximum CLK Fall Time		tf**				500	ns
Output Rise Time of Iout		tor			15	20	ns
Output Fall Time of Iout		tof			15	20	ns

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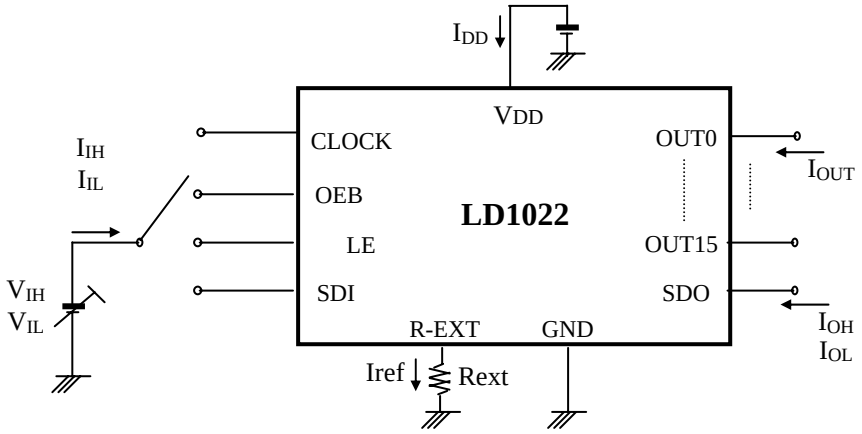
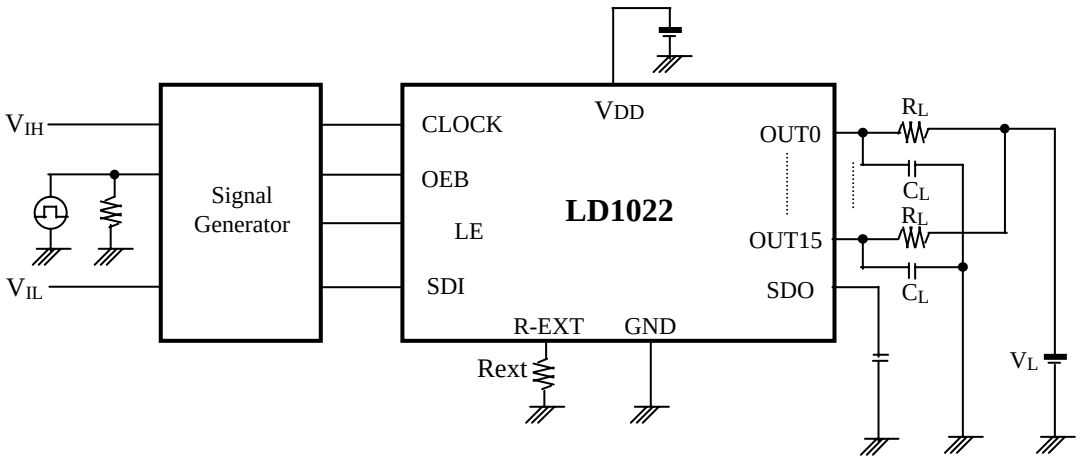
DC CHARACTERISTIC TEST CIRCUIT



AC CHARACTERISTIC TEST CIRCUIT



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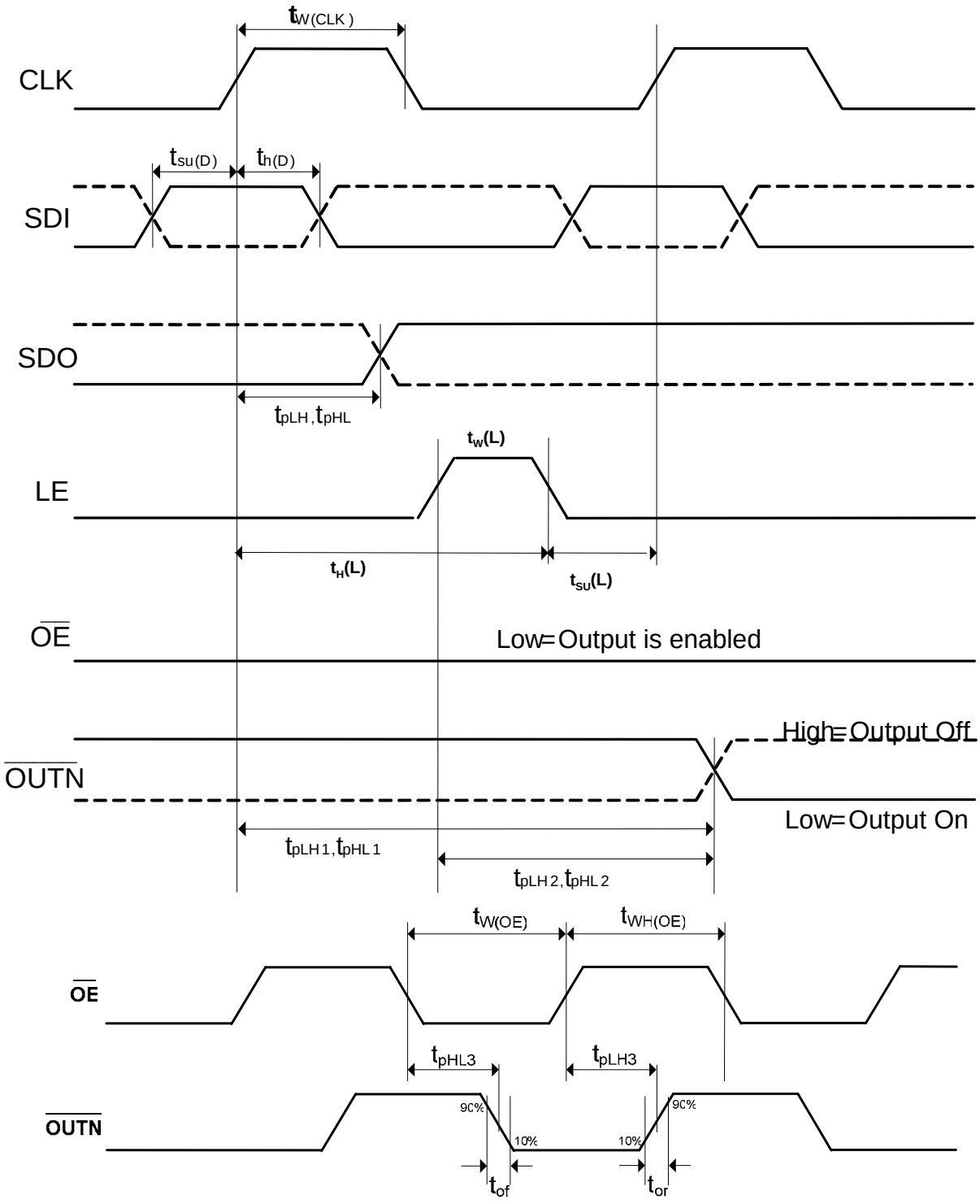
TIMING WAVEFORM

NORMAL MODE



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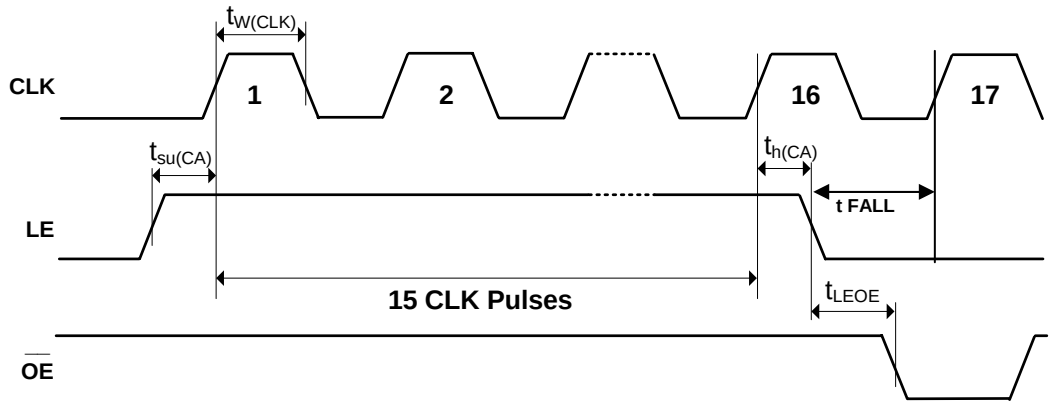
Entering Current Adjust Mode



*** The falling edge of LE should be appeared before t FALL**

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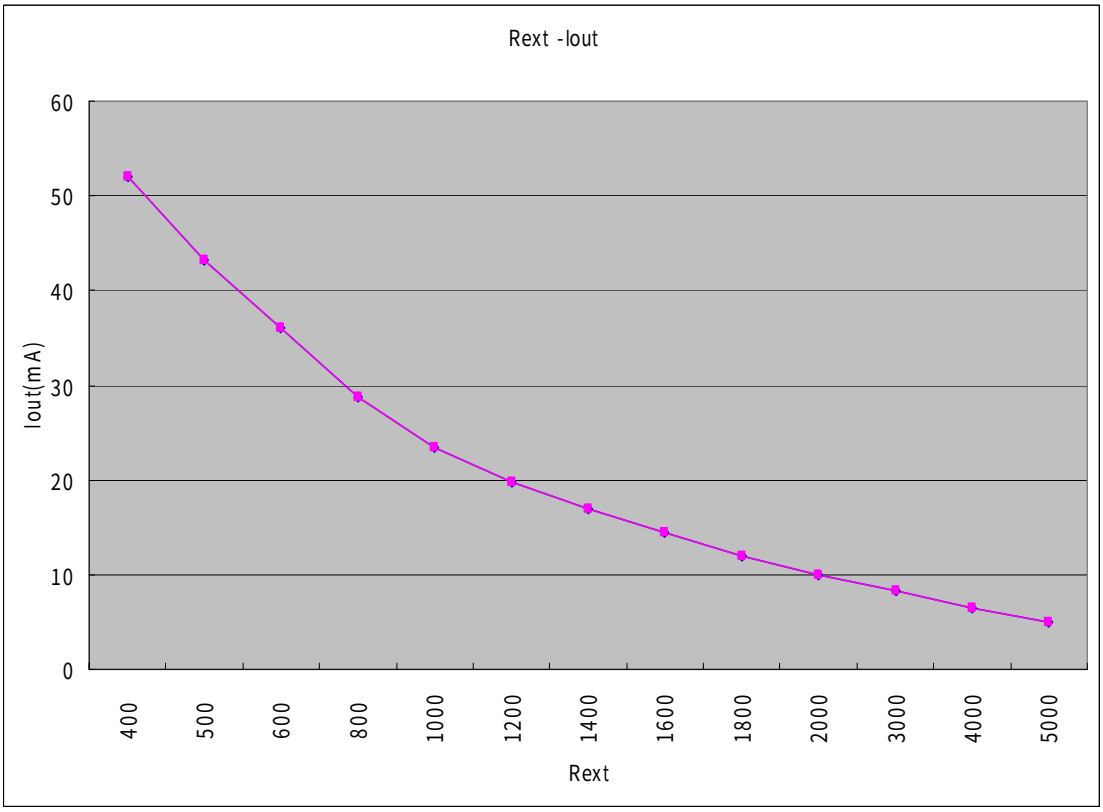
ADJUSTING OUTPUT CURRENT

The output current is determined by an external resistor. The relationship between I_{OUT} and R_{EXT} is as follows;

When VDD = 5V	When VDD = 3.3V
$I_{OUT}[A] = \{1.16/(90+R_{EXT})\} * 22$	$I_{OUT}[A] = \{1.16/(90+R_{EXT})\} * 21$

VDD = 5.0V



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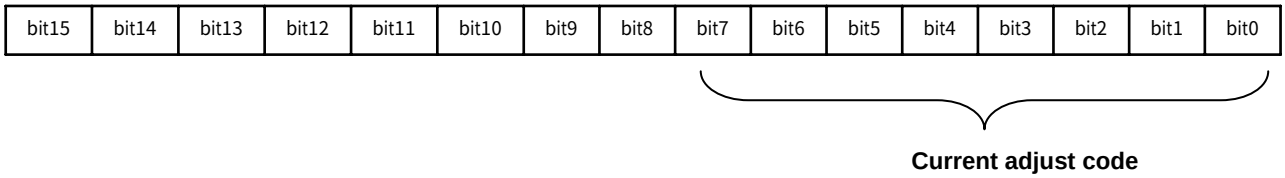
Current Adjust Mode

During current adjust mode, the system controller should send 16bit of data including the 8-bit current adjust code (bit0 to bit7) to the SDI pin. Once LE holds high for 16 CLK cycles, sampling at every rising edge of CLK, BCT5028 will re-direct the contents stored in the Shift Register to a 16-bit Configuration Latch CR [15:0] rather than the 16-bit Output Latch in a Normal mode. Pin OE always enables the output port no matter BCT5028 enters a Current Adjust mode or not.

1. Configuration Register (CR [15:0])



2. Current Gain Table

bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0	bit setting
0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	1	1
-	-	-	-	-	-	-	-	-
-	-	-	-	-	-	-	-	-
1	1	1	1	1	1	0	1	253
1	1	1	1	1	1	1	0	254
1	1	1	1	1	1	1	1	255

Default setting: FFh

Iout = [Bit_setting + 72] / [18*Rext]

Where Rext: External Resistor

Bit setting: Current Value

For Example:

Example 1:

If R-ext =360 ohm;

CR<7:0>=00H will provide 11.11mA

CR<7:0>=FFH will provide 50.46mA

Example 2:

If R-ext =1000 ohm;

CR<7:0>=00H will provide 4.00mA

CR<7:0>=FFH will provide 18.17mA

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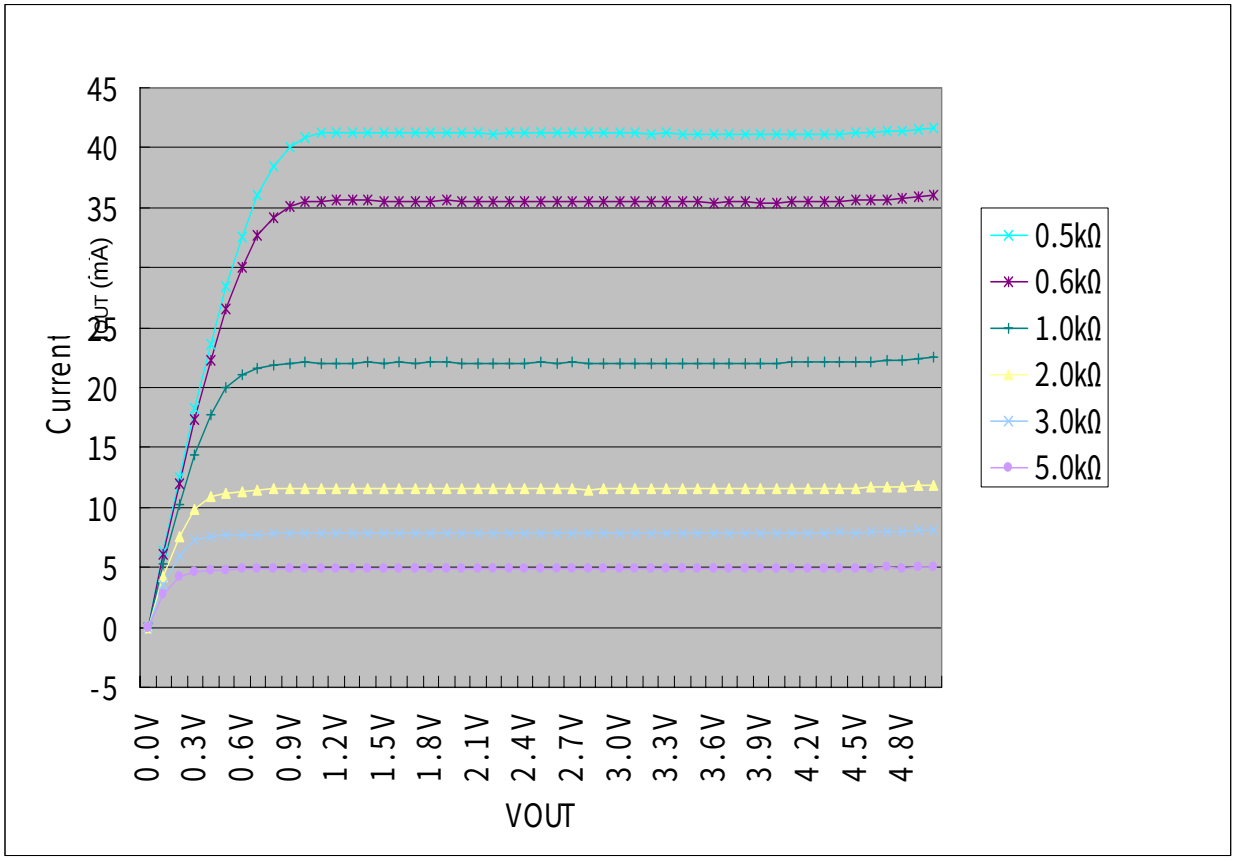
CONSTANT OUTPUT CURRENT

The LD1022 provides a constant current output characteristics for LED display application. The pin to pin deviation is max +/- 1.5% and chip to chip deviation is max +/- 3%.

When VDD = 5.0V



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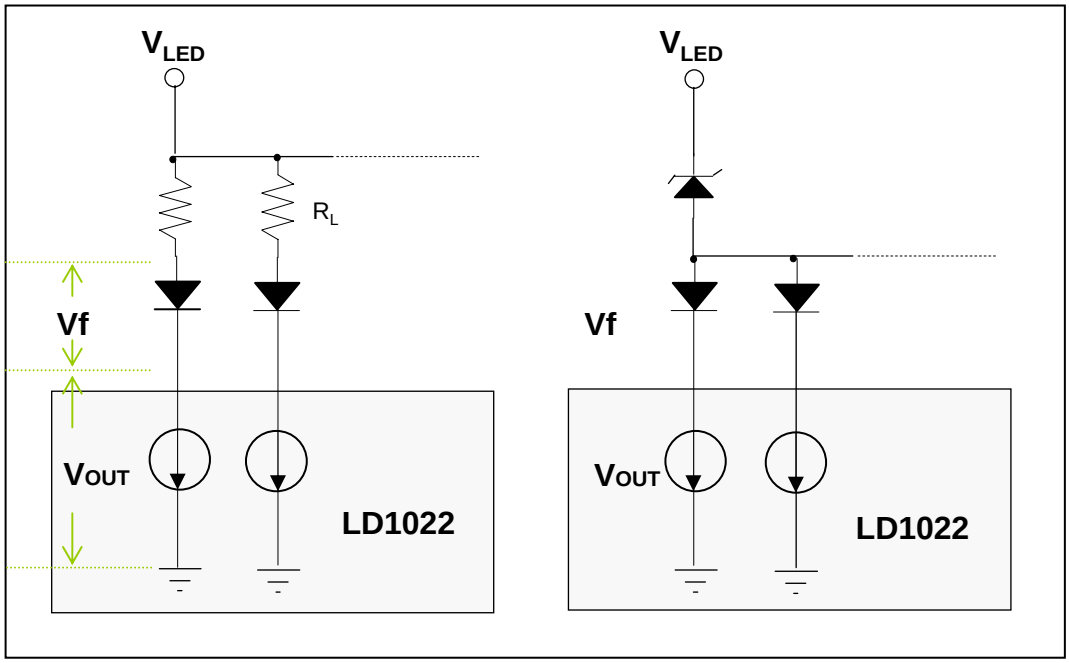
LED SUPPLY VOLTAGE(VLED)



It is very important to select the proper value of Load Resistor(RL). Because the optimal VOUT value guarantees the constant output current and long life time of LED driver IC without over power consumption.

For example, let's calculate the Load Resistor value at VLED=5V, Iout=20mA, LED Forward Voltage(Vf)=3V.

1) The full current of LD1022 = 20mA x 16 (channels) = 320mA
2) The power consumption is 320mA x VOUT voltage.
- when VOUT = 1V, the power consumption is 320mW.
- when VOUT= 2V, the power consumption is 640mW.

Therefore, the Load Resistor (RL) = (VLED – VOUT– Vf) / Iout
= (5V – VOUT – 3V) / 20mA
= 50Ω (When VOUT = 1V)

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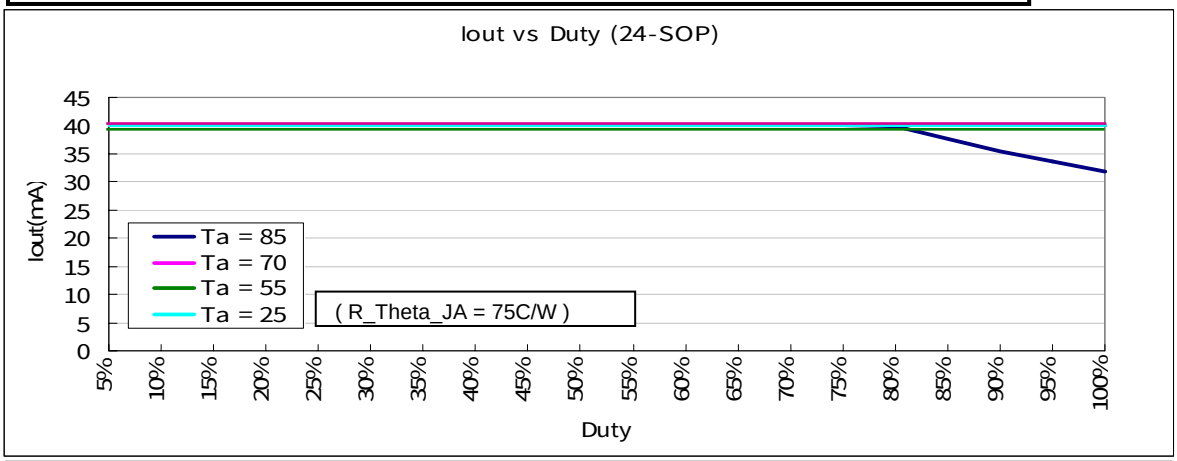
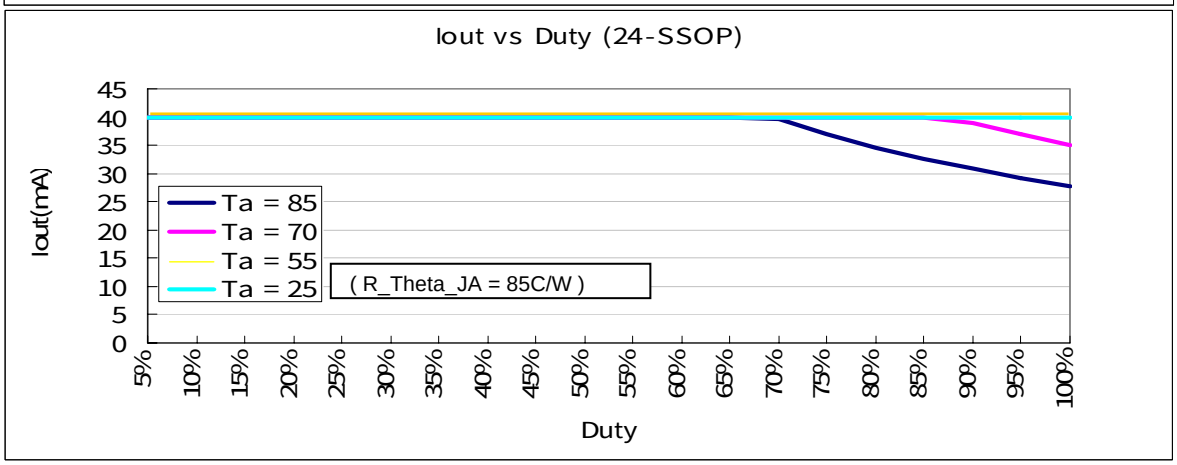
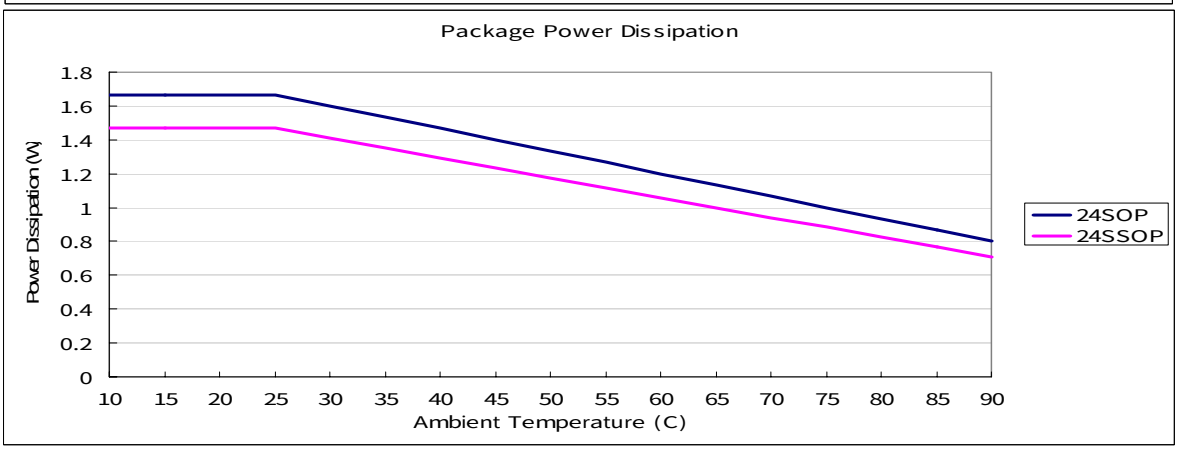
PACKAGE POWER DISSIPATION(PD)

The LD1022 provides many package types such as 24-SOP package and 24-SSOP package. The maximum allowable package power dissipation is determined as PD(max) = (Tj – Ta) / R_Theta_JA. When 16 output channels are turned on simultaneously, the actual power dissipation of package is PD(act) = (IDD x VDD) + (IOUT x Duty x VOUT x 16). Therefore, to keep that PD(act) is less than PD(max).
The maximum allowable output current as a function of duty cycle is:

IOUT = {[(Tj – Ta) / R_Theta_JA] – (IDD x VDD)} / VOUT / Duty / 16 where Tj =150C







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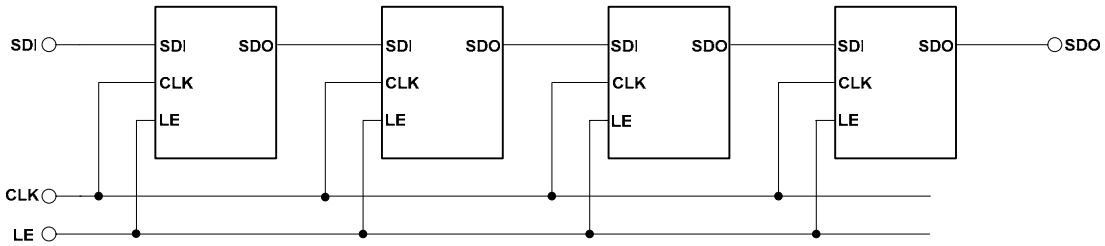
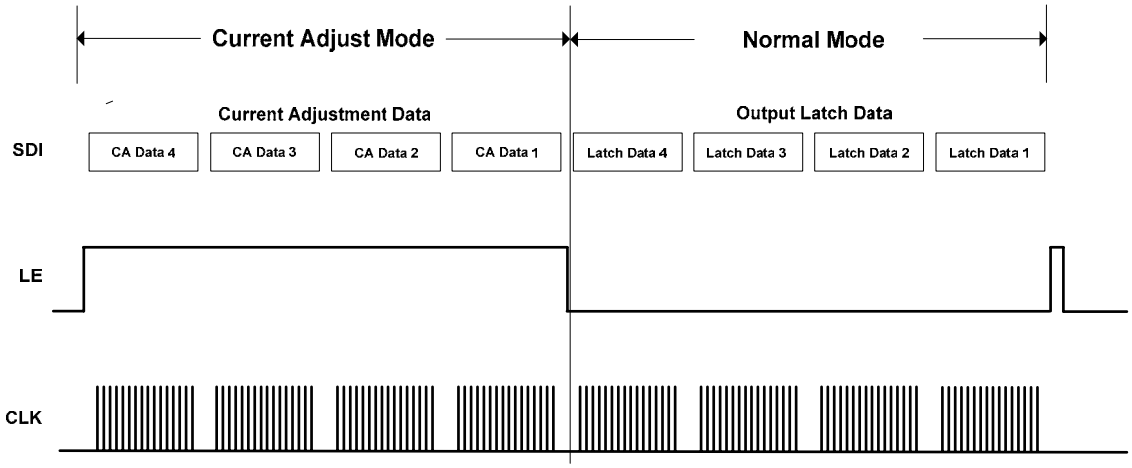
APPLICATION CIRCUIT1

Four chips are connected in cascade configuration, data are programmed in current adjust mode then follow by normal mode.



Example on data written in sequence



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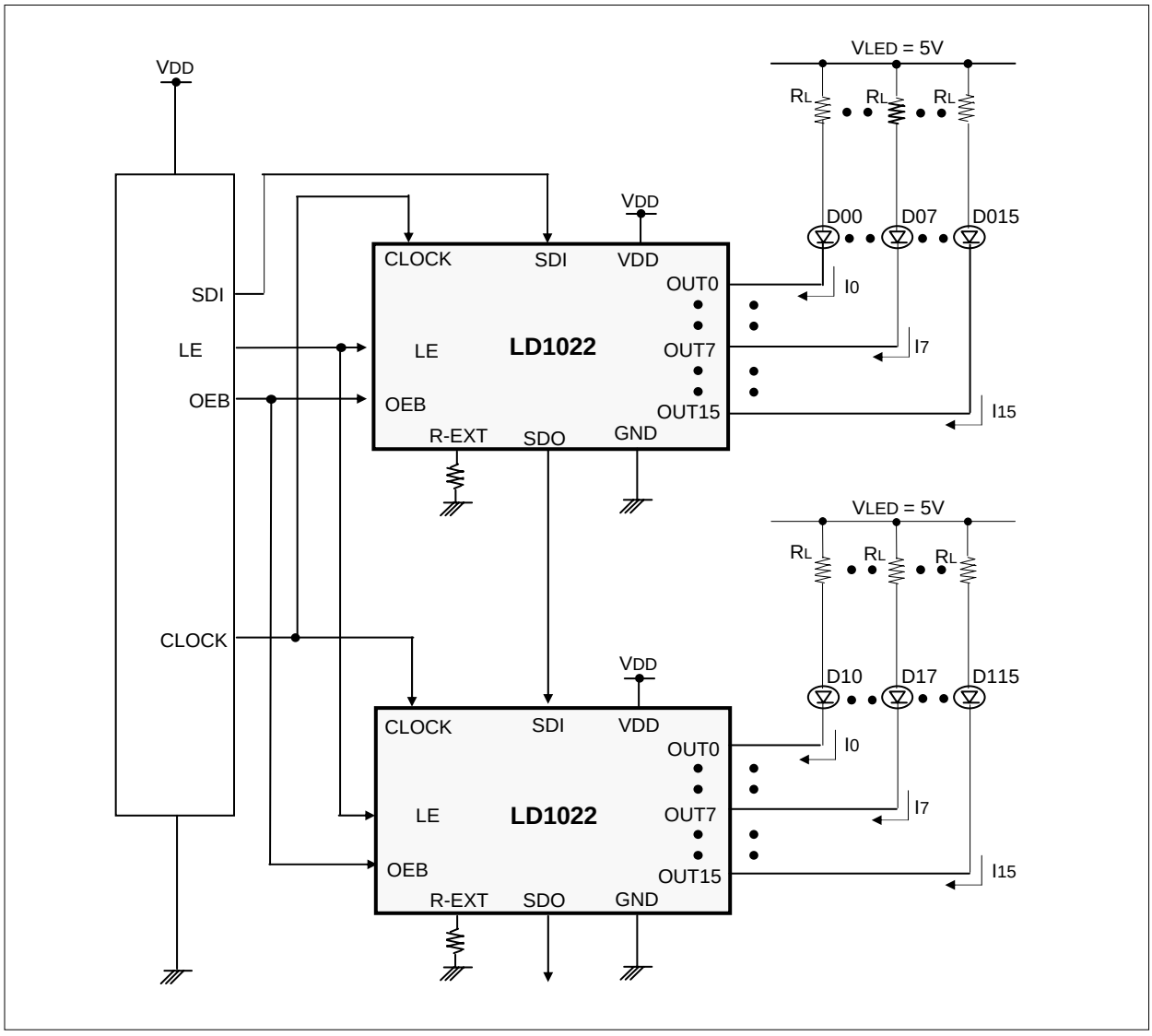
APPLICATION CIRCUIT 2 (16x2 Static Type)



Data & Control Signal Connection for 16x2 Static Type Application

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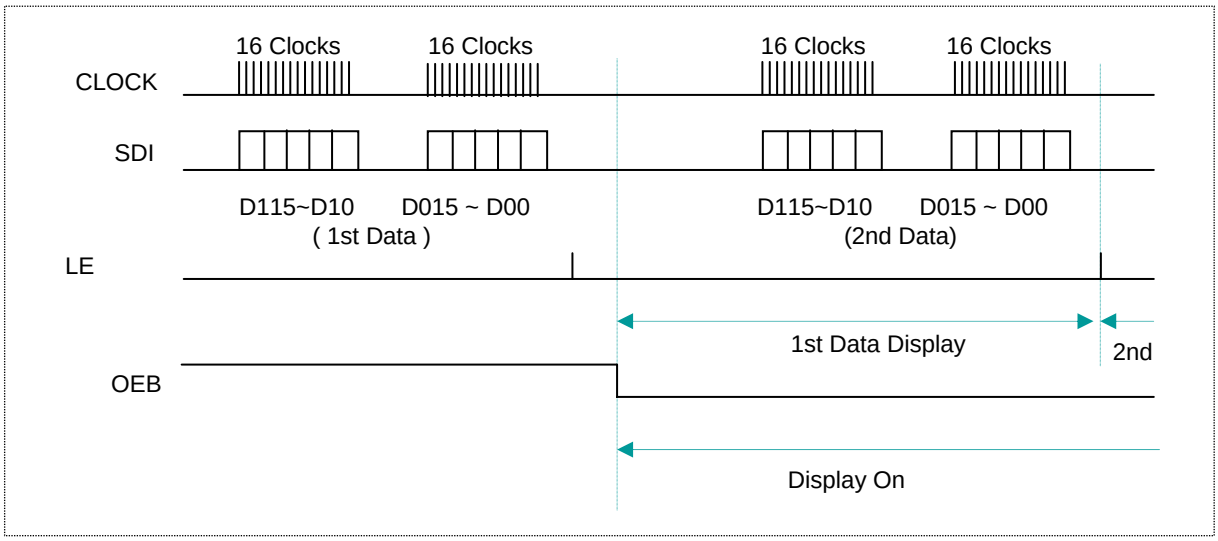
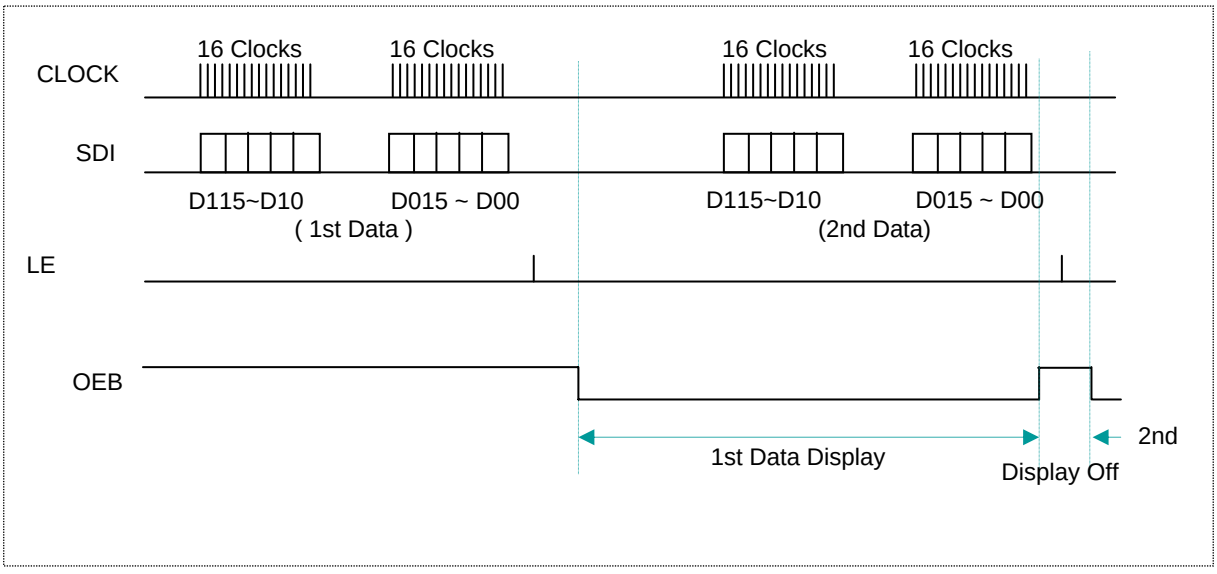
Timing Diagram for Application Circuit 2 (16x2 Static Type)



Timing Diagram for Application Circuit 2 (16x2 Static Type) : Another Case



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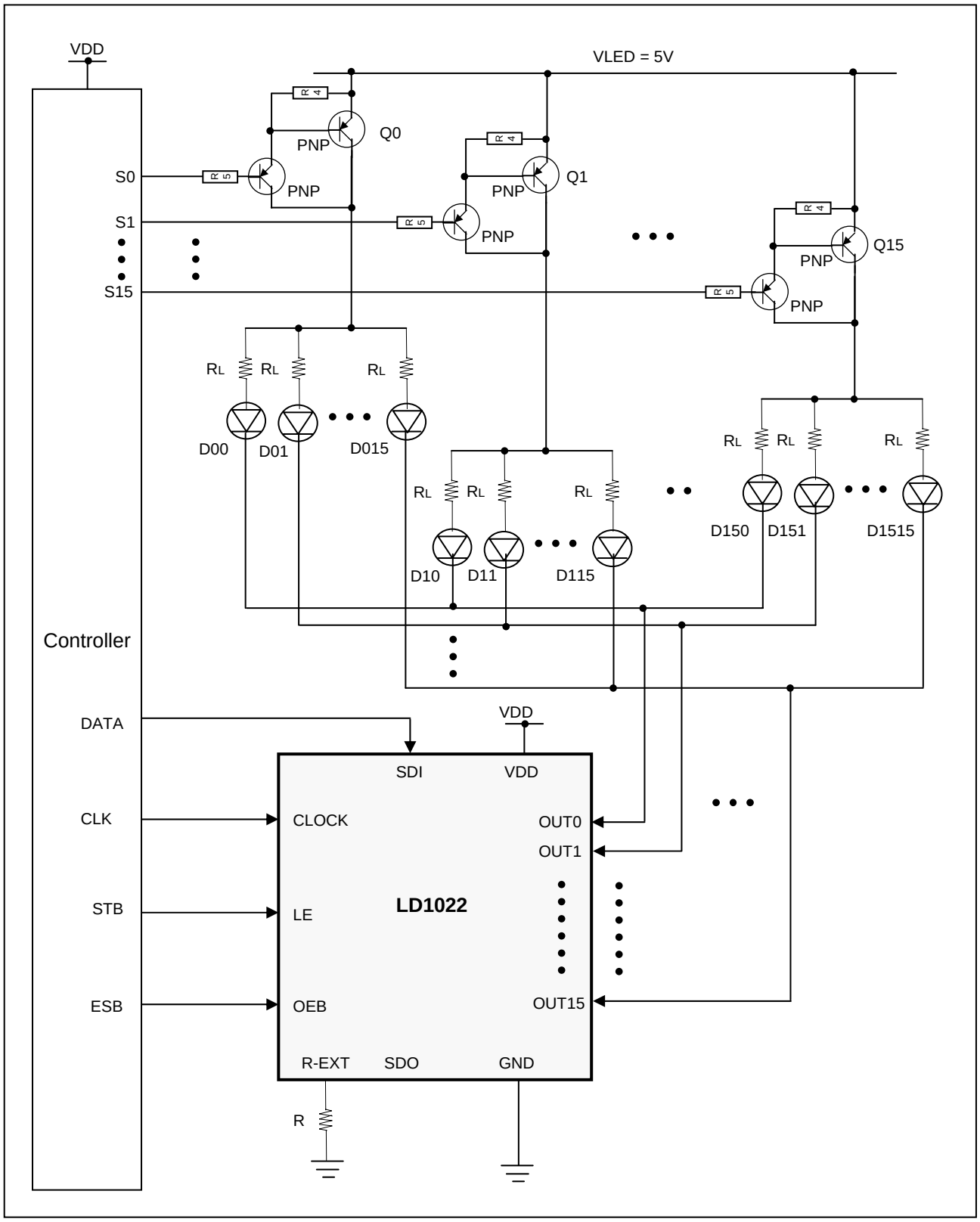
APPLICATION CIRCUIT 2 (16x16 Dynamic Type)



Data & Control Signal Connection for 16x16 Dynamic Type Application

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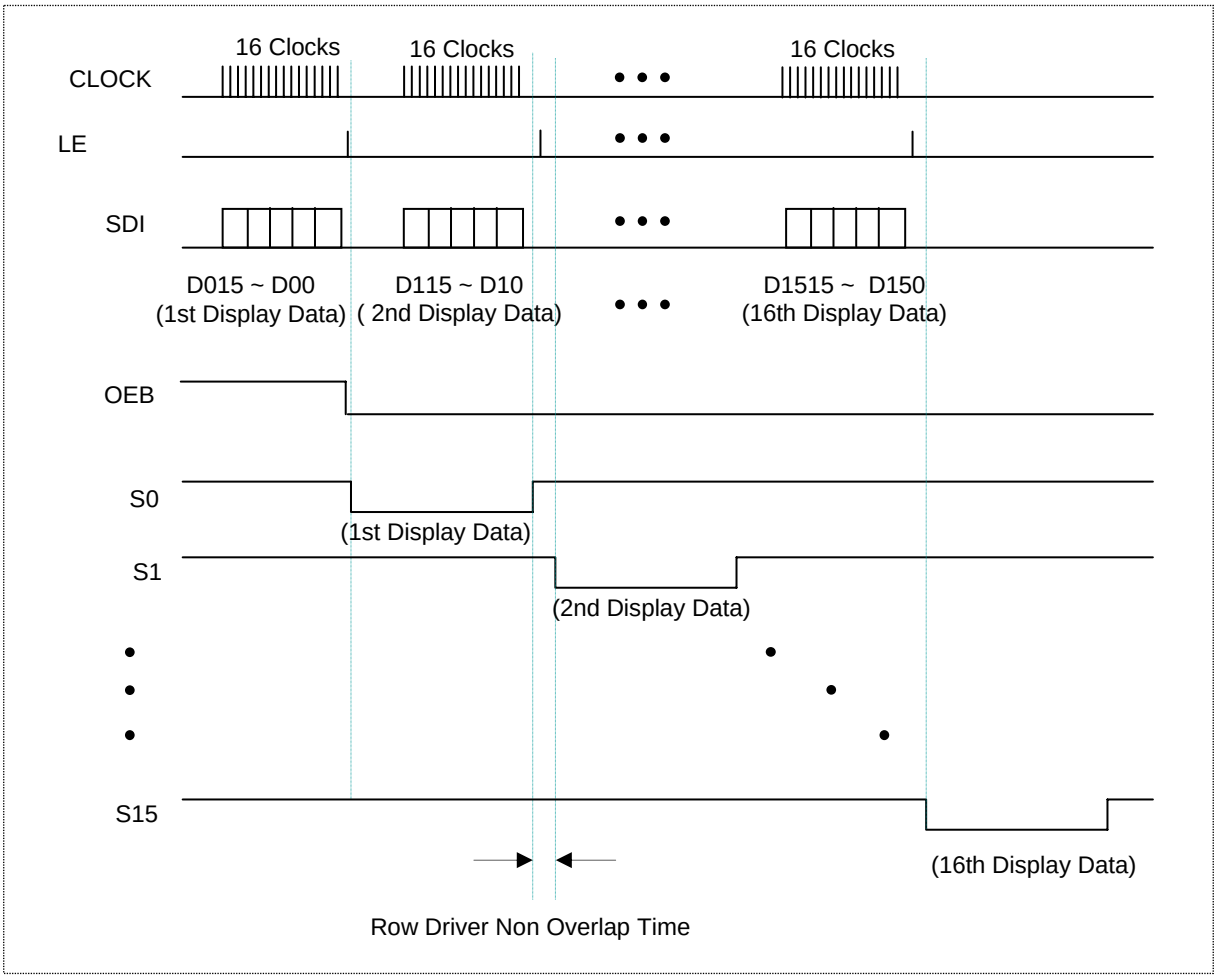
Timing Diagram for Application Circuit 2 (16x16 Dynamic Type)



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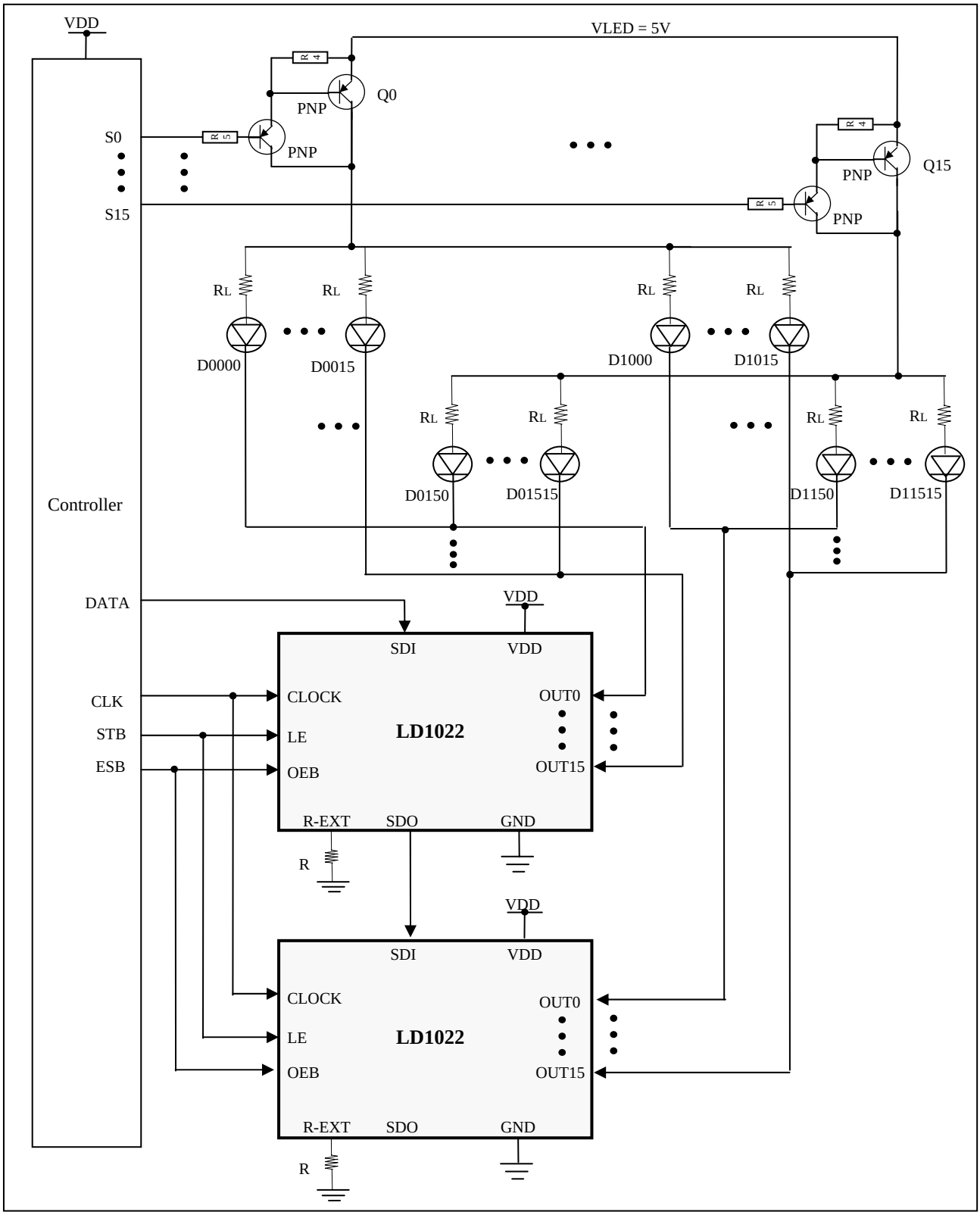
APPLICATION CIRCUIT 3 (32x16 Dynamic Type)



Data & Control Signal Connection for 32x16 Dynamic Type Application

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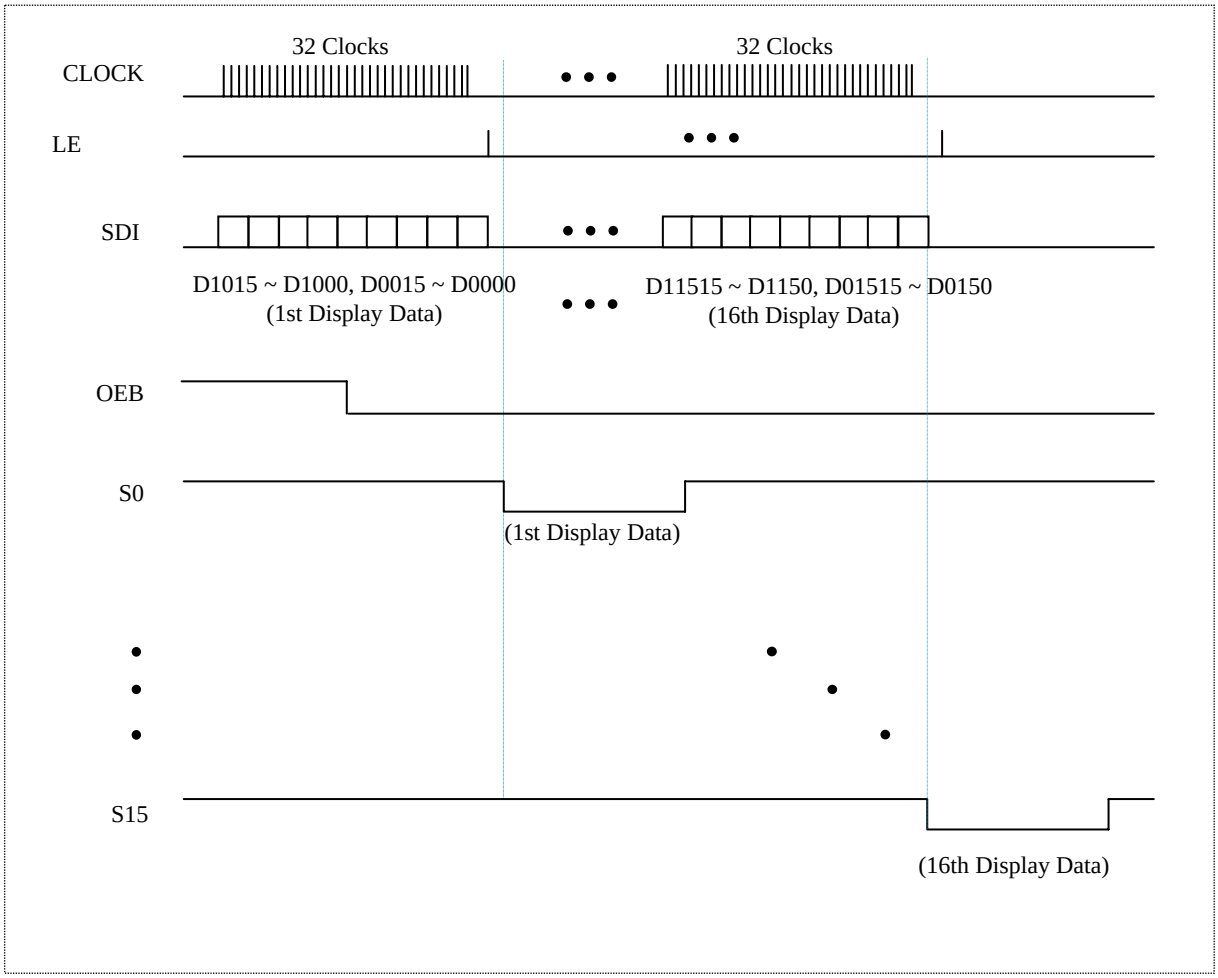
Timing Diagram for Application Circuit 3 (32x16 Dynamic Type)



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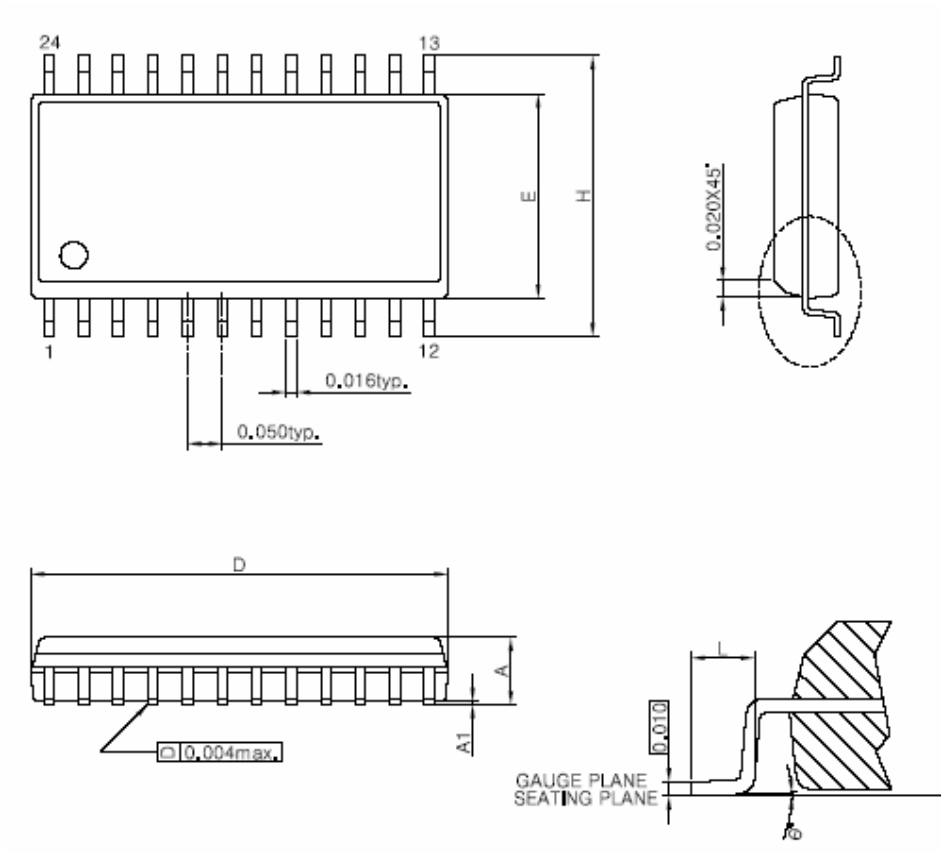
PACKAGE INFORMATION

LD1022-SP (SOP 24)



SYMBOLS	MIN.	NOM	MAX.
A	-	-	0.104
A1	0.004	-	-
D	0.612	0.618	0.624
E	0.292	0.296	0.299
H	0.405	0.412	0.419
L	0.021	0.031	0.041
θ°	0	4	8

UNIT : INCH

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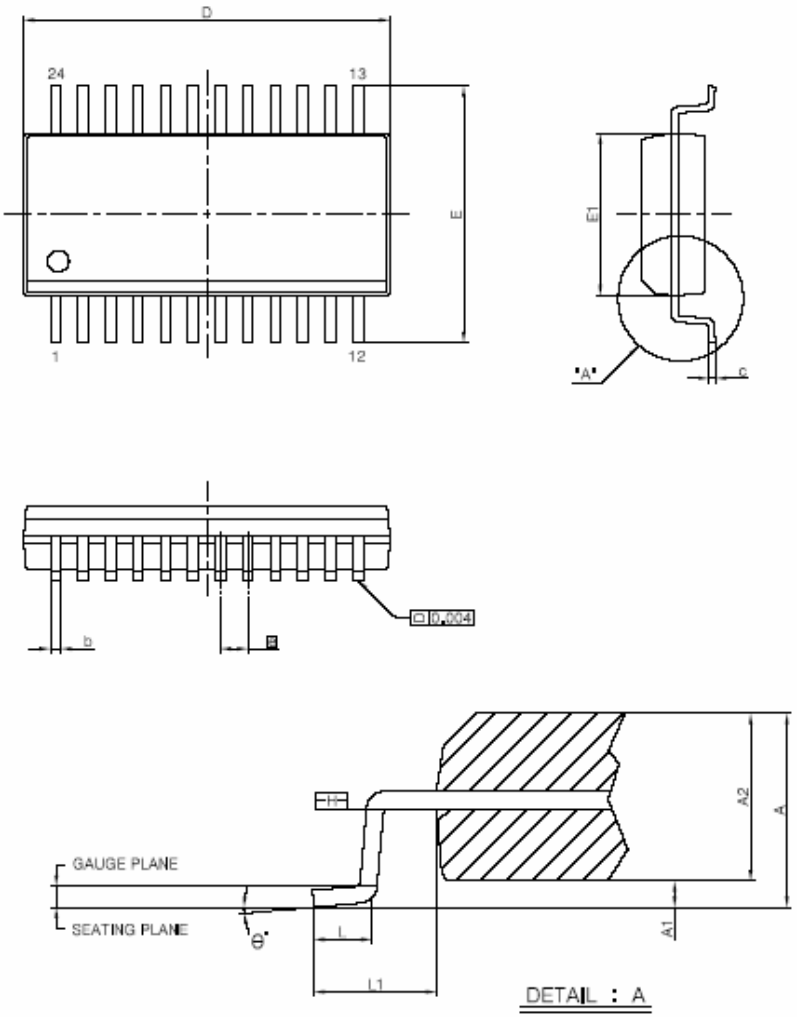
LD1022-SS (SSOP 24)



SYMBOLS	MIN.	NOM	MAX.
A	0.053	0.064	0.069
A1	0.004	0.006	0.010
A2	–	–	0.059
D	0.337	0.341	0.344
E	0.228	0.236	0.244
E1	0.150	0.154	0.157
b	0.008	–	0.012
C	0.007	–	0.010
e		0.025 BASIC	
L	0.016	0.025	0.050
L1		0.041 BASIC	
θ°	0°	–	8°

UNIT : INCH

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