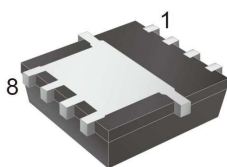


TSM40N03PQ56

30V N-Channel Power MOSFET

PDFN56



Pin Definition:

- | | |
|-----------|----------|
| 1. Source | 8. Drain |
| 2. Source | 7. Drain |
| 3. Source | 6. Drain |
| 4. Gate | 5. Drain |

PRODUCT SUMMARY

V _{DS} (V)	R _{DS(on)} (mΩ)	I _D (A)
30	4.5 @ V _{GS} =10V	19
	5.8 @ V _{GS} =4.5V	16

Features

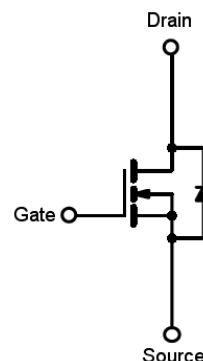
- Advanced Trench Technology
- Low On-Resistance
- Low gate charge typical @ 12nC (Typ.)
- Low Crss typical @ 140pF (Typ.)

Ordering Information

Part No.	Package	Packing
TSM40N03PQ56 RLG	PDFN56	2.5Kpcs / 13" Reel

Note: "G" denote for Halogen Free Product

Block Diagram



N-Channel MOSFET

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	30	V	
Gate-Source Voltage	V _{GS}	±20	V	
Continuous Drain Current	I _D	T _C =25°C	40	A
		T _C =70°C	40	
		T _A =25°C	31	
		T _A =70°C	25	
Drain Current-Pulsed Note 1	I _{DM}	100	A	
Avalanche Current, L=0.5mH	I _{AS} , I _{AR}	38	A	
Avalanche Energy, L=0.5mH	E _{AS} , E _{AR}	72	mJ	
Maximum Power Dissipation	P _D	T _C =25°C	36	W
		T _C =70°C	23	
		T _A =25°C	4.2	
		T _A =70°C	2.7	
Storage Temperature Range	T _{STG}	-55 to +150	°C	
Operating Junction Temperature Range	T _J	-55 to +150	°C	

* Limited by maximum junction temperature

Thermal Performance

Parameter	Symbol	Limit	Unit
Thermal Resistance - Junction to Case	Rθ _{JC}	3.5	°C/W
Thermal Resistance - Junction to Ambient	Rθ _{JA}	30	°C/W

Notes: Surface mounted on FR4 board t ≤ 10sec

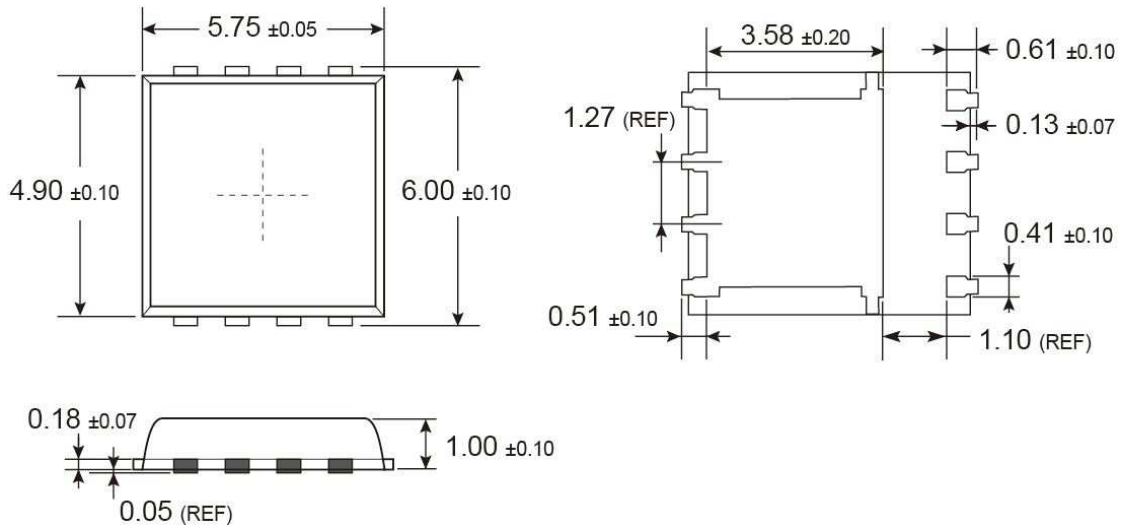
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	BV_{DSS}	30	--	--	V
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 19A$	$R_{DS(ON)}$	--	3.5	4.5	mΩ
	$V_{GS} = 4.5V, I_D = 16A$		--	4.6	5.8	
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	1.15	--	2.2	V
Zero Gate Voltage Drain Current	$V_{DS} = 24V, V_{GS} = 0V$	I_{DSS}	--	--	1	μA
Gate Body Leakage	$V_{GS} = \pm 20V, V_{DS} = 0V$	I_{GSS}	--	--	±100	nA
Dynamic						
Total Gate Charge	$V_{DS} = 15V, I_D = 19A, V_{GS} = 4.5V$	Q_g	--	12	--	nC
Gate-Source Charge		Q_{gs}	--	5.4	--	
Gate-Drain Charge		Q_{gd}	--	4.6	--	
Input Capacitance	$V_{DS} = 15V, V_{GS} = 0V, f = 1.0MHz$	C_{iss}	--	1700	--	pF
Output Capacitance		C_{oss}	--	350	--	
Reverse Transfer Capacitance		C_{rss}	--	140	--	
Switching						
Turn-On Delay Time	$V_{GS} = 4.5V, V_{DS} = 15V, R_G = 1\Omega$	$t_{d(on)}$	--	25	--	nS
Turn-On Rise Time		t_r	--	20	--	
Turn-Off Delay Time		$t_{d(off)}$	--	25	--	
Turn-Off Fall Time		t_f	--	15	--	
Drain-Source Diode Characteristics and Maximum Rating						
Drain-Source Diode Forward Voltage	$V_{GS}=0V, I_S=10A$	V_{SD}	--	0.8	1.2	V
Reverse Recovery Time	$I_S = 10A, T_J=25^\circ C, di/dt = 100A/\mu s$	t_{fr}	--	25	--	nS
Reverse Recovery Charge		Q_{fr}	--	17	--	nC

Notes:

1. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
2. $R\theta_{JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R\theta_{JC}$ is guaranteed by design while $R\theta_{CA}$ is determined by the user's board design. $R\theta_{JA}$ shown below for single device operation on FR-4 in still air
3. The maximum current rating is limited by package.

PDFN56 Mechanical Drawing



Unit: Millimeters

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