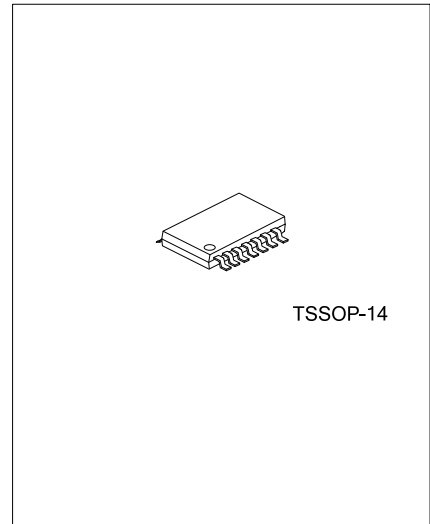




U74LCX74

CMOS IC

LOW VOLTAGE DUAL D-TYPE POSITIVE EDGE-TRIGGERED FLIP-FLOP WITH 5V TOLERANT INPUTS



DESCRIPTION

The **U74LCX74** is a dual D-type flip-flop with Asynchronous Clear and Set inputs and complementary (Q, \bar{Q}) outputs. Information at the input is transferred to the outputs on the positive edge of the clock pulse. After the Clock Pulse input threshold voltage has been passed, the Data input is locked out and information present will not be transferred to the outputs until the next rising edge of the Clock Pulse input.

Asynchronous inputs:

LOW input to \bar{S}_D (Set) sets Q to HIGH level

LOW input to \bar{C}_D (Clear) sets Q to LOW level

Clear and Set are independent of clock

Simultaneous LOW on \bar{C}_D and \bar{S}_D makes both Q and \bar{Q} high

FEATURES

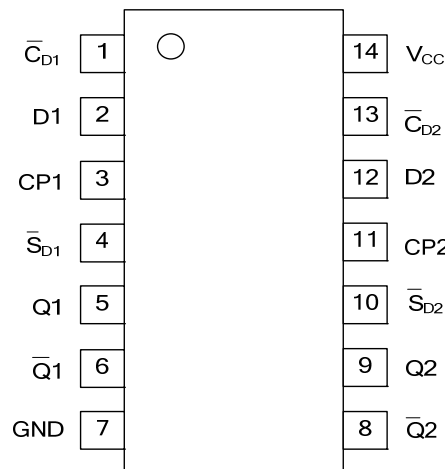
- * 2.3V-3.6V V_{CC} specifications provided
- * 5V tolerant inputs
- * 7.0 ns t_{PD} max ($V_{CC}=3.3V$), $I_{CC}=10\mu A$ (max.)
- * Power down high impedance inputs and outputs
- * $\pm 24mA$ output drive ($V_{CC}=3.0V$)

ORDERING INFORMATION

Ordering Number		Package	Packing
Lead Free	Halogen Free		
U74LCX74L-P14-T	U74LCX74G-P14-T	TSSOP-14	Tube
U74LCX74L-P14-R	U74LCX74G-P14-R	TSSOP-14	Tape Reel

<p>U74LCX74L-P14-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Lead Free</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) P14: TSSOP-14</p> <p>(3) L: Lead Free, G: Halogen Free</p>
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■ PIN CONFIGURATION



■ PIN DESCRIPTIONS

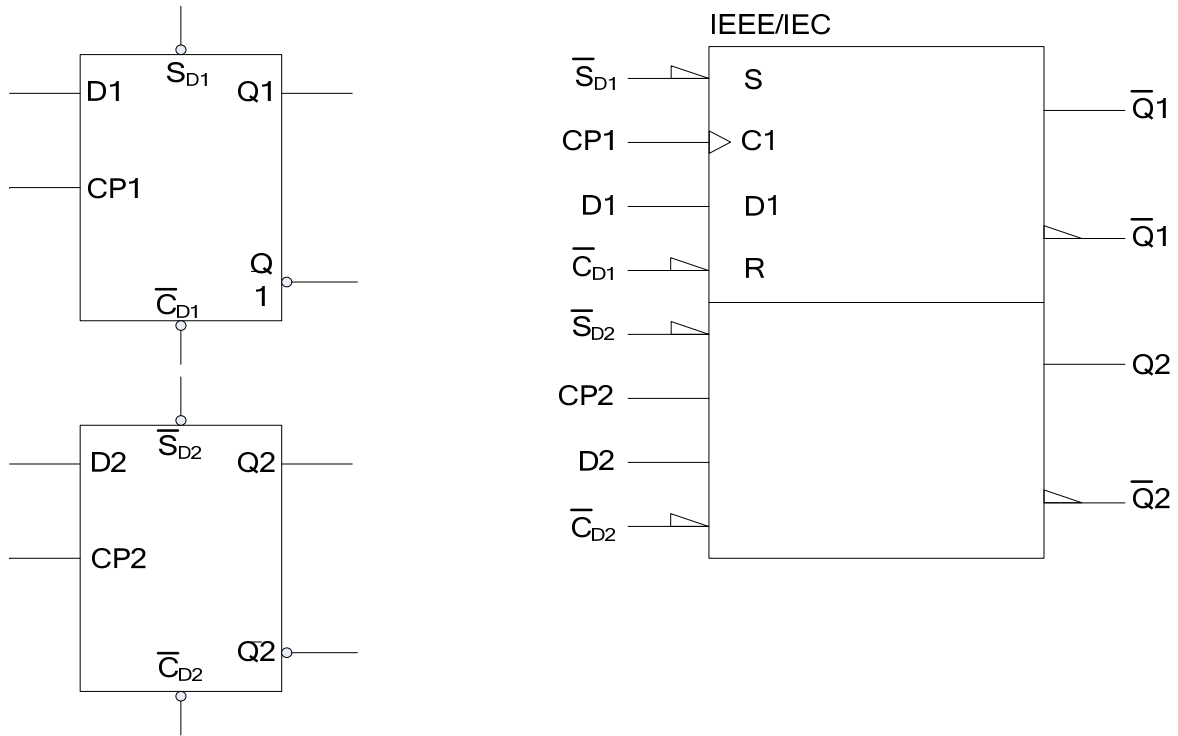
Pin Names	Description
D1, D2	Data inputs
CP1, CP2	Clock Pulse Inputs
\bar{C}_{D1} , \bar{C}_{D2}	Direct Clear Inputs
\bar{S}_{D1} , \bar{S}_{D2}	Direct Set Inputs
Q1, \bar{Q}_1 , Q2, \bar{Q}_2	Outputs

■ FUNCTION TABLE (each gate)

INPUT				OUTPUT		Function
\bar{S}_D	\bar{C}_D	CP	D	Q	\bar{Q}	
L	H	X	X	H	L	Asynchronous Set
H	L	X	X	L	H	Asynchronous Clear
L	L	X	X	H	H	Undetermined
H	H	↑	H	H	L	Load and Read Register
H	H	↑	L	L	H	
H	H	L	X	Q ₀	\bar{Q}_0	Hold

H=High Voltage Level; L=Low Voltage Level;
 X=Immaterial; ↑=Low-to-High Clock Transition;
 Q₀ (\bar{Q}_0)=Previous Q(\bar{Q}) before Low-to-High Transition of Clock

■ LOGIC DIAGRAM (positive logic)



■ ABSOLUTE MAXIMUM RATING (unless otherwise specified)(Note 1)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	-0.5~7.0	V
Input Voltage	V_{IN}	-0.5~ 7.0	V
Output Voltage	V_{OUT}	-0.5~ $V_{CC}+0.5$	V
Input Diode Current($V_I < GND$)	I_{IK}	-50	mA
Output Diode Current($V_O < GND$ or $V_O > V_{CC}$)	I_{OK}	± 50	mA
Output Current	I_{OUT}	± 50	mA
V_{CC} or GND Current	I_{CC}	± 100	mA
Ground Current	I_{GND}	± 100	mA
Storage Temperature	T_{STG}	-65 ~ +150	°C

Notes: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
 2. Absolute maximum ratings are those values beyond which the device could be permanently damaged.
 Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ RECOMMENDED OPERATING COMDITIONS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}		2.0		3.6	V
Input Voltage	V_{IN}		0		5.5	V
Output Voltage	V_{OUT}		0		V_{CC}	V
Input Transition Rise or Fall Rate	$\Delta t/\Delta v$	Input Edge Rate, $V_{IN}=0.8V-2V, V_{CC}=3V$	0		10	ns/V
Operating Temperature	T_A		-40		+85	°C

■ STATIC CHARACTERISTICS ($T_A=-40^{\circ}C$ to $+85^{\circ}C$, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
High-level input voltage	V_{IH}	$V_{CC}=2.3V$ to $2.7V$	1.7			V
		$V_{CC}=2.7V$ to $3.6V$	2.0			
Low-level input voltage	V_{IL}	$V_{CC}=2.3V$ to $2.7V$			0.7	V
		$V_{CC}=2.7V$ to $3.6V$			0.8	
High-Level Output Voltage	V_{OH}	$V_{CC}=2.3V$ to $3.6V, I_{OH}=-100\mu A$	$V_{CC}-0.2$			V
		$V_{CC}=2.3V, I_{OH}=-8mA$	1.8			
		$V_{CC}=2.7V, I_{OH}=-12mA$	2.2			
		$V_{CC}=3V, I_{OH}=-18mA$	2.4			
Low-Level Output Voltage	V_{OL}	$V_{CC}=2.3V$ to $3.6V, I_{OL}=100\mu A$			0.2	V
		$V_{CC}=2.3V, I_{OL}=8mA$			0.6	
		$V_{CC}=2.7V, I_{OL}=12mA$			0.4	
		$V_{CC}=3V, I_{OL}=16mA$			0.4	
		$V_{CC}=3V, I_{OL}=24mA$			0.55	
Input Leakage Current	$I_{I(LEAK)}$	$V_{CC}=2.3V \sim 3.6V, V_{IN}=0 \sim 5.5V$			± 5	μA
Quiescent Supply Current	I_Q	$V_{CC}=2.3V$ to $3.6V, V_{IN}=V_{CC}$ or GND			10	μA
		$V_{CC}=2.3V$ to $3.6V, 3.6V \leq V_{IN} \leq 5.5V$			± 10	
Increase I_{CC} per input	ΔI_Q	$V_{CC}=2.3V$ to $3.6V, V_{IH}=V_{CC}-0.6V$			500	μA
Power-Off Leakage Current	I_{OFF}	$V_{CC}=0, V_{IN}$ or $V_{OUT}=5.5V$			10	μA
Input Capacitance	C_{IN}	$V_{CC}=\text{Open}, V_I=0$ or V_{CC}		7.0		pF
Output Capacitance	C_{OUT}	$V_{CC}=3.3V, V_I=0$ or V_{CC}		8.0		pF

■ DYNAMIC CHARACTERISTICS (Input: $t_r, t_f=3\text{ns}$, $f=1\text{MHz}$, $T_A=-40^\circ\text{C}$ to 85°C , $R_L=500\Omega$)

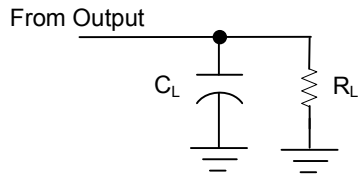
PARAMETER	SYMBOL	Conditions	MIN	TYP	MAX	UNIT
Maximum Clock Frequency	f_{MAX}	$V_{\text{CC}}=2.5\text{V}\pm 0.2\text{V}$, $C_L=30\text{pF}$	150			MHZ
		$V_{\text{CC}}=2.7\text{V}$, $C_L=50\text{pF}$	150			
		$V_{\text{CC}}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$	150			
Propagation Delay CPn to Qn or \bar{Q}_n	$t_{\text{PHL}}/t_{\text{PLH}}$	$V_{\text{CC}}=2.5\text{V}\pm 0.2\text{V}$, $C_L=30\text{pF}$	1.5		8.4	ns
		$V_{\text{CC}}=2.7\text{V}$, $C_L=50\text{pF}$	1.5		8.0	
		$V_{\text{CC}}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$	1.5		7.0	
Propagation Delay \bar{C}_{Dn} or \bar{S}_{Dn} to Qn or \bar{Q}_n	$t_{\text{PHL}}/t_{\text{PLH}}$	$V_{\text{CC}}=2.5\text{V}\pm 0.2\text{V}$, $C_L=30\text{pF}$	1.5		8.4	ns
		$V_{\text{CC}}=2.7\text{V}$, $C_L=50\text{pF}$	1.5		8.0	
		$V_{\text{CC}}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$	1.5		7.0	
Setup Time	t_s	$V_{\text{CC}}=2.5\text{V}\pm 0.2\text{V}$, $C_L=30\text{pF}$	4.0			ns
		$V_{\text{CC}}=2.7\text{V}$, $C_L=50\text{pF}$	2.5			
		$V_{\text{CC}}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$	2.5			
Hold Time	t_H	$V_{\text{CC}}=2.5\text{V}\pm 0.2\text{V}$, $C_L=30\text{pF}$	2.0			ns
		$V_{\text{CC}}=2.7\text{V}$, $C_L=50\text{pF}$	1.5			
		$V_{\text{CC}}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$	1.5			
Pulse Width CP	t_w	$V_{\text{CC}}=2.5\text{V}\pm 0.2\text{V}$, $C_L=30\text{pF}$	4.0			ns
		$V_{\text{CC}}=2.7\text{V}$, $C_L=50\text{pF}$	3.3			
		$V_{\text{CC}}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$	3.3			
Pulse Width and \bar{C}_{Dn} , \bar{S}_{Dn}	t_w	$V_{\text{CC}}=2.5\text{V}\pm 0.2\text{V}$, $C_L=30\text{pF}$	4.0			ns
		$V_{\text{CC}}=2.7\text{V}$, $C_L=50\text{pF}$	3.6			
		$V_{\text{CC}}=3.3\text{V}\pm 0.3\text{V}$, $C_L=50\text{pF}$	3.3			

See Fig. 1 and Fig. 2 for test circuit and waveforms.

■ OPERATING CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Dissipation Capacitance	C_{PD}	$V_{\text{CC}}=3.3\text{V}$, $V_I=0\text{V}$ or V_{CC} , $f=10\text{MHz}$		25		pF

■ TEST CIRCUIT AND WAVEFORMS

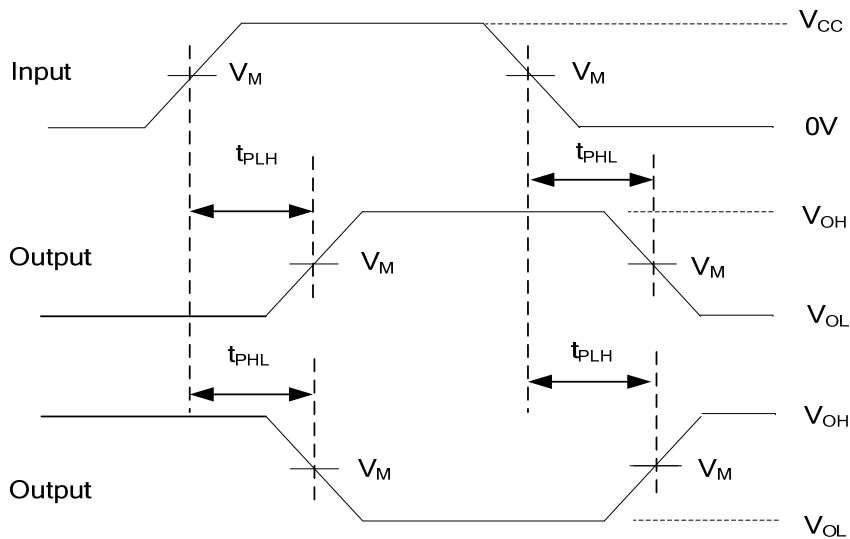


TEST CIRCUIT

Note: C_L includes probe and jig capacitance.

Fig. 1 Load circuitry for switching times.

V_{CC}	V_M	C_L	R_L
$2.5V \pm 0.2V$	$V_{CC}/2$	30pF	500Ω
2.7V	1.5V	50pF	500Ω
$3.3V \pm 0.3V$	1.5V	50pF	500Ω



PROPAGATION DELAY TIMES

■ TEST CIRCUIT AND WAVEFORMS(Cont.)

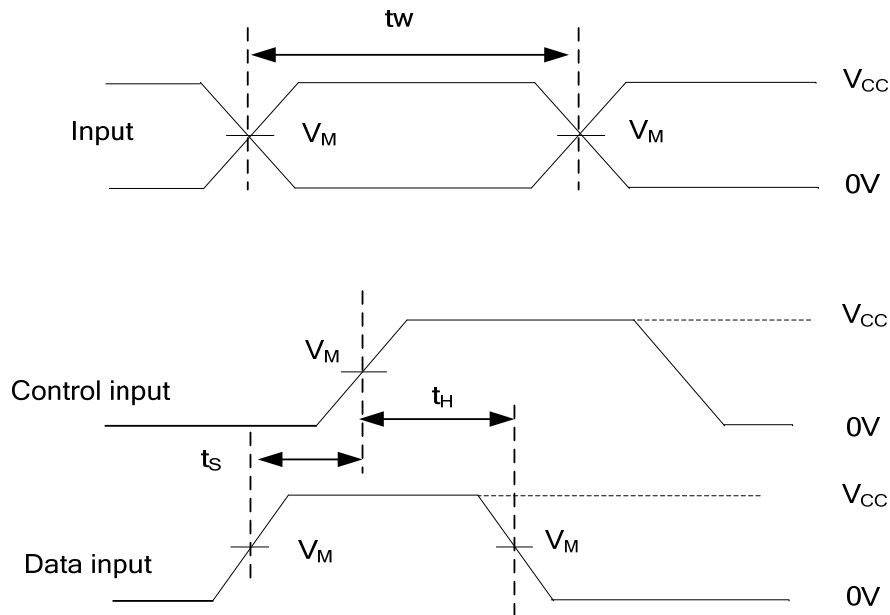


Fig. 2 Propagation delay from input to output and input voltage waveforms.

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