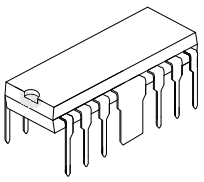
TEA2025A

LINEAR INTEGRATED CIRCUIT

STEREO AUDIO AMPLIFIER



DIP-12H

■ DESCRIPTION

The UTC **TEA2025A** is a monolithic integrated circuit, consisting of a 2-channel power amplifier. It is suitable for stereo and bridge amplifier application of radio cassette tape recorders.

■ FEATURES

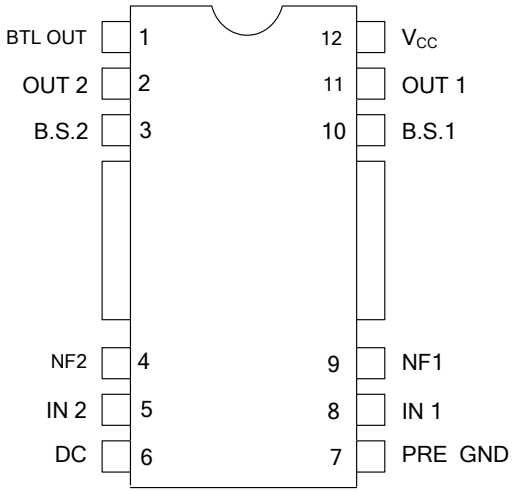
* High output power
  Stereo: Po=2.3W (Typ) at Vcc=9V, R_L=4 Ω
  Bridge: Po=4.7W (Typ) at Vcc=9V, R_L=8Ω
* Low switching distortion at high frequency
* Small shock noise at the time of power on/off dur to a built-in muting circuit
* Good ripple rejection due to a built-in ripple filter
* Good channel separation
* Soft tone at the time of output straiten
* Closed loop voltage gain fixed 45dB (Bridge: 51dB) but availability with external resistor added
* Minimum number of external parts required
* Easy to design radiator fin

■ ORDERING INFORMATION

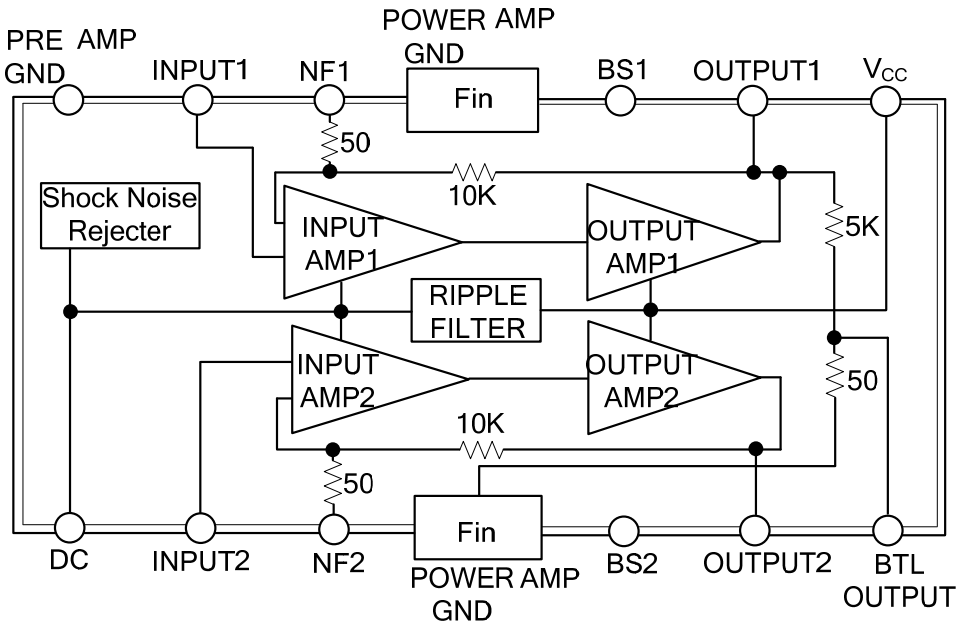
Order Number		Package	Packing
Lead Free	Halogen Free		
TEA2025AL-D12-H-T	TEA2025AG-D12-H-T	DIP-12H	Tube

TEA2025AL-D12-H-T (1)Packing Type (2)Package Type (3)Lead Plating	(1) T: Tube (2) D12-H: DIP-12H (3) G: Halogen Free, L: Lead Free

■ PIN CONFIGURATION



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS (T_A=25°C, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_S	15	V
Power Dissipation	P_D	4	W
Operating Temperature	T_{OPR}	-20~+70	°C
Storage Temperature	T_{STG}	-40~+150	°C

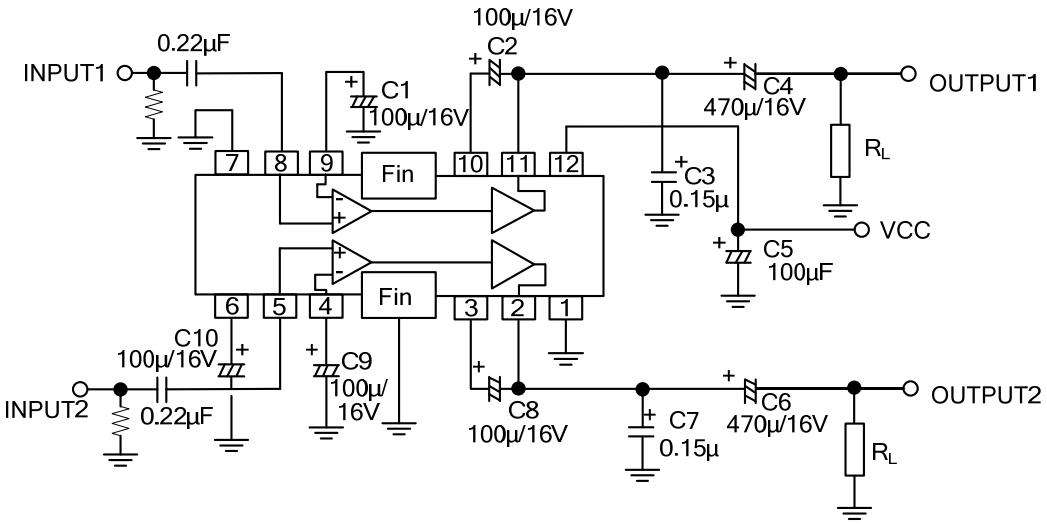
Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ ELECTRICAL CHARACTERISTICS (T_A=25°C, R_G=600V, Stereo, unless otherwise specified.)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage	V_{CC}		3		12	V
Quiescent Current	I_{CC}	Vi=0, Stereo		40	50	mA
Closed Loop Voltage Gain	A_V	Stereo, Vi=-45dBm	43	45	47	dB
		Bridge, Vi=-45dBm	49	51	53	dB
Channel Balance	C_B	Stereo	-1	0	+1	dB
Output Power	P_O	Stereo, R_L=4Ω, THD=10%	1.7	2.3		W
		Stereo, R_L=8Ω, THD=10%		1.3		W
		Bridge, R_L=8Ω, THD=10%		4.7		W
Total Harmonic Distortion	T_{HD}	Stereo, Po=250mW, R_L=4Ω		0.3	1.5	%
		Bridge, Po=250mW, R_L=4Ω		0.5		%
Input Resistance	R_I		21	30		KΩ
Rijpple Rejection	R_R	Stereo, Rg=0Ω, Vr=150mV, f=100Hz	40	46		dB
Output Noise Voltage	V_{NO}	Stereo, Rg=0Ω		1.5	3	mV
		Stereo, Rg=10KΩ		3	6	mV
Cross-Talk	C_T	Stereo, Rg=10KΩ, Vo=0dBm	40	55		dB

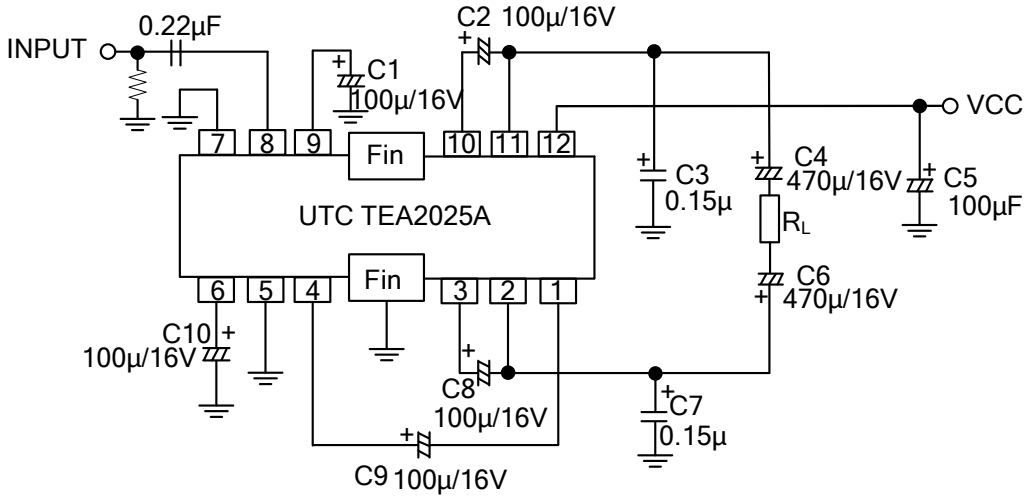
■ APPLICATION IN FORMATION

Stereo Amplifier



Polyester film capacitor

Bridge Amplifier



Polyester film capacitor

■ APPLICATION INFORMATION

Input Capacitor

Input capacitor is PNP type allowing source to be referenced to ground. In this way no input coupling capacitor is required. However, a series capacitor (0.22 uF)to the input side can be useful in case of noise due to variable resistor contact.

Bootstrap

The bootstrap connection allows to increase the output swing. The suggested value for the bootstrap capacitors (100uF) avoids a reduction of the output signal also at low frequencies and low supply voltages.

Voltage Gain Adjust

STEREO MODE (Figure 1)

The voltage gain is determined by on-chip resistors R1 and R2 together with the external RfC1 series connected between pin 6 (11) and ground. The frequency response is given approximated by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1}{R_f + R_2 + \frac{1}{JWC1}}$$

With R_f=0, C_1=100μF, the gain results 46 dB with pole at f=32 Hz.

The purpose of Rf is to reduce the gain. It is recommended to not reduce it under 36 dB.

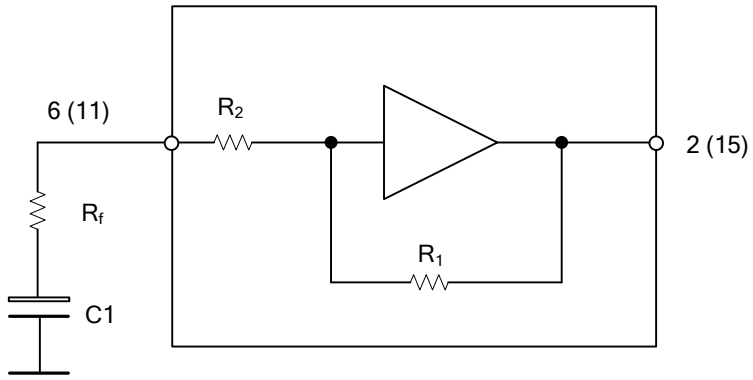


Figure 1

BRIDGE MODE (Figure 2)

The bridge configuration is realized very easily thanks to an internal voltage divider which provides (at pin 1) the CH 1 output signal after reduction. It is enough to connect pin 6 (inverting input of CH 2) with a capacitor to pin 1 and to connect to ground the pin 7.

The total gain of the bridge is given by:

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_1}{R_f + R_2 + \frac{1}{JWC1}} \left(1 + \frac{R_3}{R_4} \frac{R_1}{R_2 + R_4 + \frac{1}{JWC1}}\right)$$

and with the suggested values (C1 = C2 = 100 uF, R_f = 0) means: Gv = 52 dB with first pole at f = 32 Hz

■ APPLICATION INFORMATION(Cont.)

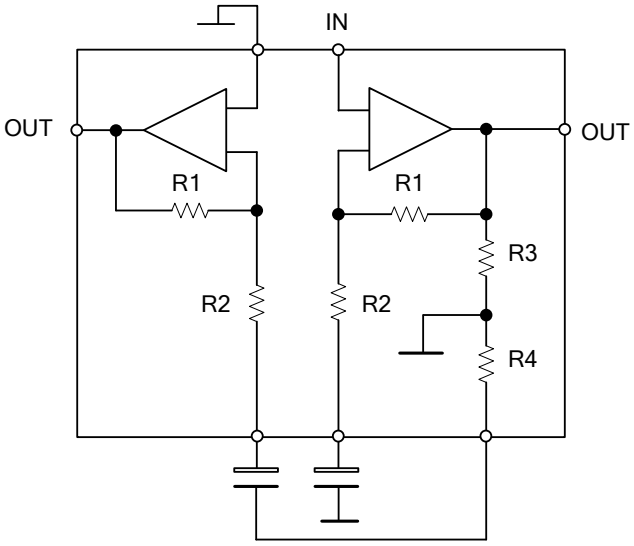


Figure 2

Output Capacitors

The low cut off frequency due to output capacitor depending on the load is given by:

$$F_L = \frac{1}{2\pi C_{OUT} \times R_L}$$

with C_{OUT} 470uF and R_L = 4 ohm it means F_L = 80Hz.

Pop Noise (Figure 3)

Most amplifiers similar to UTC **TEA2025A** need external resistors between DC outputs and ground in order to optimize the pop on/off performance and crossover distortion.

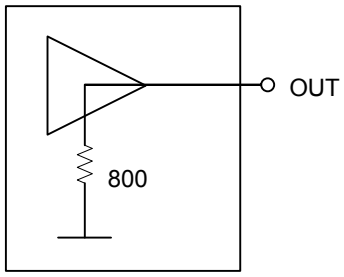


Figure 3

The UTC **TEA2025A** solution allows to save components because of such resistors (800 ohm) are included into the chip.

Stability

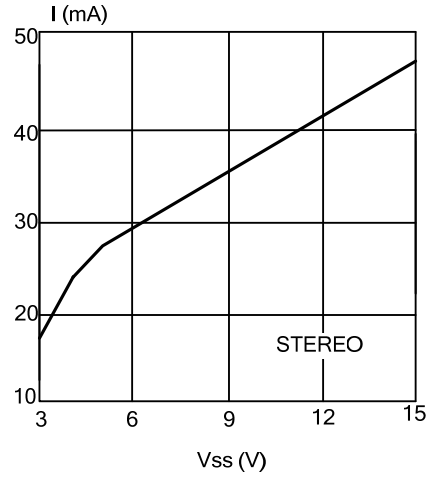
A good layout is recommended in order to avoid oscillations. Generally the designer must pay attention on the following points:

- Short wires of components and short connections.
- No ground loops.
- Bypass of supply voltage with capacitors as nearest as possible to the supply I. C. pin. The low value (poliester) capacitors must have good temperature and frequency characteristics.
- No sockets.

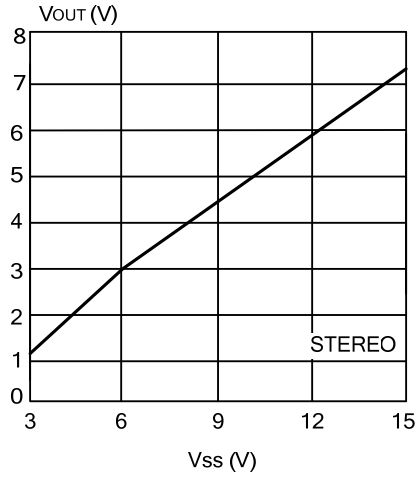
The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no device damage in the case of excessive junction temperature: all that happens is that P_O (and therefore P_{tot}) and Id are reduced.

■ TYPICAL CHARACTERISTICS

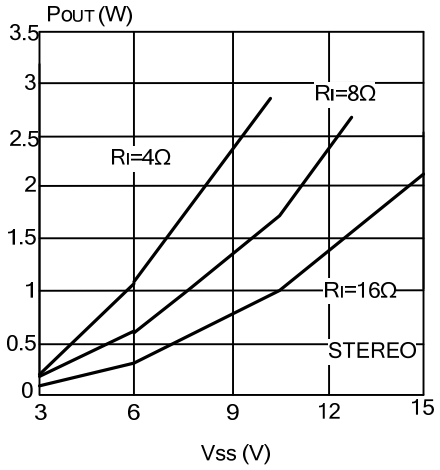
Supply Current vs.Supply Voltage
(R_L=4Ω)



Output Voltage vs. Supply Voltage



Output Power vs. Supply Voltage
(THD=10%, f=1KHz)



THD vs. Output Power
(f=1KHz, Vss=6V)