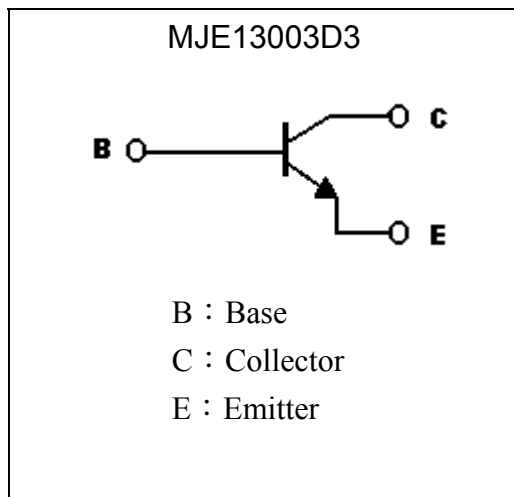
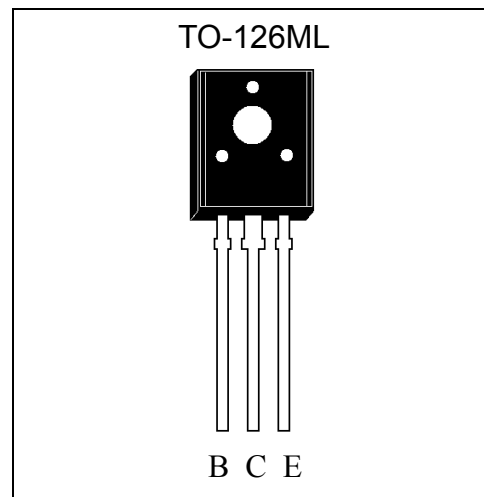


General Purpose NPN Epitaxial Planar Transistor

MJE13003D3

Features

- High breakdown voltage, $V_{CEO}=400V$ (min.)
- High collector current, $I_{C(max)}=1.5A$ (DC)
- Pb-free package

Symbol

Outline

Absolute Maximum Ratings ($T_a=25^\circ C$)

Parameter	Symbol	Limits	Unit
Collector-Base Voltage	V_{CBO}	700	V
Collector-Emitter Voltage	V_{CEO}	400	V
Emitter-Base Voltage	V_{EBO}	9	V
Collector Current(DC)	I_C	1.5	A
Collector Current(Pulsed)	I_{CP}	3 (Note)	A
Base Current	I_B	0.2	A
Power Dissipation($T_A=25^\circ C$)	P_d	1.5	W
Power Dissipation($T_C=25^\circ C$)		20	W
Junction Temperature	T_j	150	$^\circ C$
Storage Temperature	T_{stg}	-55~+150	$^\circ C$

 Note : Single pulse, $P_w \leq 300\mu s$, Duty Cycle $\leq 2\%$.

**Characteristics (Ta=25°C)**

Symbol	Min.	Typ.	Max.	Unit	Test Conditions
BV _{CBO}	700	-	-	V	I _C =100μA
BV _{CEO}	400	-	-	V	I _C =10mA
BV _{EBO}	9	-	-	V	I _E =2mA
I _{CBO}	-	-	10	μA	V _{CB} =700V, I _E =0
I _{CEO}	-	-	500	μA	V _{CE} =400V, I _E =0
I _{EBO}	-	-	10	μA	V _{EB} =9V, I _C =0
*V _{CE(SAT)}	-	-	300	mV	I _C =500mA, I _B =100mA
*V _{CE(SAT)}	-	-	600	mV	I _C =1A, I _B =250mA
*V _{BE(SAT)}	-	-	1.2	V	I _C =1A, I _B =250mA
*h _{FE 1}	10	-	30	-	V _{CE} =5V, I _C =500mA
*h _{FE 2}	5	-	-	-	V _{CE} =5V, I _C =1.5A
f _T	5	-	-	MHz	V _{CE} =10V, I _C =100mA, f=100MHz
t _{stg}	-	-	0.5	μs	V _{CC} =100V, I _C =1A, I _{B1} =-I _{B2} =0.2A, I _C =0.25A
t _r	1.8	-	6.6		

*Pulse Test: Pulse Width ≤380μs, Duty Cycle ≤2%

Classification Of h_{FE}

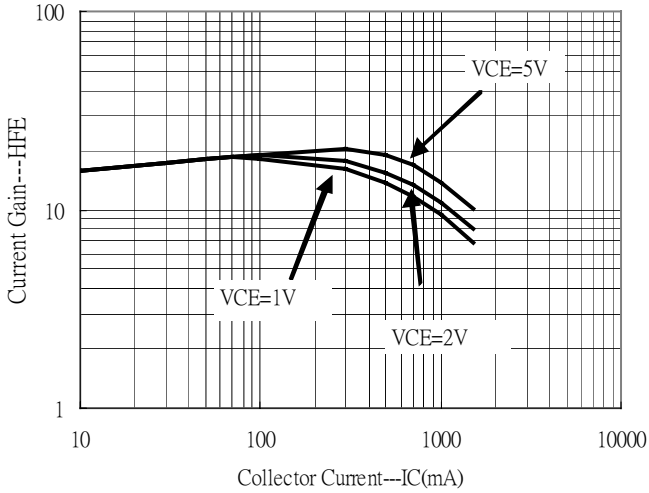
Rank	A	B	C	D
Range	10~15	15~20	20~25	25~30

Ordering Information

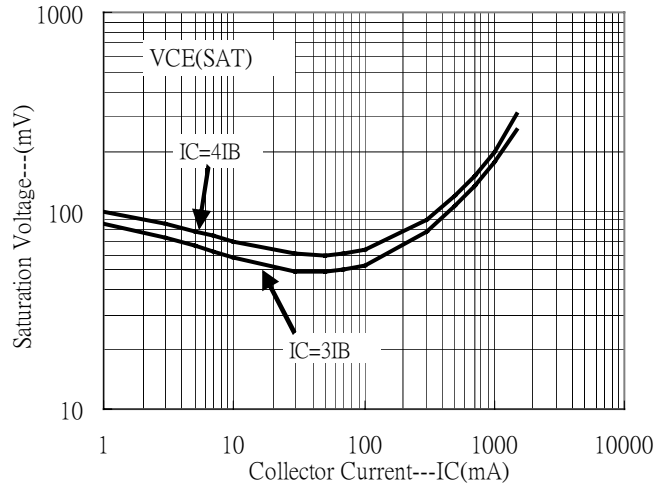
Device	Package	Shipping	Marking
MJE13003D3	TO-126ML (Pb-free)	200 pcs / Bag, 15 Bags/Box, 10 Boxes/Carton	13003

Characteristic Curves

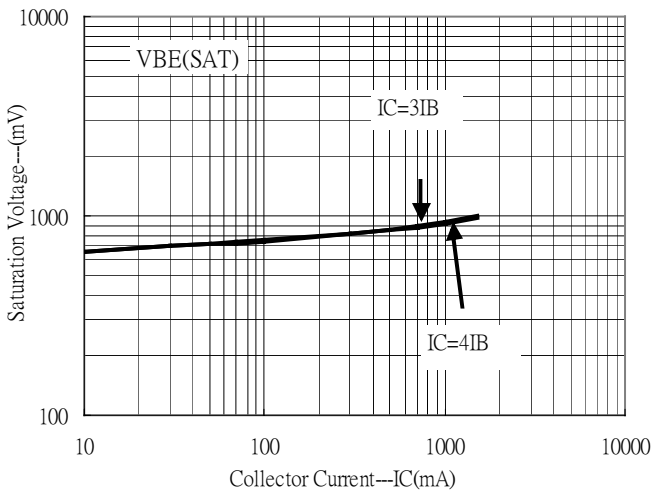
Current Gain vs Collector Current



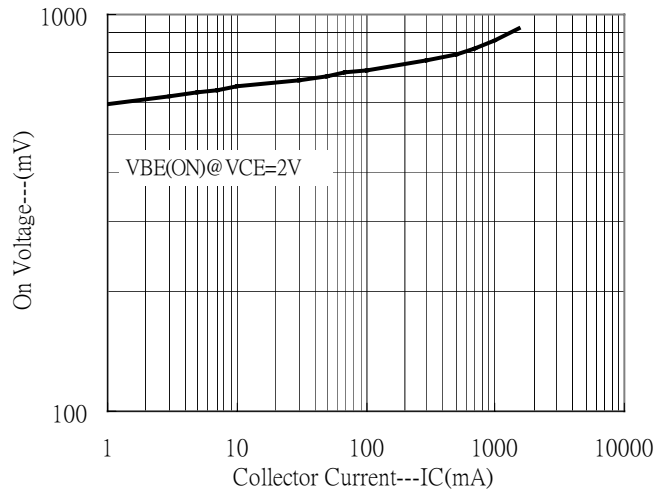
Saturation Voltage vs Collector Current



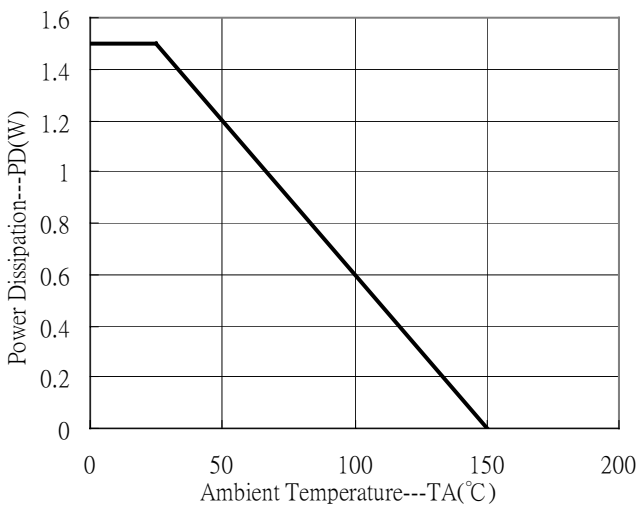
Saturation Voltage vs Collector Current



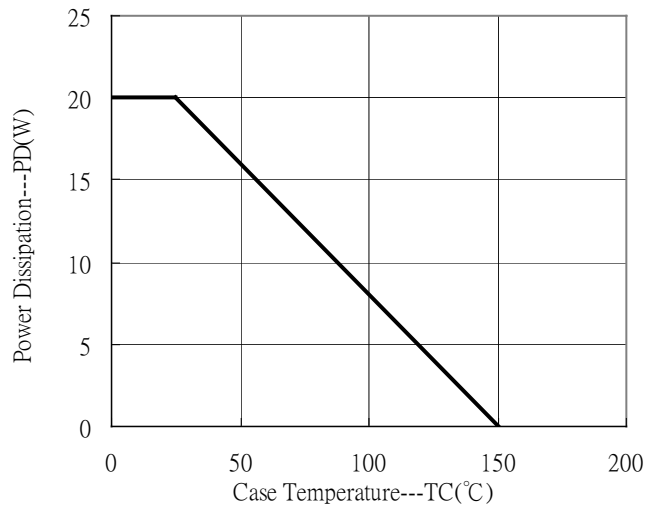
On Voltage vs Collector Current



Power Derating Curve



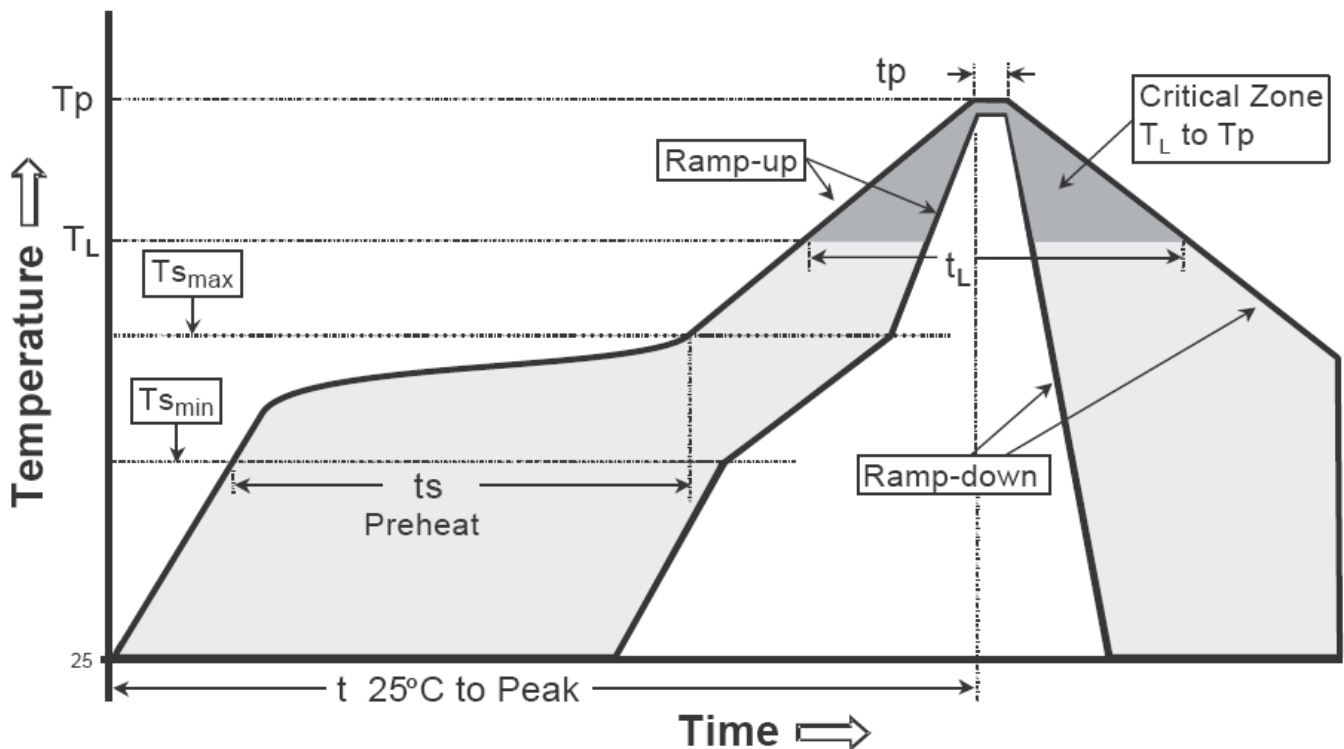
Power Derating Curve



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

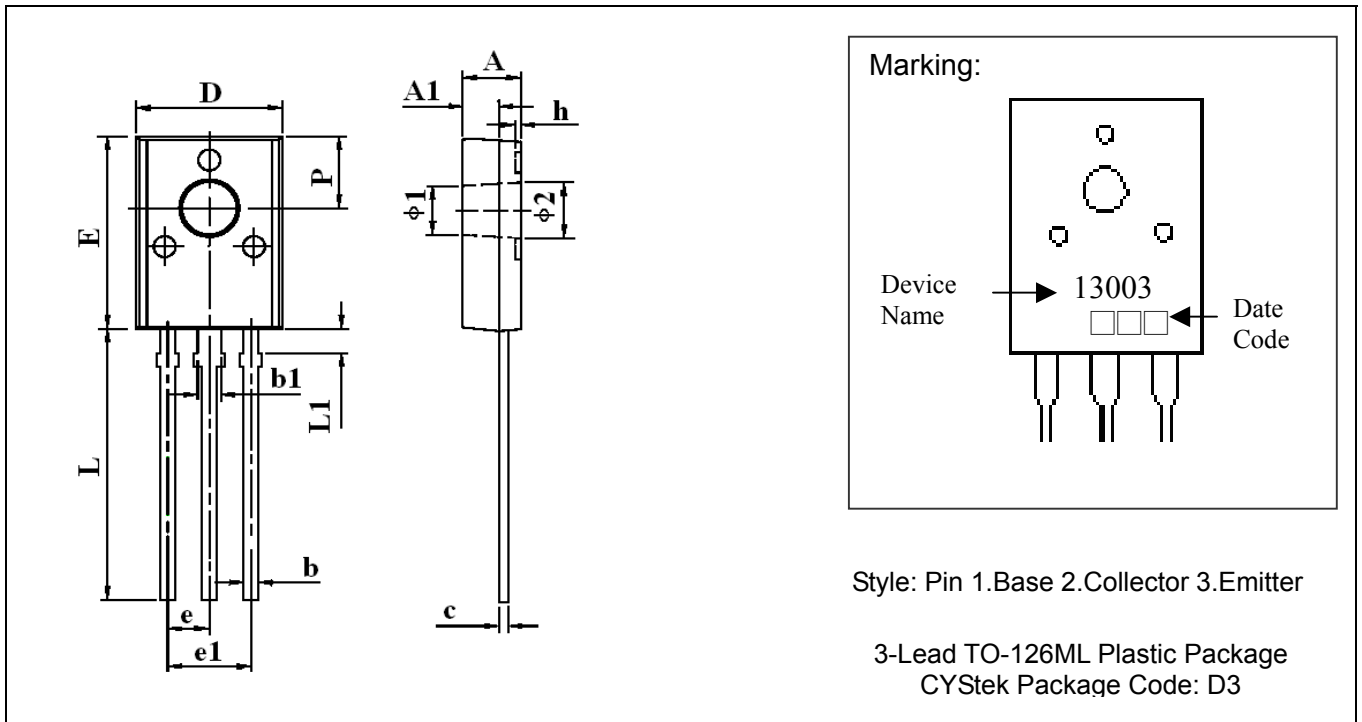
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(Ts min)	100°C	150°C
-Temperature Max(Ts max)	150°C	200°C
-Time(ts min to ts max)	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (TL)	183°C	217°C
- Time (tL)	60-150 seconds	60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

TO-126ML Dimension



*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.118	0.134	3.000	3.400	e	*0.090		*2.28	
A1	0.071	0.087	1.800	2.200	e1	0.176	0.183	4.460	4.660
b	0.026	0.034	0.660	0.860	L	0.594	0.610	15.100	15.500
b1	0.046	0.054	1.170	1.370	L1	0.051	0.059	1.300	1.500
c	0.018	0.024	0.450	0.600	P	0.159	0.167	4.040	4.240
D	0.307	0.323	7.800	8.200	Φ ₁	0.118	0.126	3.000	3.200
E	0.425	0.441	10.800	11.200	Φ ₂	0.122	0.130	3.100	3.300

Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: KFC ; solder plating
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0

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