MP8832

Triple 8-Bit High Speed ADC with Gamma Compensated References

March 1998-3

FEATURES

- 3 Independent 8-bit ADCs
- Simultaneous Sampling @ 4 MSPS
- Independent Digitally Controlled References with Proprietary Gamma Compensation
- 7-bit Positive Reference and 5-bit Negative Reference Adjustment Resolution
- On-Chip Reference
- Internal SH: 10MHz Input -3dB Frequency
- Single 5V Supply
- ADC (Full Scale) Range 1.25V to 2.5V
- ADC Offset Range 0.45V to 0.60V
- CMOS Low Power: 300mW (typ.)
- Zero Level Output
- Latch-Up Free

BENEFITS

- Digitally Controlled Gamma Correction: Improves Effective Resolution over Software Correction Schemes
- Digitally Controlled Gain and Offset Adjustment: Reduced DSP Demands and Reduction of Parts Count and System Cost

APPLICATIONS

- Precision Color Scanners
- Precision Color Digital Cameras
- Digital Color Copiers
- IR Camera

GENERAL DESCRIPTION

The MP8832 is a simultaneous sampling 4.0 MSPS triple Analog-to-Digital Converter (ADC) with an on-chip voltage reference. Each ADC has a 7-bit DAC driving its positive reference input and a 5-bit DAC driving its negative reference input to adjust the gain and offset of ADCs independently. This makes possible the correction of analog input gain and offset from sample-to-sample (e.g. pixel-to-pixel) by loading the DAC digital inputs from an external correction memory. In addition, the MP8832 incorporates a proprietary gamma-correction circuit to adjust the transfer function of each ADC independently by providing an eight segment approximation. The value of gamma is from 1.0 to 2.0 and controlled by a 4-bit DAC to provide 16 sets of correction value for each 8 segments of the transfer function. This simple and programmable function enables the user to define the dynamic range of each ADC relative to input signal values. A near 11-bit dynamic range is achieved for the smaller codes of the ADC transfer function by using the gamma-correction.

Two separate 7-bit and 5-bit I/O ports are used to update the gain and offset DACs before each sample.

An 8-bit I/O port sequentially outputs the digitized value of each channel (ADC) after each conversion period. The same I/O port could be used to write or read the gain and offset DAC's digital input codes.

The MP8832 uses ADCs with a sub-ranging architecture to maintain low power consumption at high conversion rates. Our proprietary comparator design achieves a low analog input capacitance and performs an on-chip sample and hold function. The MP8832 uses proprietary high speed DACs to drive the ADC references which allows reference adjustment on every conversion at a 4.0MHz rate.

The MP8832 operates from a single 5V supply and an internal 1V reference and consumes only 300mW of power. Specified for operation over the temperature range -40°C to +85°C, the MP8832 is available in a 44 lead Plastic Quad Flat Pack (PQFP) package.

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ORDERING INFORMATION

Part No.	Package	Operating Temperature Range
MP8832AE	44-Lead PQFP (10 mm x 10 mm)	-40°C to +85°C

BLOCK DIAGRAM

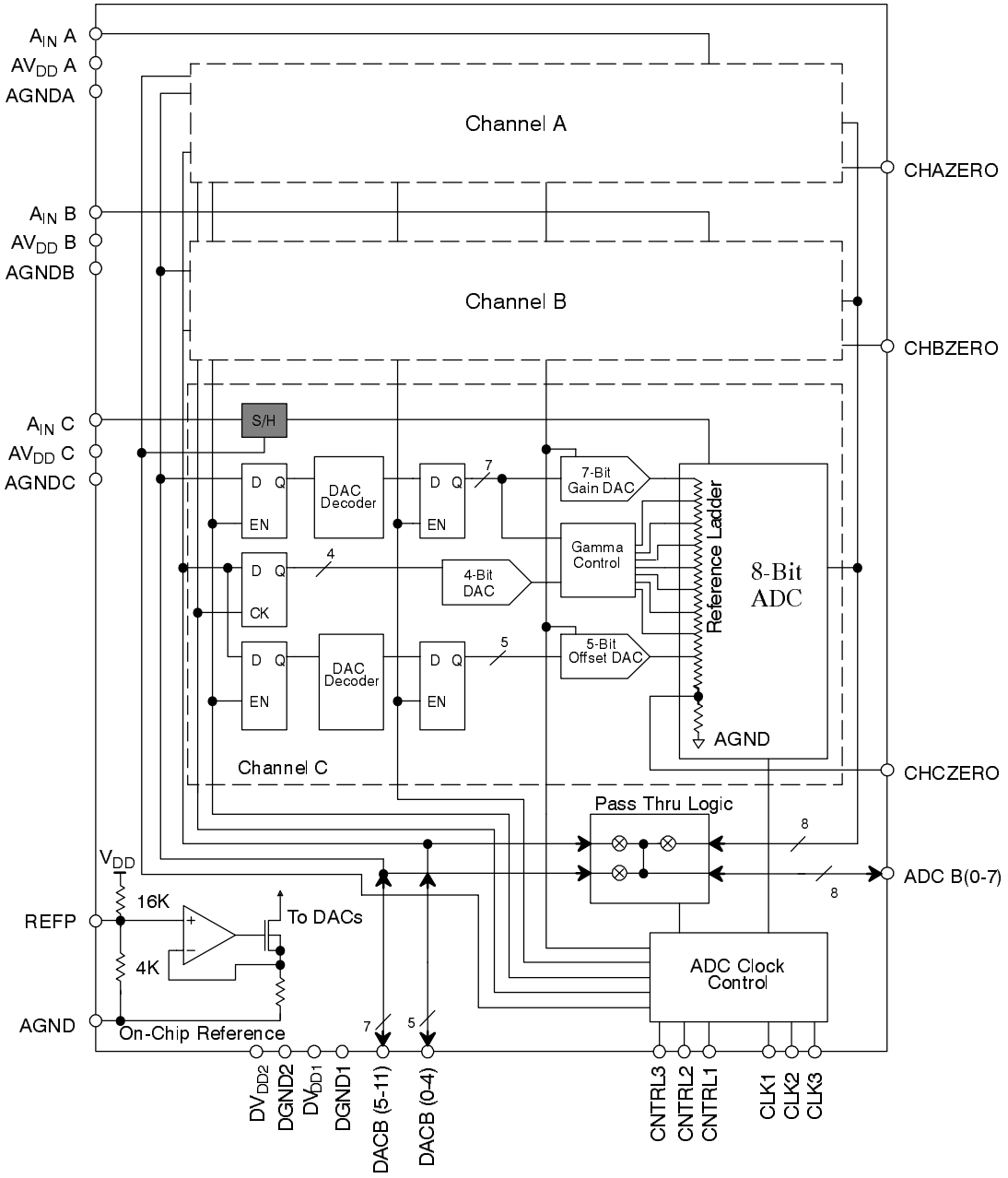
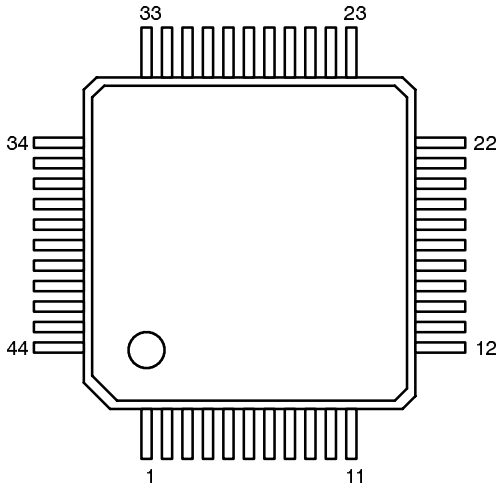


Figure 1. Block Diagram

PIN CONFIGURATION



44 Lead PQFP (10 mm x 10 mm)

PIN DESCRIPTION

Pin #	Symbol	Description
1	DACB1	DAC Data Bit 1.
2	DACB2	DAC Data Bit 2.
3	DACB3	DAC Data Bit 3.
4	DACB4	DAC Data Bit 4 (MSB Offset DAC).
5	DACB5	DAC Data Bit 5 (LSB Gain DAC).
6	DACB6	DAC Data Bit 6.
7	DACB7	DAC Data Bit 7.
8	DACB8	DAC Data Bit 8.
9	DACB9	DAC Data Bit 9.
10	DACB10	DAC Data Bit 10.
11	DACB11	DAC Data Bit 11 (MSB Gain DAC).
12	CHCZERO	Internal Ground Reference Monitor.
13	$A_{IN}C$	Analog Input, Channel C.
14	AGNDC	Analog Ground, Channel C.
15	$AV_{DD}C$	Analog Positive Supply, Channel C.
16	CHBZERO	Internal Ground Reference Monitor.
17	$A_{IN}B$	Analog Input, Channel B.
18	AGNDB	Analog Ground, Channel B.
19	$AV_{DD}B$	Analog Positive Supply, Channel B.

PIN DESCRIPTION (CONT'D)

Pin #	Symbol	Description
20	REFP	Positive Reference Input.
21	AGND	Analog Ground.
22	CHAZERO	Internal Ground Reference Monitor.
23	$A_{IN}A$	Analog Input, Channel A.
24	AGNDA	Analog Ground, Channel A.
25	$AV_{DD}A$	Analog Positive Supply, Channel A.
26	CNTRL1	Mode Control 1.
27	CNTRL2	Mode Control 2.
28	CNTRL3	Mode Control 3.
29	CLK3	Chip Control Clock 3.
30	CLK 2	Chip Control Clock 2.
31	CLK 1	Chip Control Clock 1.
32	DGND1	Digital Ground Supply 1.
33	$DV_{DD}1$	Digital Positive Supply 1.
34	ADCB0	ADC Data Bit 0 (LSB).
35	ADCB1	ADC Data Bit 1.
36	ADCB2	ADC Data Bit 2.
37	ADCB3	ADC Data Bit 3.
38	ADCB4	ADC Data Bit 4.
39	ADCB5	ADC Data Bit 5.
40	ADCB6	ADC Data Bit 6.
41	ADCB7	ADC Data Bit 7 (MSB).
42	DGND2	Digital Ground 2.
43	$DV_{DD}2$	Digital Positive Supply 2.
44	DACB0	DAC Data Bit 0 (LSB Offset DAC).

ELECTRICAL CHARACTERISTICS

Test Conditions: DV_{DD} = AV_{DD} = 5.0 V, V_{REFP} = 1.0 V, T_A = 25°C, All INL Measurements use the Best Fit Straight Line Technique Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
ADC						
RADC	Resolution		8		Bits	
DNL	Differential Non-Linearity	-1.0		1.0	LSB	Guaranteed monotonic GD = 00h, OD = 0h
INL	Integral Non-Linearity	-2.0		2	LSB	Best Fit Line, Gamma = 0h, GD = 00h, OD = 0h
$A_{IN}pp$	Analog Input Full Scale Range[2]	0.475		2.75	V	Over all DAC codes
ΔA_{IN}	Input Voltage Change			100	% FS	Sample to Sample
C_{IN}	Input Capacitance		20		pF	A_{IN} = 2.5V
E_{ZS}	Zero Scale Error		150		mV	
E_{FS}	Full Scale Error		2.0		% FS	Gamma = 0000
	Effective Sample Rate		4.0		MSPS	Per Channel
Offset DAC						
RODAC	Resolution		5		Bits	
DNL	Differential Non-Linearity[4]	-3/4		3/4	LSB	
INL	Integral Non-Linearity	-1.0		1.5	LSB	Best Fit Line[3]
V_{FS}	Full Scale Range		0.151		V	
VO_Z	Effective Zero Voltage	0.45	0.475	0.50	V	Code = 00000
VOE_{FS}	Effective Full Scale Voltage	0.60	0.625	0.65	V	Code = 11111
Gain DAC						
RG–DAC	Resolution		7		Bits	
DNL	Differential Non-Linearity[3]	-1		1	LSB	
INL	Integral Non-Linearity	-2		2	LSB	Best Fit Line, Gamma = 0000[2]
	Nominal Full Scale Range		1.25		V	Same as ADC
VO_Z	Effective Zero Voltage	1.1	1.125	1.35	V	Code = 00h, Referenced to Voff V_{REFP}=1.0
V_{GFS}	Effective Full Scale Voltage	2.25	2.5	2.75	V	Code = 7Fh, Referenced to Voff V_{REFP}=1.0
GC_{MAX}	Maximum Change per Conversion			30	% FSR	
Gamma DAC						
RγDAC	Resolution		4		Bits	
γ	Gamma Correction Range	1.0		2.0		
DNL	Differential Non-Linearity[1]	-1/2		1/2	LSB	
err_{TV}	Tap Voltage Error		±0.5	±1.5	%	Referenced to full scale and offset voltages
γACC	Gamma Curve Accuracy	-2.25	±1.5	2.25	% FSR	Best fit line to ideal gamma curve over all gamma codes (*Figure 9.*)

ELECTRICAL CHARACTERISTICS (CONT'D)

Test Conditions: DV_{DD} = AV_{DD} = 5.0 V, V_{REFP} = 1.0 V, T_A = 25°C, All INL Measurements use the Best Fit Straight Line Technique Unless Otherwise Specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Reference Voltages						
V_{REF}	Reference Voltage (Internal)	0.9	0.95	1.0	V	Internal V_{REF} is over-ridden if external V_{REF} is used.
V_{REF}	Reference Voltage (External)	0.9	0.95	1.0	V	
I_{REFB}	Reference Current[1]			50	µA	
R_{INR}	Reference Input Impedance[1]			4	kΩ	
Power Supplies						
AV_{DD}	Analog Supply Voltage	4.75	5.00	5.25	V	
DV_{DD}	Digital Supply Voltage	4.75	5.00	5.25	V	
I_{DD}	Total Supply Current		55	100	mA	I_{DVDD} + I_{AVDD}
Digital Characteristics						
V_{INH}	Digital High Input Voltage	3.5			V	
V_{INL}	Digital Low Input Voltage			1.5	V	
I_{IN}	Input Current	–10		+10	µA	
C_{IN}	Input Capacitance[1]			10	pF	
V_{OH}	High Output Voltage	4.5				I_{SOURCE} = 2 mA
V_{OL}	Low Output Voltage			0.5	V	I_{SINK} = 2 mA
	High-Z Leakage[1]		±10		µA	

Notes

[1] Not production tested.

[2] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[3] Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

[4] V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

Specifications are subject to change without notice

ABSOLUTE MAXIMUM RATINGS (T_A = +25°C unless otherwise noted)[1, 2, 3]

V_{DD} to GND 6V

All Inputs ..... V_{DD} +0.5 to GND -0.5V

Storage Temperature ..... -65 to +150°C

Lead Temperature (Soldering 10 seconds) .. +300°C

ESD Rating (on all pins) 2000V

Package Power Dissipation Rating @ 75°C

QFP 1000mW

Derates above 75°C ..... 25mW/°C

Storage Temperature ..... -65 to +150°C

Notes:

[1] Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation at or above this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

[2] Any input pin which can see a value outside the absolute maximum ratings should be protected by Schottky diode clamps (HP5082-2835) from input pin to the supplies. All inputs have protection diodes which will protect the device from short transients outside the supplies of less than 100mA for less than 100µs.

CLK1	CLK2	CLK3	Action
1	1	↑	DAC gain and offset data read into DACA register.
↓	1	1	ADC samples the analog input, The analog input should not be slewing at this time. Data from previous ADCA conversion written to data bus.
↑	1	1	ADCs makes MSB comparison. DAC gain and offset data read into DACB register.
1	↓	1	Data from previous ADCB conversion written to data bus.
1	↑	1	ADCs makes LSB comparison, DACs must be settled at this time. DAC gain and offset data read into DACC register.
1	1	↓	The gain and offset DACs are updated on the falling edge of CLK–3 and the ADC starts to track the input.
1	1	↑	Error correction done and data passed to output registers.

Table 1. MP8832 Simplified Functional Description (Control in Normal Conversion Mode)

CNTRL1	CNTRL2	CNTRL3	Description of Operation
0	1	0	Normal operation / conversion mode.
0	0	0	Conversion Mode / DAC not updated.
1	0	0	Pass-through mode, data present on the ADC(0-4) bus will be written to the DAC(0-4) via internal bus control.
1	0	1	Pass-through mode, data present on the ADC(0-6) bus will be written to the DAC(5-11) via internal bus control.
1	1	0	Pass-through mode, data present on the DAC(0-4)bus will be written to the ADC(0-4) via internal bus control.
1	1	1	Pass-through mode, data present on the DAC(5-11) bus will be written to the ADC(0-6) via internal bus control.
0	1	1	Gamma DAC write mode. Data present on the DAC(0-4) bus will be latched to the Gamma DACs on the rising edge of CLK1, 2, and 3
0	0	1	DAC Test Mux enabled (address controlled by CLK1, 2, and 3). Refer to Figures 1, 2, and 3.

Table 2. Control Word Truth Table

Clock / Data I/O Timing	Time Interval	Time	Unit	Comments
Delay ClkC to ClkA	t1	50	ns typ	
Delay ClkA to ClkB	t2	30	ns min	
Delay ClkB to ClkC	t3	30	ns min	
Clk1 Pulse Width	t4	50	ns min	
Clk2 Pulse Width	t5	50	ns min	
Clk3 Pulse Width	t6	30	ns min	
DAC Data Hold Time	t7	10	ns min	
DAC Data Setup Time	t8	15	ns min	
Data Access Time	t9	25	ns max	C_{load} = 40pf
Data Bus Relinquish Time	t10	20	ns max	
Aperture Delay	t_{AP}	25	ns max	
Pass-through Write Propagation Delay (ADC bus to DAC bus)	t11	35	ns max	C_{load} = 40pf
Pass-through Read Propagation Delay (DAC bus to ADC bus)	t12	35	ns max	C_{load} = 40pf
CNTRL3 to Data Bus Relinquish	t13	20		
CNTRL3 to Data Bus Valid	t14	25	ns max	
CNTRL1 to Data Bus Relinquish	t15	20		
CNTRL3 to Data Bus Valid	t16	25		
CNTRL1 to Data Bus Valid	t17	25		

Table 3. Digital Timing Specifications

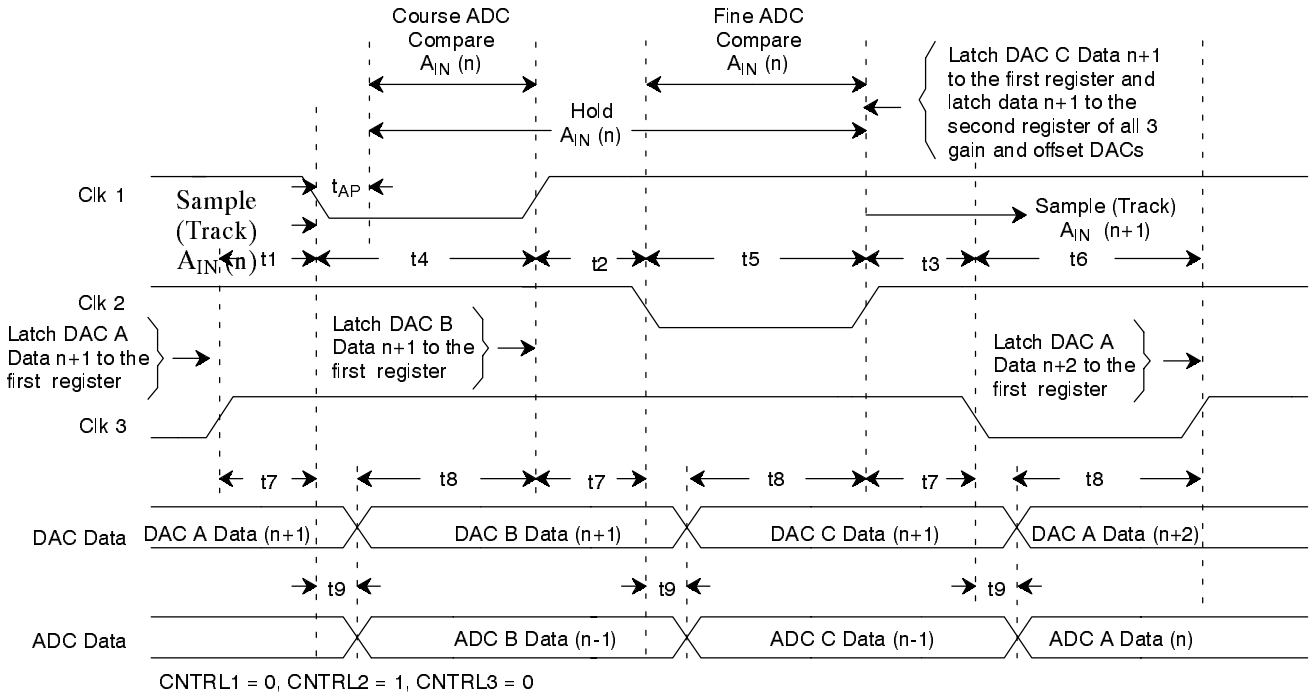


Figure 2. MP8832 Clock Timing Diagram

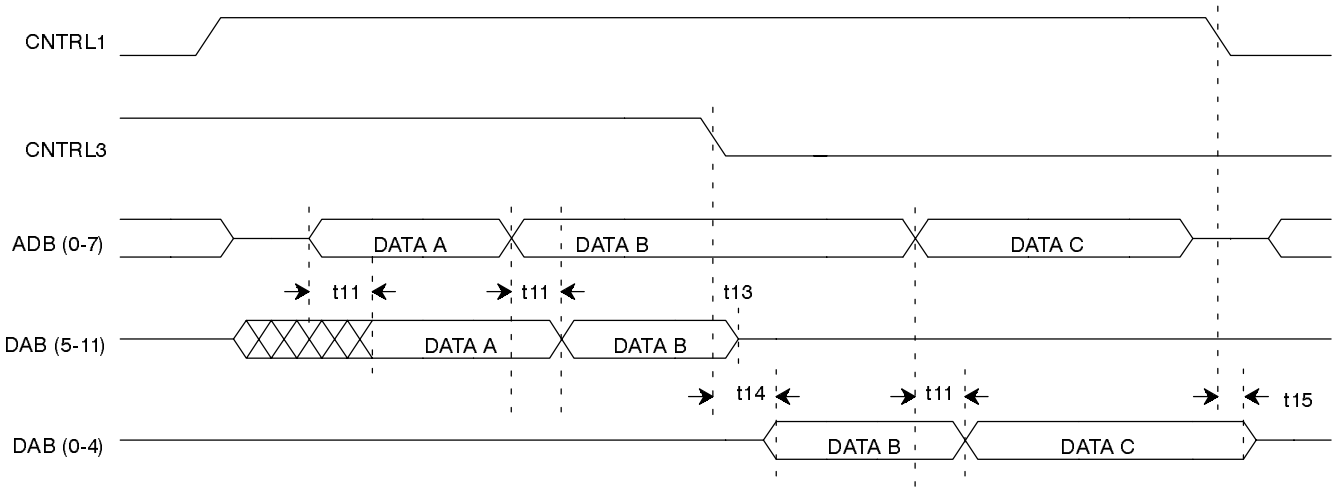


Figure 3. Write-Through Mode Timing CNTRL2 = 0 (ADC Port to DAC Port)

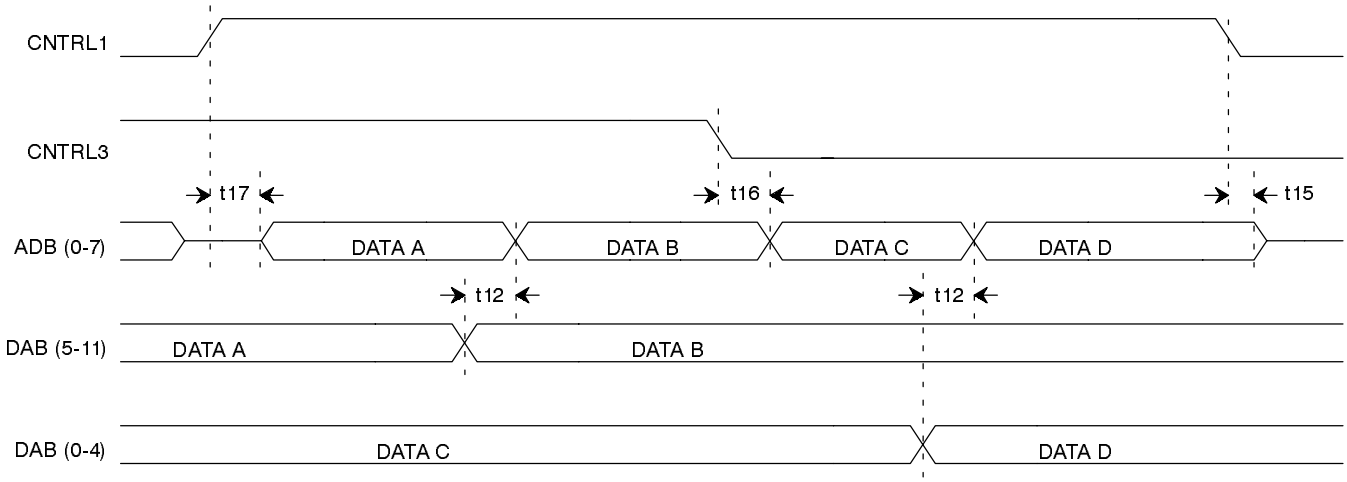


Figure 4. Write-Through Mode Timing CNTRL2 = 1 (DAC Port to ADC Port)

ADC ANALOG INPUT

The MP8832 part has a switched capacitor type input circuit. This means that the input impedance changes with each phase of the input clocks. *Figure 5.* shows an equivalent input circuit.

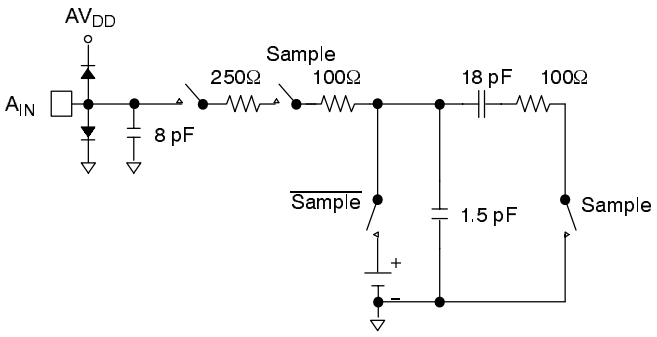


Figure 5. ADC Equivalent Input Circuit

ADC Gain and Offset and Relationship to DAC Data

Each channel of the MP8832 contains a 8-bit ADC, a 8-bit DAC, with the MSB internally set high (7 active bits), driving the positive reference and a 5-bit DAC driving the negative reference of the ADC's ladder network. The relationship between the ADC gain and offset and the DAC Data can be expressed mathematically. Assign the terms VRT and VRB to represent the voltages for the ADC full scale and zero levels respectively. Code gain and Code off represent the digital value for the gain and offset parameters set by the DACs.

VRT and VRB are defined by the equations:

$$V_{OFF} = \left\{\left(\frac{Code_{OFF}}{2^5}\right) \cdot 0.156\right\} \cdot V_{REF} + 0.45$$

$$V_{FS} = \left\{\left(1 + \frac{Code_{GAIN}}{2^7}\right) \cdot 1.25\right\} \cdot V_{REF} + V_{RB}$$

therefore the ADC input range is given by:

$$A_{INPP} = V_{RT} - V_{RB}$$

$$= \left\{\left(1 + \frac{Code_{GAIN}}{2^7}\right) \cdot 1.25\right\} \cdot V_{REF}$$

Gamma DAC

The MP8832 incorporates a proprietary internal gamma correction circuit that adjust the linearity of the ADC to provide an eight segment approximation of the function:

$$Code = \left(\frac{V_{IN}}{V_{REF}}\right)^{1/r} * (2^n - 1)$$

Where γ has a value of 1.0 to 2.0, and n is the number of bits in the ADC. The value of gamma (γ) is controlled using a 4-bit DAC to provide 16 steps of correction given in *Table 4.* The values for the codes between each tap point is a linear interpolation between each of the corresponding tap point voltages. This results in small errors for these codes when referred to the ideal gamma transfer curve as shown in *Figure 8.* The value of gamma is written to the MP8832 by setting CNTRA(1-3) to 011 and writing the gamma word for each ADC to the DCB(0-4) port similar to normal operation. The DAC's are immediately updated on the falling edge of each of the clock inputs. During the time when the circuit is in the gamma write mode the ADC is non-operable and the data present at the output of the ADC port is invalid. Gamma DAC write timing is shown in *Figure 6.*

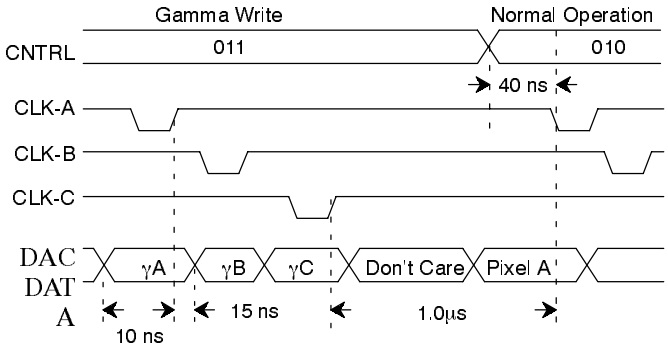


Figure 6. Gamma DAC Write Timing Diagram

Gamma Code (hex)	Min. Error Gamma Value*	Normalized Tap Voltage (Code)							
		32	64	96	128	160	192	224	256
0	1.0000	0.125	0.250	0.375	0.500	0.625	0.750	0.875	1.000
1	1.0434	0.118	0.238	0.359	0.483	0.609	0.738	0.868	1.000
2	1.0887	0.110	0.225	0.344	0.467	0.594	0.725	0.860	1.000
3	1.1361	0.103	0.213	0.328	0.45	0.578	0.713	0.853	1.000
4	1.1859	0.096	0.200	0.313	0.433	0.563	0.700	0.846	1.000
5	1.2382	0.089	0.188	0.297	0.417	0.547	0.688	0.839	1.000
6	1.2933	0.081	0.175	0.281	0.400	0.531	0.675	0.831	1.000
7	1.3516	0.074	0.163	0.266	0.383	0.516	0.663	0.824	1.000
8	1.4134	0.067	0.150	0.250	0.367	0.500	0.650	0.817	1.000
9	1.4792	0.059	0.138	0.234	0.350	0.484	0.638	0.809	1.000
A	1.5495	0.052	0.125	0.219	0.333	0.469	0.625	0.802	1.000
B	1.6251	0.045	0.113	0.203	0.317	0.453	0.613	0.795	1.000
C	1.7067	0.038	0.100	0.188	0.300	0.438	0.600	0.788	1.000
D	1.7954	0.030	0.088	0.172	0.283	0.422	0.588	0.780	1.000
E	1.8926	0.023	0.075	0.156	0.267	0.406	0.575	0.773	1.000
F	2.0000	0.016	0.063	0.141	0.250	0.391	0.563	0.766	1.000

* Gamma value is chosen so that the error at code 96 equals zero.

Table 4. Normalized Ladder Tap Voltages

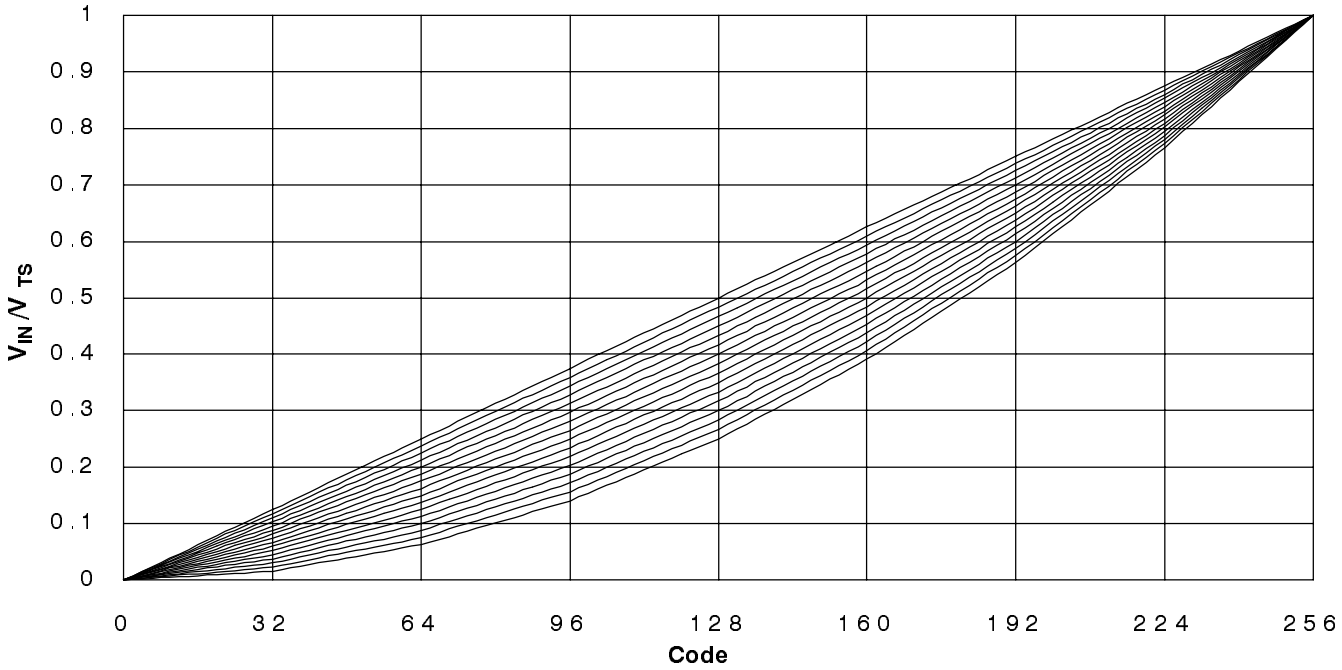


Figure 7. Transfer Function

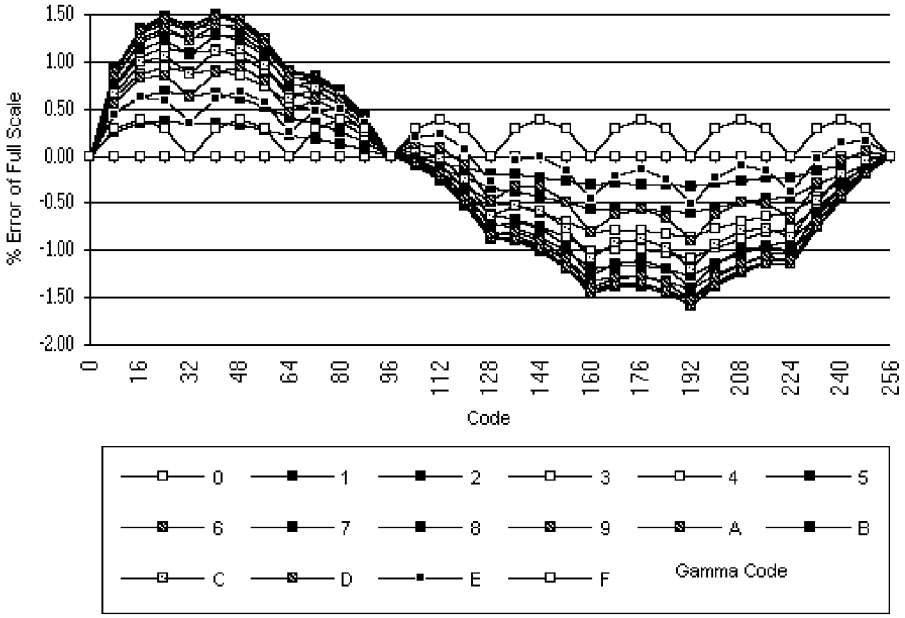


Figure 8. Error of Ladder Segment Approximation (Gamma is Curve Fit so that the Error of Code 96 Equals Zero)

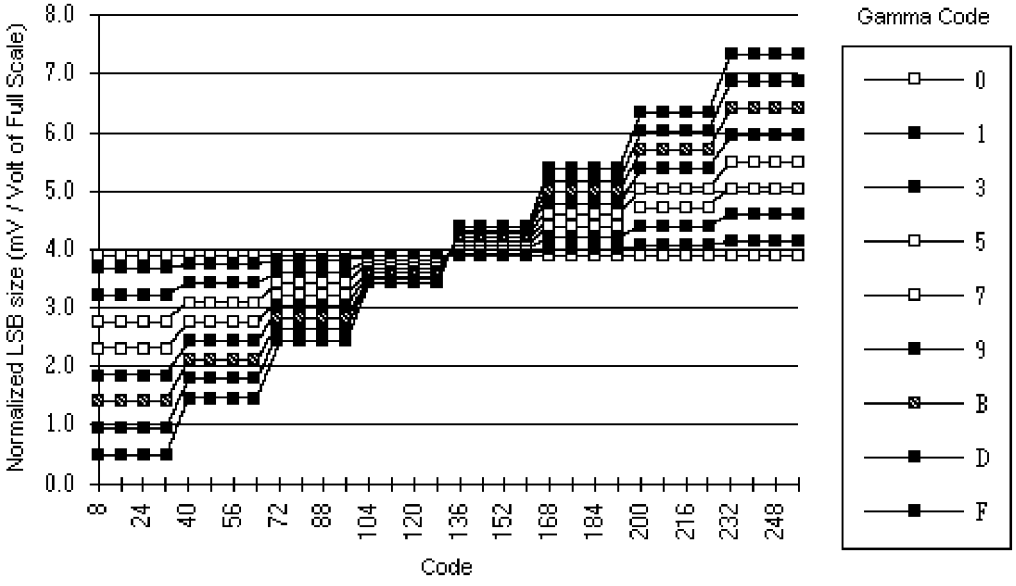


Figure 9. Normalized ADC LSB Size (LSB size normalized to the Full Scale Ladder Voltage Programmed via the Gain DAC

SUPPLY AND GROUNDS

DV_{DD} to DGND

A decoupling capacitor, preferably 0.1 μF high frequency ceramic, should be connected directly at the package across the digital supplies at pin 33 and 43. A DV_{DD} to DGND supply/ground plane should also be provided in the layout.

Analog Supply and Grounds

AGNDA, AGNDB, and AGNDC should be connected under the package to make their common impedance as low as possible. These AGND pins power the analog sections of the ADC and the circuitry in the DACs.

AGND is the analog ground related to DAC bias and should be connected to the analog ground using a star connection. The ADC ladder resistor terminates to this pin as well as the internal bias resistor used for setting the DAC reference.

$AV_{DD}A$, $AV_{DD}B$, and $AV_{DD}C$ should be connected to a common supply plane which forms a supply / ground plane with the analog ground plane. In addition, local decoupling, preferably a 0.1 μF high frequency ceramic, should be connected between each AV_{DD} pin and its closest analog ground.

Overview of Operation

The MP8832 is composed of three ADC converters with dynamic gain and offset and gamma controls, along with their associated analog and digital support circuitry. The three converters are intended to be used in a simultaneous sampling configuration. The only external circuitry required is a reference and input buffers.

The ADC Gain and Offset DAC inputs, ADC output data, and the A_{IN} sampling time are related to the three clock inputs (CLK1, CLK2, CLK3) as shown in *Figure 2.* To simplify board layout, a data pass-through configuration and mux is provided to allow bi-directional communication between the ADC data port and each of the DAC I/O ports.

A fast mode is provided, where only the 4 ADC MSBs are produced while the remaining data is set to 0(hex).

A zero reference voltage is provided for each channel and should be used as the ground reference for the analog buffer to increase the noise rejection of the overall system. In applications which require rejecting a bias level from the analog input, this output with the addition of minor circuitry can be used to reject the bias present during DCL= 0.

ADC System Overall Sequence

Assume that during the previous cycle, the values for the gains and offsets needed for this sample set have been loaded into the first DAC registers. This data is loaded into the second DAC registers for all 3 channels on the falling edge of CLK3 and the DACs begin to slew to their final value. All channels of the ADC begin tracking A_{IN} at this time as well.

The analog input sample for all three channels is taken at the falling edge of CLK1 after the aperture delay t_{AP}.

At the rising edge of CLK1, the Channel B gain and offset data for the next cycle is loaded into the Channel B first DAC register. The MSB comparators are also enabled and begin comparing at this time. At the rising edge of CLK1, the MSB value is latched and the range for the LSBs is selected. Note that the internal gain and offset DAC must be settled by this time in order for the MSB value to be correct. Because any system noise prior to the latching of the comparator outputs may cause errors, it is important that the DAC data for channel C be present at the DAC bus as long as possible prior to the rising edge of CLK2.

On the falling edge of CLK2, the ADC data for channel B is output to the ADC data bus.

At the rising edge of CLK2, the channel C gain and offset data for the next cycle is loaded into the channel C first DAC register. The LSB comparators have been selected, enabled and begin comparing at this time. At the rising edge of CLK2 the LSB value is latched. As with the MSBs previously, any system noise prior to the latching of the comparator outputs may cause errors. Therefore, it is important that the DAC data for channel C be present at the DAC bus as long as possible prior to the rising edge of CLK2.

During the time, when all the CLK inputs are high and during the CLK3 period, the MSB data is corrected if necessary and then propagated along with the LSB data to the ADC output registers. On the next falling edge of CLK1, the channel A data is enabled at the output port.

Since the actual ADC samples are taken at the falling edge of CLK1 after t_{AP} delay, during this period of time the ADC is the most sensitive to noise transitions from digital

components. Keep all digital transitions within the time window as few as possible. The internal logic to the MP8832 inhibits the outputting of data prior to the critical timing periods until after t_{AP}. Because of this delay, the hold time of the DAC data must be as long as t_{AP} for certain cases.

The gain and offset DACs data paths are double buffered so that the DAC data can be sequentially loaded on the falling edge of each of the three clock inputs CLK(1-2-3). The data to all of the DACs is then simultaneously updated on the falling edge of CLK3. This timing gives the ADC ladder sufficient time to settle prior to the MSBs comparing against the reference ladder. The gain and offset DAC registers are not reset internally upon power-up, and therefore initial gain and offset values must be written to the part using the normal operation sequence prior to initiating conversions. The gamma DACs, unlike the gain and offset DACs, are reset to zero (gamma=1.0) upon power up and do not have to be initiated. Additionally, the internal clock registers of the MP8832 are not reset upon power up and therefor at least one full clock sequence consisting of CLK-1, 2 and 3 is required.

The DAC data bus can be disabled and the data present in the DAC registers preserved by making CNTRL2=0 during the conversion process. This is useful for the cases where the gain and offset DACs do not have to be changed for each conversion . To insure that the data in the DAC registers is not corrupted, CNTRL2 should only be changed during the time t3.

The MP8832 can be put into a powered-down mode by taking all the input clocks low simultaneously. During power-down the ADC comparators are put into a latched state and the reference amps are turned off, thereby reducing the ADC ladder currents to zero. To insure that the comparators are in the proper state during power-on, the clock inputs should be brought high in the correct order as shown in *Figure 10.* If the power-on sequence cannot be adhered to, then two conversion cycles should be executed to ensure that all of the internal comparator and data registers are in the correct state. Because the reference amps are shut off during power-down, a delay of 20μs should be incurred to let the reference amp settle prior to starting ADC conversions.

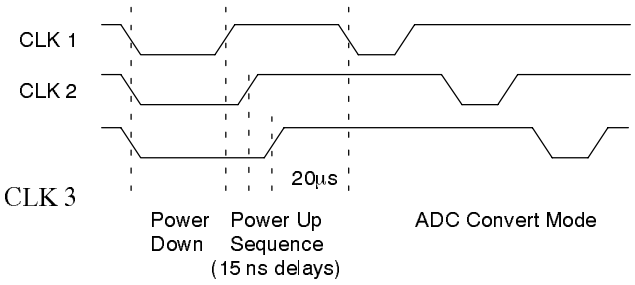


Figure 10. Power-Down/Up Sequence

Reference Voltage

A reference voltage of V_{DD}/5.3 V is internally generated between pins REFP and AGND of the MP8832. For low noise operation a 0.1μF capacitor should be placed between these two pins to reduce any noise that may be present at REFP pin. The operation of the MP8832 with external reference voltages can be implemented by applying an external reference voltage between REFP and AGND. The input impedance of REFP is typically 3.5K, so it it easily driven with most commonly used op amps.

Reference Ladder Test Mode

The internal zero and full scale voltage of the ADC, as well as the gamma tap voltages, can be measured by placing the MP8832 into the DAC test mode which is built into the part. This feature can be used to check the reference tap voltages in order to calibrate out any differences from ideal values. The MP8832 is placed into the test mode by setting the control bits to 001 as shown in *Table 4.* When in the DAC test mode the ADC outputs are connected to the ADC reference ladder using a mux. The CLK inputs control the mux address select which ladder tap to be connected to the ADC output bits as shown in *Table 5.* The ADC is not operational during DAC testing.

CLK 3	CLK 2	CLK 1	Channel A		Channel B		Channel C	
			ADB0	ADB1	ADB2	ADB3	ADB6	ADB7
0	0	1	Vt0	Vt255	Vt0	Vt255	Vt0	Vt255
0	1	0	Vt32	Vt224	Vt32	Vt224	Vt32	Vt224
0	1	1	Vt64	Vt192	Vt64	Vt192	Vt64	Vt192
1	0	0	Vt96	Vt160	Vt96	Vt160	Vt96	Vt160
1	0	1	Vt128	N/C	Vt128	N/C	Vt128	N/C

CNTRL1 = 0, CNTRL2 = 0, CNTRL3 = 1

Table 5. ADC Ladder/DAC Test Mode Control

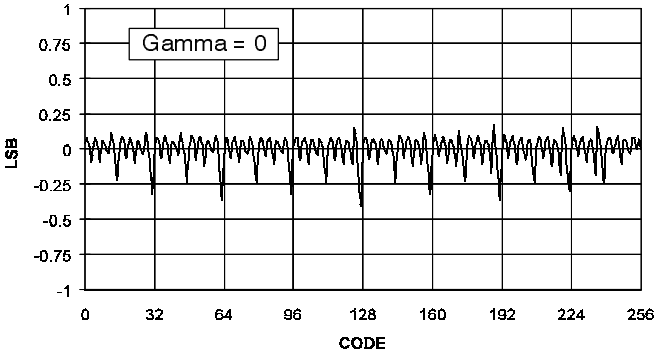


Figure 11. ADC DNL Error Plot Channel A

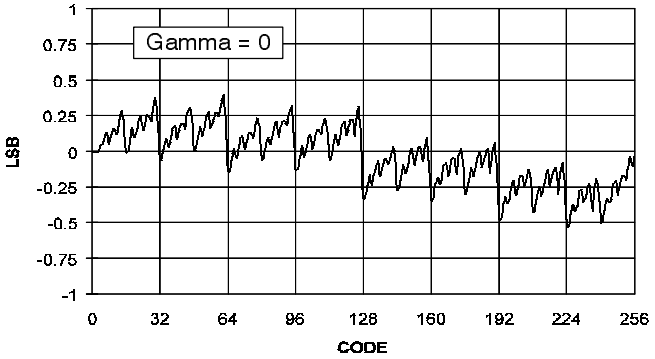


Figure 12. ADC INL Error Plot Channel A

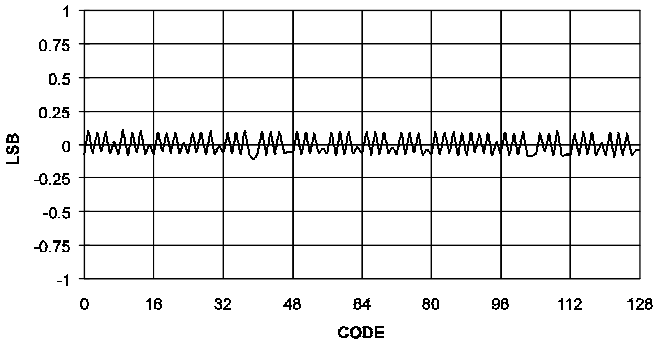


Figure 13. Gain DAC DNL Error Plot Channel A

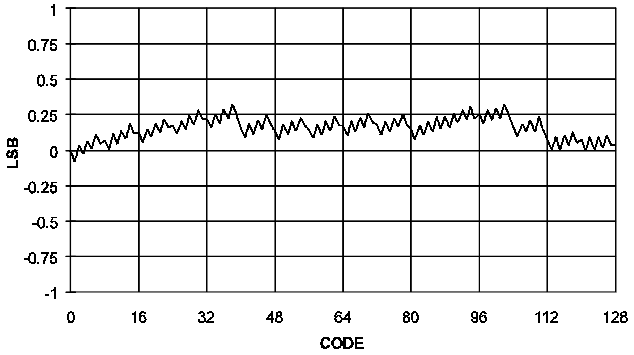


Figure 14. Gain DAC INL Error Plot Channel A

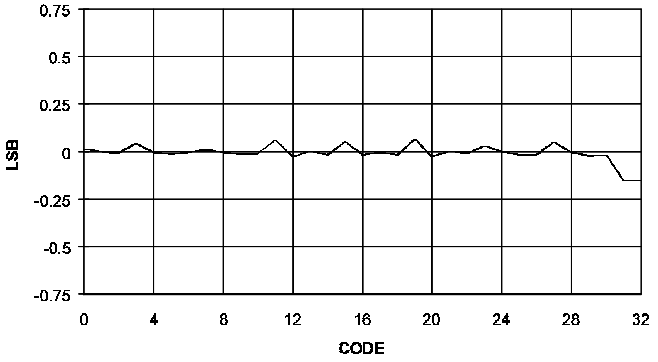


Figure 15. Offset DAC DNL Error Plot Channel A

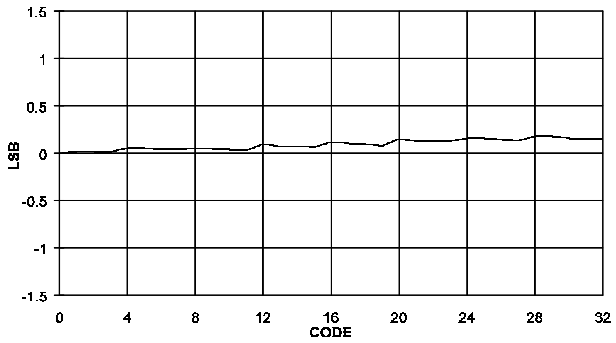


Figure 16. Offset DAC INL Error Plot Channel A

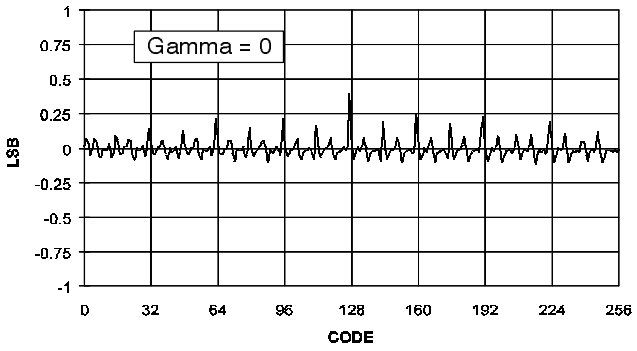


Figure 17. ADC DNL Error Plot
Channel B

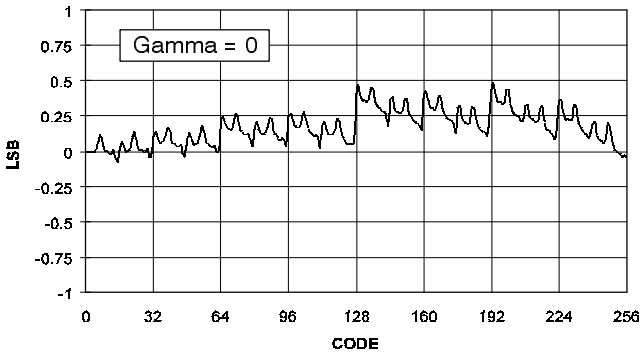


Figure 18. ADC INL Error Plot
Channel B

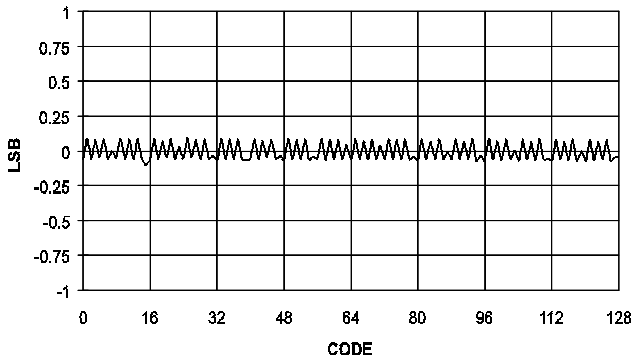


Figure 19. Gain DAC DNL Error Plot
Channel B

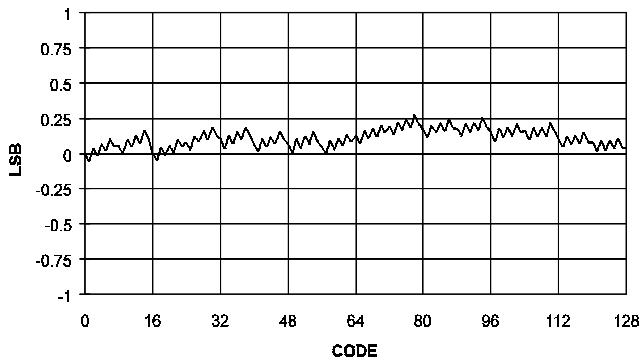


Figure 20. Gain DAC INL Error Plot
Channel B

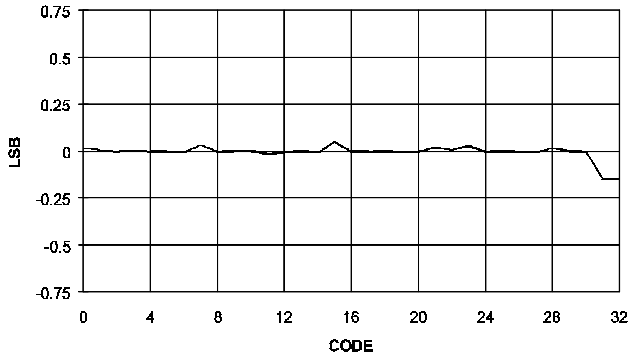


Figure 21. Offset DAC DNL Error Plot
Channel B

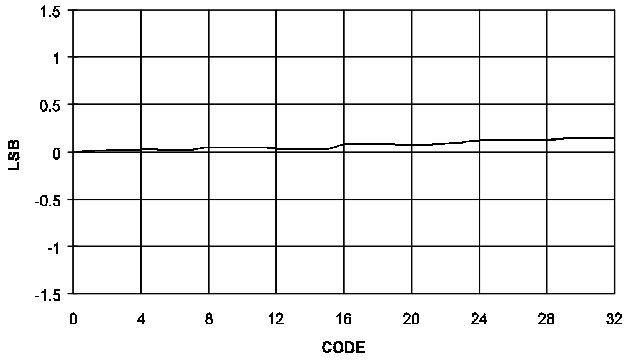


Figure 22. Offset DAC INL Error Plot
Channel B

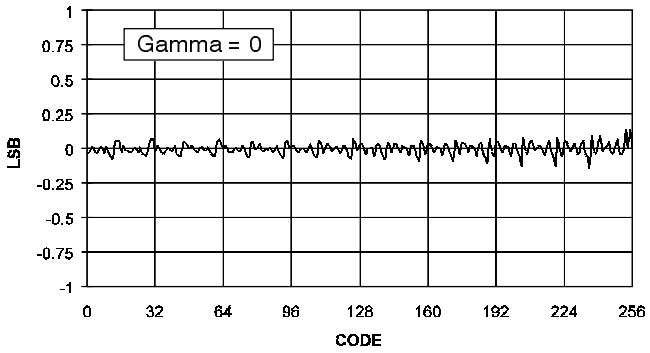


Figure 23. ADC DNL Error Plot Channel C

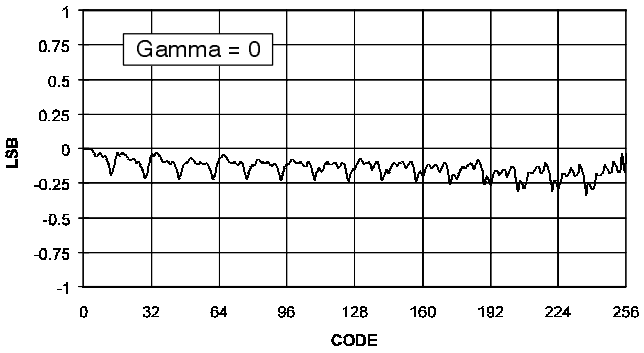


Figure 24. ADC INL Error Plot Channel C

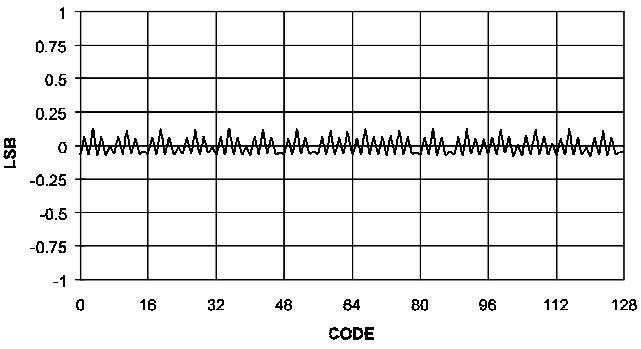


Figure 25. Graph 1. Gain DAC DNL Error Plot Channel C

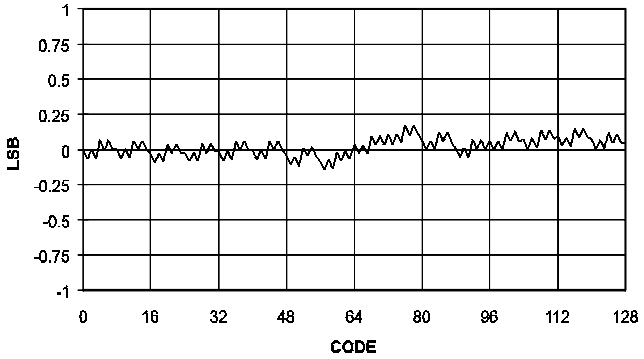


Figure 26. Gain DAC INL Error Plot Channel C

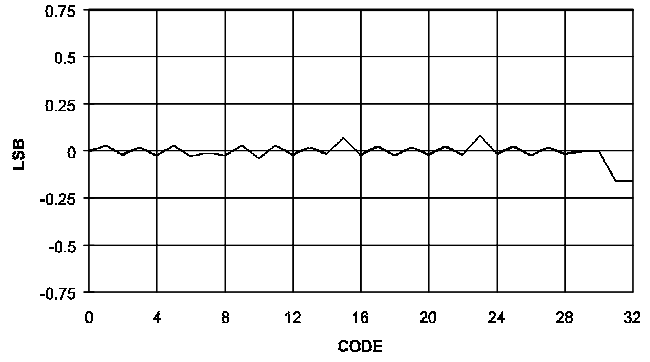


Figure 27. Offset DAC DNL Error Plot Channel C

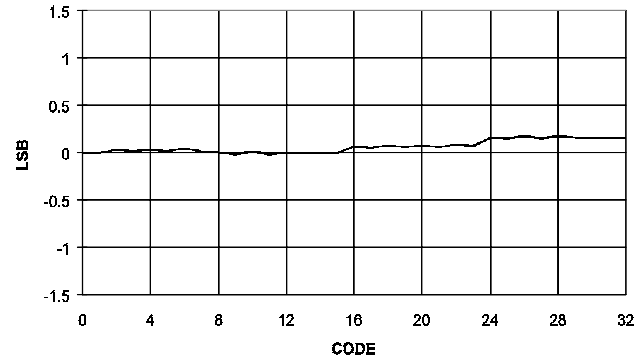


Figure 28. Offset DAC INL Error Plot Channel C