LAMBDA ADVANCED ANALOG INC.

ART2815T Series

Hybrid – High Reliability Radiation Hardened DC/DC Converter

DESCRIPTION

The ART2815T series of DC/DC converters are designed specifically for use in the hostile radiation environments characteristic of space and weapon systems. The ART's extremely high level of radiation tolerance is the culmination of extensive research, thorough analysis and testing, and careful component selection. Many of Advanced Analog's best circuit design features have been incorporated in the ART to create a new design capable of high levels of performance in a radiation intense environment.

The converters are packaged in a rugged, low profile package that meets all requirements of MIL-PRF-38534. Long term hermeticity is assured by parallel seam weld lid attachment and by the exclusive use of ceramic insulators on all package pins. These converters are manufactured in a facility fully qualified to MIL-PRF-38534 for Class H. All manufacturing processes have been qualified enabling Advanced Analog to deliver fully compliant devices.

FEATURES

- **Total Dose >100K rad(Si); 2:1 design margin.**
- **Derated to MIL-STD-975 and MIL-STD-1547.**
- **Compliant to MIL-PRF-38534 Class H with full Class K processing.**
- **19 to 50V DC input range.**
- **5V, ±12V, and ±15V outputs available.**
- **Short circuit protection.**
- **Input under voltage lockout.**
- **3 to 30 watts output power.**
- **12.8 W/In³ output power density.**
- **True hermetic package.**
- **High electrical efficiency.**
- **External shutdown port.**
- **External synchronization port.**
- **2,000,000 hour MTBF.**

CIRCUIT TOPOLOGY

The ART2815T converter has been implemented using a single ended forward conversion topology. Single ended topology is well suited to radiation hardened designs as it is not subject to the transformer saturation problems associated with some double ended topologies. Nominal conversion frequency is 250KHz. The design incorporates an input LC filter to attenuate input ripple current. When used in conjunction with an external filter, compliance to MIL-STD-461B CE03 is obtained (see EMI application note). An efficient low overhead linear bias regulator is used to provide a stable, well regulated bias for the converter primary control logic. Output control is realized using a wide band discrete Pulse Width Modulator control circuit (PWM), with a unique non linear ramp generator circuit. This stabilizes loop gain over line variations for superior output transient response. Output voltages are sensed using a patented magnetic feedback circuit. This magnetic feedback circuit is relatively insensitive to temperature variations, radiation, aging and manufacturing variations, making it particularly well suited to Rad Hard designs. Control logic uses only radiation tolerant components and all current paths are limited with series resistance to control photo currents. Other key design features include short circuit and undervoltage protection, along with an inhibit function and an external synchronization port.

RADIATION PERFORMANCE ASSURANCE

The radiation tolerance characteristics inherent in the ART2815T converter are the result of a carefully planned ground-up design program with specific radiation design goals. Following identification of a general circuit topology, the first task of this design was the selection of elements for which extensive TREE data already existed. This data was then utilized as input for PSPICE and RadSPICE analyses as well as subsequent worst case analyses, circuit optimization studies and end of life studies. Design margins utilized in component selection exceeded four or five times the post radiation requirement in order to assure performance goals on 100% of the finished converters–even without lot radiation testing of elemental wafer lots.

Radiation tests subsequently performed on finished devices as validation of the design have provided gratifying confirmation of these goals. All design goals have been met and exceeded in most cases. In summary the ART2815T radiation performance has been assured by a rigorous ground-up design incorporating the necessary hardness characteristics without having to resort to selective assurance of performance by test.

The Radiation Performance Specification table ensures that all device performance specifications are maintained following exposure to the listed tests.

Radiation Specification: Tcase = 25°± 5°C

Test	Conditions	Min	Typ	Max	Unit
Total Ionizing Dose 2:1 Margin	MIL-STD-883, Method 1019.4 Operating bias applied during exposure	100	500		KRads (Si)
Dose Rate (Gamma Dot) Temporary Saturation Survial	MIL-STD-883, Method 1021	 1E8 1E11			Rads (Si)/sec
Neutron Fluence	MIL-STD-883, Method 1017.2	3E12			Neutron /cm²
Single Event Effects - SEU, SEL	Heavy ions, (BNL Dual VanDeGraf Generator)	83			MeV• cm²/mg

SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS		RECOMMENDED OPERATING CONDITIONS	
Input voltage range	-0,5 Vdc to +80 Vdc	Input voltage range	+19 Vdc to +60 Vdc
Output power	Internally limited to 52 W typical	Derated input voltage range[1]	+19 Vdc to +50 Vdc
Lead temperature (soldering 10 seconds)	+300°C	Output power	3 W to 30 W
		Operating temperature (case)	-55°C to 125°C
Storage temperature (case)	-55°C to +135°C	Derated operating temperature (case)[1]	-55°C to 85°C

Note:
1. Stess derated per MIL-STD-975

Electrical Performance Characteristics

Parameter	Symbol	Condition		Limit MIN	Limit MAX	Units
OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 1.5 Adc, T_{CASE} = 25°C I_{OUT} = ±250 MAdc , T_{CASE} = 25°C	(main) (dual)	4.95 ±14.50	5.05 ±15.15	Vdc Vdc
OUTPUT POWER[3]	P_{OUT}	19 Vdc < V_{IN} < 50 Vdc		3	30	W
OUTPUT CURRENT[3]	I_{OUT}	19 Vdc < V_{IN} < 50 Vdc 19 Vdc < V_{IN} < 50 Vdc	(main) (dual)	150 75	3000 750	mAdc mAdc
LINE REGULATION[1]	VR_{LINE}	150 mAdc < I_{OUT} < 3000 mAdc 19 Vdc < V_{IN} < 50 Vdc ±75 mAdc < I_{OUT} < 750 mAdc	(main) (dual)	-15 -15	+15 +15	mV mV mV
LOAD REGULATION[2]	V_{LOAD}	150 mAdc < I_{OUT} < 3000 mAdc 19 Vdc < V_{IN} < 50 Vdc ±75 mAdc < I_{OUT} < 750 mAdc	(main) (dual)	-180 -300	+180 +300	mV mV mV
CROSS REGULATION[6]	VR_{CROSS}	19 Vdc < V_{IN} < 50 Vdc 19 Vdc < V_{IN} < 50 Vdc	(main) (dual)	-10 -500	+10 +500	mV mV
TOTAL REGULATION[2]	VR	All conditions of Line, Load Cross Regulation, Aging, Temperature and Radiation	(main) (dual)	4.8 14.0	5.2 14.0	V V V
INPUT CURRENT	I_{IN}	I_{OUT} = minimum rated, Pin 3 open Pin 3 shorted to Pin 2 (disabled)	(main) (dual)		250 8	mA mA
OUTPUT RIPPLE VOLTAGE[4]	V_{RIP}	19 Vdc < V_{IN} < 50 Vdc I_{OUT} = 3000 mAdc (main), ±500 mAdc	(dual)		100	mV_{p-p} mV_{p-p}
INPUT RIPPLE CURRENT[4]	I_{RIP}	19 Vdc < V_{IN} < 50 Vdc I_{OUT} = 3000 mAdc (main), ±500 mAdc	(dual)		150	mA_{p-p} mA_{p-p}
SWITCHING FREQUENCY	Fs	Synchronization input open (pin 6)		225	275	kHz
EFFICIENCY	EFF	I_{OUT} = 3000 mAdc (main), ±500 mAdc		80		%
ENABLE INPUT[1] open circuit voltage drive current (sink) voltage range				 3.0 -0.5	 5.0 100 50	 V µA V
SYNCHRONIZATION INPUT[1] frequency range pulse high level pulse low level pulse rise time pulse duty cycle		External clock signal on Synch. input (pin 4)		 225 4.5 -0.5 40 20	 310 10.0 0.25 80	 kHz V V V/µA %
POWER DISSIPATION, LOAD FAULT	PD	Short circuit, any output			7,5	W
OUTPUT RESPONSE TO STEP LOAD CHANGES[5,9]	V_{TLD}	10% Load to/from 50% load 50% Load to/from 100% load		-200 -200	200 200	mV_{PK} mV_{PK}
RECOVERY TIME FROM STEP LOAD CHANGES[3]	T_{TLD}	10% Load to/from 50% load 50% Load to/from 100% load			200 200	µS µS
OUTPUT RESPONSE TO STEP LINE CHANGES[8,9]	V_{TLN}	I_{OUT} = 3000 mAdc V_{IN} = 19 V to/from 50V I_{OUT} = ±500 mAdc	(main) (dual)	-350 -1050	+350 +1050	mV_{PK} mV_{PK} mV_{PK}
RECOVERY TIME FROM STEP LINE CHANGES[8,9,11]	T_{TLN}	I_{OUT} = 3000 mAdc V_{IN} = 19 V to/from 50V I_{OUT} = ±500 mAdc	(main) (dual)		500 500	µS µS µS

SPECIFICATIONS (Continued)

Electrical Performance Characteristics

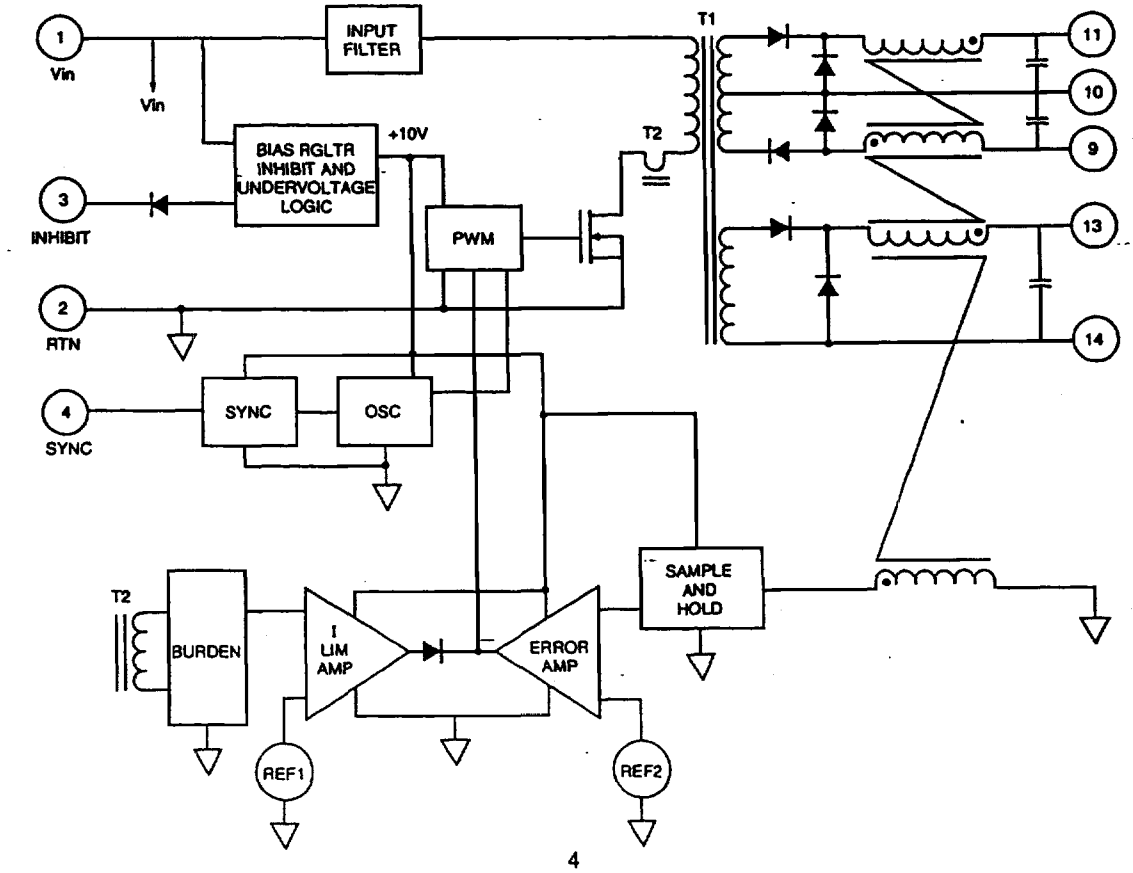
Parameter	Symbol	Condition		Limit MIN	Limit MAX	Units
TURN ON OVERSHOOT	Vos	I_{OUT} = minimum and full rated	(main) (dual)		500 1500	mV mV
TURN ON DELAY[12]	T_{DLY}	I_{OUT} = minimum and full rated		5	20	mS
CAPACITIVE LOAD[7,8]	CL	No effect on DC performance	(main) (dual)		500 100	µF µF
ISOLATION	ISO	500 VDC Input to Output or any pin to case (except) pin 12		100		MΩ

Notes:

1. Parameter measured from 28V to 19V or to 50V while loads remain fixed.
2. Parameter measured from nominal to minimum or maximum load conditions while line remains fixed.
3. Up to 750 mA is available from the dual outputs provided the total output power does not exceed 30 W.
4. Guaranteed for a bandwidth of DC to 20 Mhz. Tested using a 20Khz to 2 Mhz bandwidth.
5. Load current is stepped for output under test while other outputs are fixed at half rated load.
6. Load current is fixed for output under test while other output loads are varied for any combination of minimum to maximum.
7. A capacitive load of any value from 0 to the specified maximum is permitted without compromise to DC performance. A capacitive load in excess of the maximum limit may interfere with the proper operation of the converter's short circuit protection, causing erratic behavior during turn on.
8. Parameter is tested as part of design characterization or after design or process changes. Thereafter, parameters shall be guaranteed to the limits specified in the table.
9. Load transient rate of change, dv/dt ≤ 2 A/µSec.
10. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of its steady state value.
11. Line transient rate of change, di/dt ≤ 50 V/µSec.
12. Turn on delay time is for either a step application of input power or a logical low to high transition on the inhibit pin (pin 3) while power is present at the input.

- Stresses above the absolute maximum ratings may cause permanent damage to the device. Extended operation at the absolute maximum ratings may degrade performance and affect reliability.
- Device performance outside the recommended operating conditions not specified.

BLOCK DIAGRAM



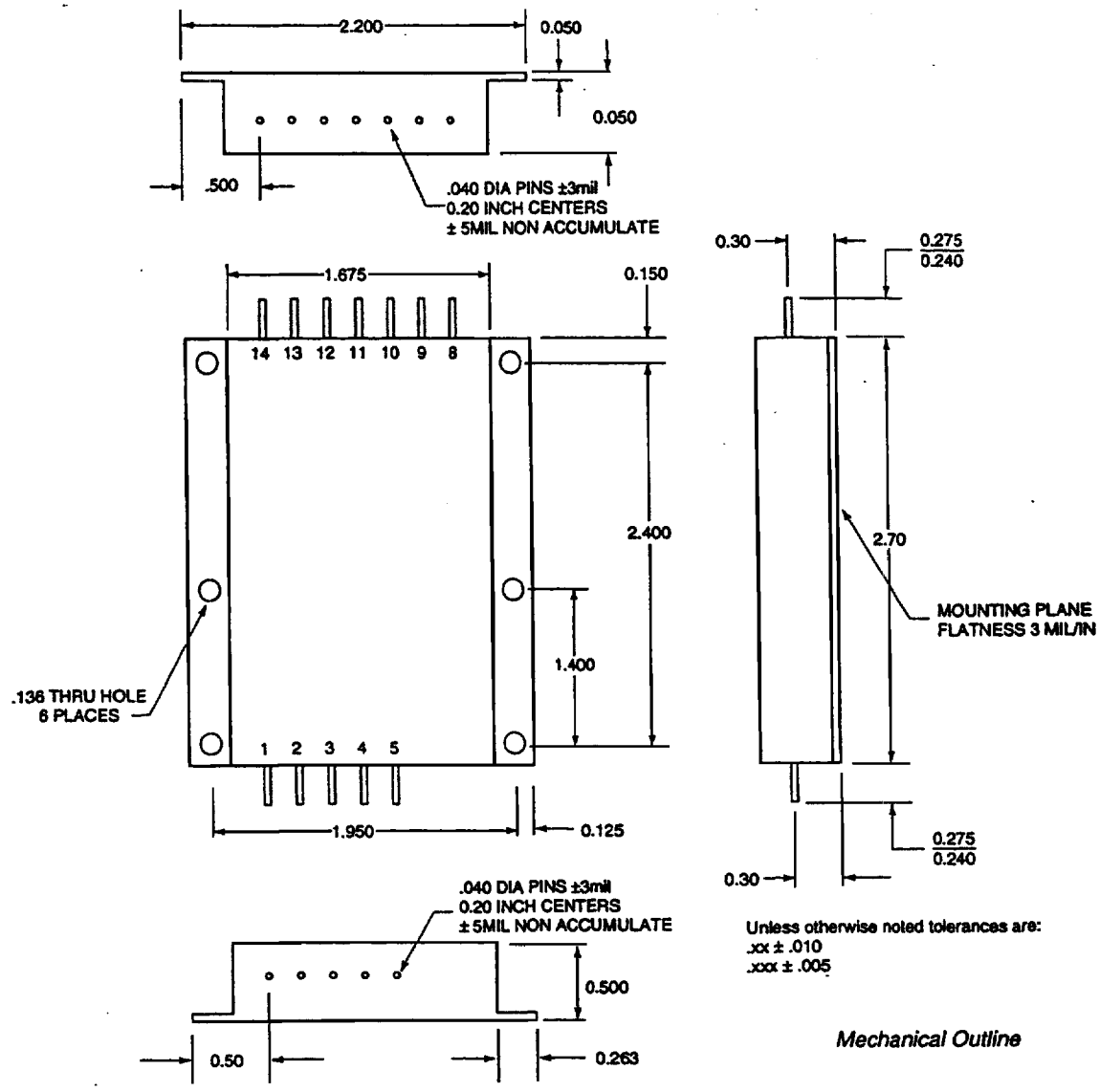
SPECIFICATIONS

Group A Electrical Tests

Parameter	Symbol	Condition		Group A subgroups	Limit MIN	Limit MAX	Units
OUTPUT VOLTAGE ACCURACY	V_{OUT}	I_{OUT} = 1.5 Adc, T_{CASE} = 25°C I_{OUT} = ±250 MAdc, T_{CASE} = 25°C	(main) (dual)	1,2,3 1,2,3	4.95 ±14.50	5.05 ±15.15	V V
OUTPUT POWER[1]	P_{OUT}	V_{IN} =19V, 28V, 50V		1,2,3	3	30	W
OUTPUT CURRENT[1]	I_{OUT}	V_{IN} =19V, 28V, 50V V_{IN} =19V, 28V, 50V	(main) (dual)	1,2,3 1,2,3	150 75	3000 750	mAdc mAdc
OUPTUT REGULATION[4]	VR	I_{OUT} = 150, 1500, 3000mAdc V_{IN} =19V, 28V, 50V I_{OUT} = ±75, ±250, ±500mAdc	(main) (dual)	1,2,3 1,2,3	4.8 14.0	5.2 15.8	V V
INPUT CURRENT	I_{IN}	I_{OUT} = minimum rated, Pin 3 open Pin 3 shorted to Pin 2 (disabled)	(main) (dual)	1,2,3 1,2,3		250 8	mA mA
OUTPUT RIPPLE[2]	V_{RIP}	V_{IN} =19V, 28V, 50V I_{OUT} = 3000mAdc main, ±500mA dual		1,2,3		100	mV_{p-p}
INPUT RIPPLE[2]	I_{RIP}	V_{IN} =19V, 28V, 50V I_{OUT} = 3000mAdc main, ±500mA dual		1,2,3		150	mV_{p-p}
SWITCHING FREQUENCY	Fs	Synchronization input open (pin 6)		4,5,6	225	275	kHz
EFFICIENCY	EFF	I_{OUT} = 800 mA main, ±500 mA dual		1 2,3	80 78		% %
POWER DISSIPATION LOAD FAULT	PD	Short circuit, any output		1,2,3		7.5	W
OUTPUT RESPONSE TO STEP LOAD CHANGES [3,5]	V_{TLD}	10% Load to/from 50% load 50% Load to/from 100% load		4,5,6 4,5,6	-200 -200	200 200	mV_{PK} mV_{PK}
RECOVERY TIME FROM STEP LINE CHANGES[5,6]	T_{TL}	10% Load to/from 50% load 50% Load to/from 100% load		4,5,6 4,5,6		200 200	µS µS
TURN ON OVERSHOOT	Vos	I_{OUT} = minimum and full rated	(main) (dual)	4,5,6 4,5,6		500 1500	mV mV
TURN ON DELAY[7]	T_{DLY}	I_{OUT} = minimum and full rated		4,5,6	5	20	mS
ISOLATION	ISO	500 Vdc input to output or any pin to case (except pin 12)		1		100	mΩ

Notes:
1. Parameter verified during dynamic load regulation tests.
2. Guaranteed for DC to 20 Mhz bandwidth. Tested conducted using a 20Khz to 2 Mhz bandwidth.
3. Load current is stepped for output under test while other outputs are fixed at half rated load.
4. Each output is measured for all combinations of line and load. Only the minimum and maximum readings for each output are recorded.
5. Load step transition time ≥ 10µS.
6. Recovery time is measured from the initiation of the transient to where V_{OUT} has returned to within ±1% of its steady state value.
7. Turn on delay time is for either a step application of input power or a logical low to high transition on the inhibit pin (pin 3) while power is present at the input.

MECHANICAL DIAGRAM

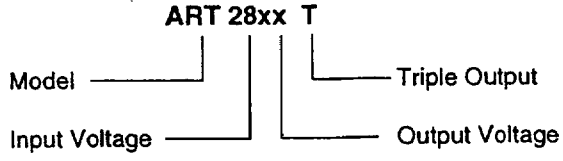


Mechanical Outline

PIN DESIGNATION

Pin 1	+V Input	Pin 9	- Dual Output
Pin 2	Input Return	Pin 10	Dual Return
Pin 3	Enable	Pin 11	+ Dual Output
Pin 4	Sync	Pin 12	Chassis
Pin 5	N/C	Pin 13	+5 Volt Output
Pin 8	No connection	Pin 14	5 V Return

PART NUMBER

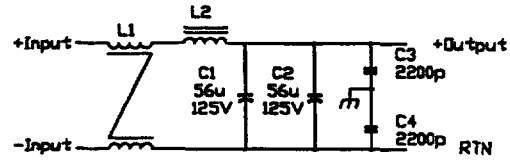


APPLICATION INFORMATION

Inhibit Function

Connecting the enable input (Pin 3) to input common (Pin 2) will shut down the converter. Typically, this can be accomplished by driving the enable pin with an open collector device capable of sinking at least 100µA. The pin may also be driven with TTL. A TTL low level will inhibit all outputs. Open circuit voltage of the inhibit pin is 4V±1V. An internal pull-up resistor is provided. Pin 3 may be left floating if the inhibit function is not used. An internal series blocking diode protects against excessive voltages to 50V. Reverse voltages to -.5v can be tolerated.

External EMI Filter



L1-7 Turns AWG#20 Bifilar on Mag Inc P/N YJ-41305 or equivalent
L2-30 Turns AWG#20 on Mag Inc P/N MPP55048 or equivalent
C1, C2 - 56uf, 125 Volts M39006/22-0880 or equivalent
C3, C4 - 2200pf, CKR Type or equivalent

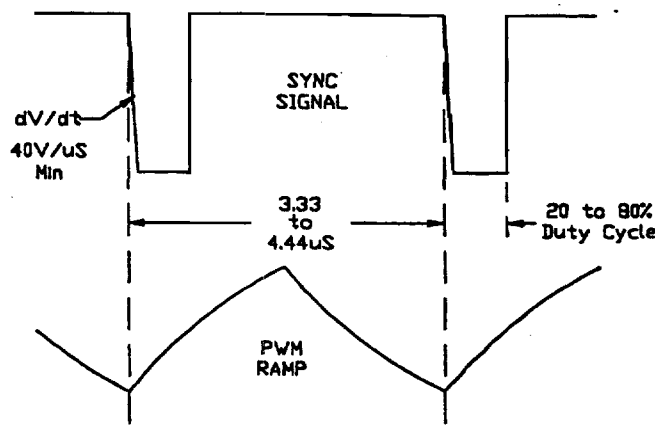
All ART series converters use a single stage "LC" input filter to attenuate input ripple current. An optional external EMI filter can be used to further attenuate ripple current to below the limits imposed by MIL-STD-461B CE03. (See figures M and N for converter conducted emissions)

Device Synchronization

When multiple switching converters are used to implement a single power conditioning system, low frequency oscillations (beat frequency noise) may arise due to slight differences in the switching frequencies of the converters.

Beat frequency noise may interfere with the proper operation of sensitive systems, such as communications, radar or telemetry. For this reason, it is recommended that switching in multiple converter systems be synchronous.

By driving the Sync Input (pin 4) with an external pulse generator, converter switching frequency can be synchronized to an external pulse generator frequency. Driving the sync pins of all converters in a multiple converter system with a single pulse generator will synchronize all converters to the pulse generator frequency.



Oscillator Synchronization to Higher External Frequency

The synchronization circuit is edge triggered. A negative going transition initiates Pulse Width Modulator (PWM) ramp generator synchronization. To ensure reliable synchronization, the pulse generator should possess the following characteristics:

1) The generator source impedance shall be less than 1000 ohm per converter being synchronized. For example, if two converter synchronization pins are driven, the source impedance must be less than 500 ohms.
2) Pulse amplitude shall be a minimum of 4.25V referenced to pin 2 (Input RTN) of the converter and a maximum of 10V. dV/dt of the falling edge of the pulse shall be at least 40V/µS.
3) The pulse waveform shall be a negative going pulse–with a duty cycle greater than 20% but less than 80%.
4) The pulse period shall be between 3.33, and 4.44µS. This forces the conversion frequency of the synchronized converters to between 225 and 300KHz.

It should be noted that the synchronization circuit is relatively fail-safe. In the event that the external pulse generator ceases switching the converters will continue to free run at their own internally set switching frequency.

Circuit layout must be such that the Pulse generator output is connected to the Sync Input (pin 4) of each converter in order to be synchronized. The Pulse Generator ground shall be referenced to Input Return (pin 2). It is important to keep run lengths short, minimize current loops and maintain good signal flow. Good mechanical design practices will minimize the possibility of radiating the sync frequency.

Input Under Voltage Protection

Units are protected from damage which might be caused by operation at excessively low input line voltages. The control logic bias regulator contains circuitry to monitor line voltage and hold the bias low until there is sufficient line voltage to guarantee proper converter operation. The Under Voltage Lockout is factory set to trigger at 16.8 volts line (nominal), and units are guaranteed to operate at 19 volts line and above for all conditions of load and temperature within the specified limits.

Output Short Circuit Protection

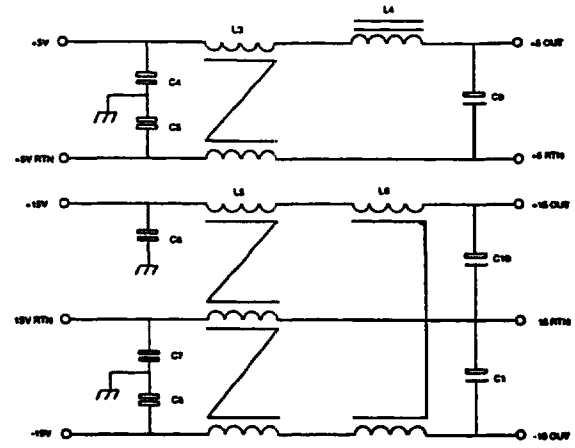
Units are protected from output short circuits using a hiccup mode current limit circuit. Primary switching currents are sensed, and if an overcurrent is detected, switching action is terminated. After a delay, switching resumes. If the short circuit condition has not been cleared, switching will again be terminated. The duty cycle of these on/off cycles is low. Therefore, output power folds back drastically ensuring minimal stress in all components. The current limit trip point is factory set for 170% of full load, nominally (roughly 50 watts out) at 28 volts line. Hiccup duty cycle is approximately 5%.

Parallel Operation

No provisions for forced current sharing have been made in the ART2815T control circuitry. However, units may be paralleled to accommodate higher output power requirements. The main 5 volt outputs will share to within approximately 10% of full load typically, and dual outputs will share to within 50% of full load typically. Load sharing is a function of the output impedances of the individual converters, and the converter with the highest nominal set voltages will be predominant.

External Output Filtering

The ART2815T is provided with internal output filtering. This filtering is sufficient for all but the most critical applications. However, when extremely low noise outputs are required, some additional external filtering will be required. The output filter shown below has been characterized with the ART2815T and component values are given for convenience. Typical performance is shown in figures S & T. It is important to note, that when filtering high frequency noise, parasitic components can dominate the filter performance. Care should be taken during circuit layout. Run and wire lengths should be minimized, high frequency current loops should be minimized, and attention should be paid to the construction details of magnetic circuit elements. Tight magnetic coupling will improve overall filter performance and reduce stray magnetic fields.



L3–7 TURNS AWG#21 BIFLAR ON MAG. INC. CORE P/N YJ-41305-TC OR EQUIVALENT
L4–4 TURNS AWG#21 ON MAG. INC CORE P/N MPP55048 OR EQUIVALENT
L5–7 TURNS AWG#24 TRIFILAR ON MAG. INC. CORE P/N YJ-41305-TC OR EQUIVALENT
L6–5 TURNS AWG#21 BIFILAR ON MAG. INC. CORE P/N MPP55048
C4 THROUGH C8 2200pF CKR TYPE CERAMIC CAPACITORS
C9 170µF 15V M39006/22-0514 TANTALUM
C10, C1 25µF 50V M39006/22-0568 TANTALUM

The measurement of high frequency noise is also critical. The noise should be measured as close to the filter output as is possible. The voltage probe ground lead should be minimum length. Measurement bandwidth will also effect the end results. Output ripple measurements shown herein were made using a 20MHz bandwidth.

TYPICAL CHARACTERISTICS

Waveforms shown are for ART2815T

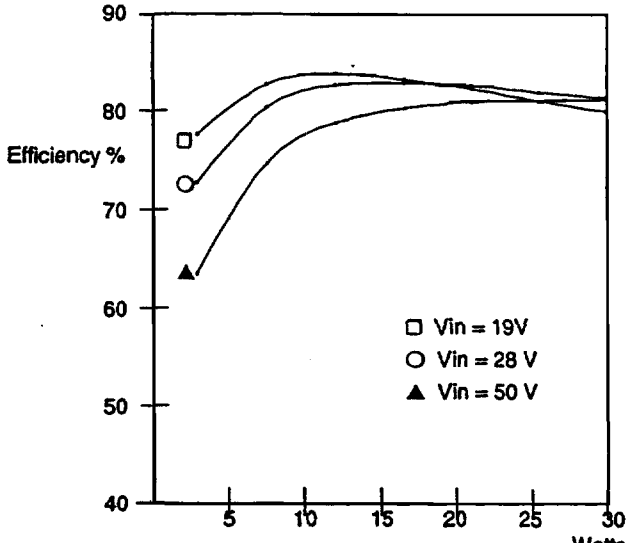


Figure B **Efficiency Vs Line & Load**

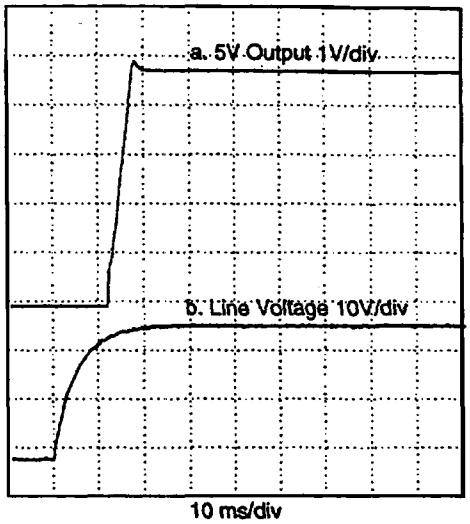


Figure C **Turn-on Response**
5V Output Full Load

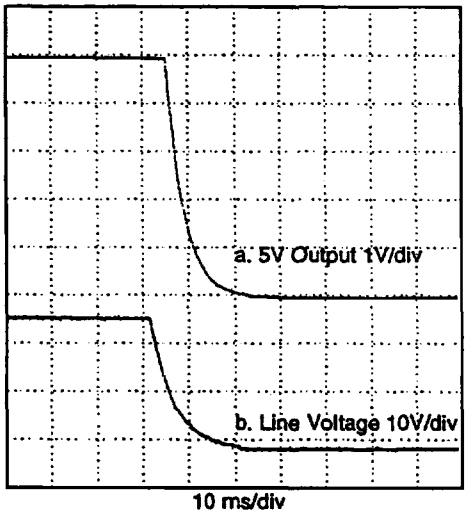


Figure D **Turn-off Response**
5V Output Min Load

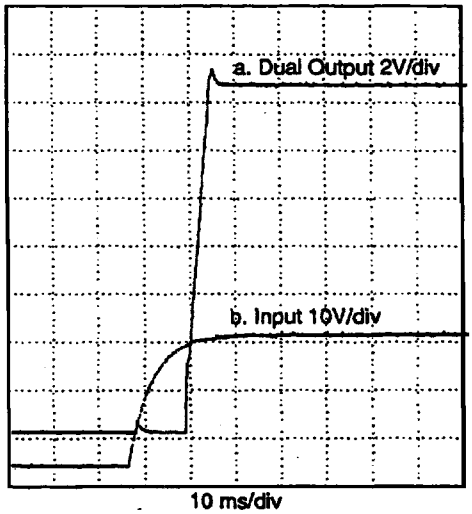


Figure E **Turn-on Response**
Dual Output Full Load

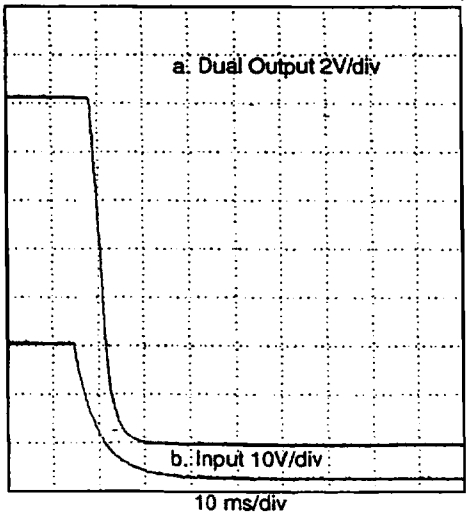


Figure F **Turn-off Response**
Dual Ouput Min Load

TYPICAL CHARACTERISTICS (Continued)

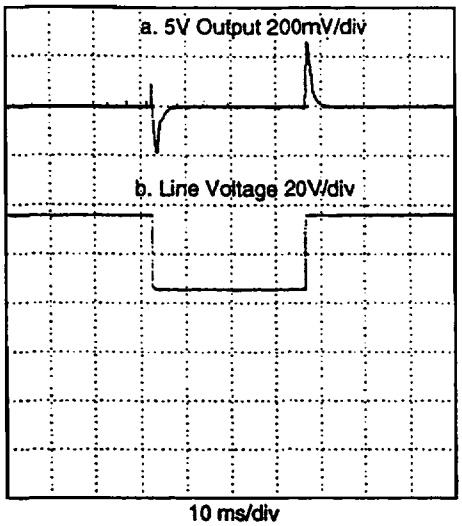


Figure G **Line Transient Response**
5V Output
Input Stepped 19–50–19V

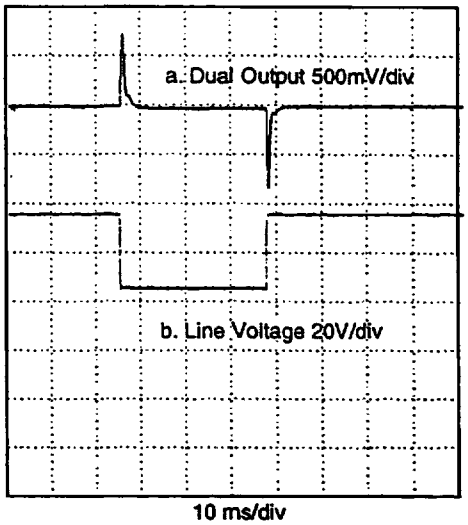


Figure H **Line Transient Response**
15V Output
Input Stepped 19–50–19V

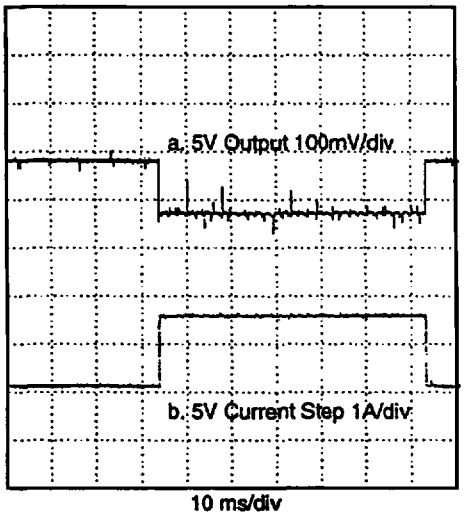


Figure I **Load Step Response**
5V Output Stepped
50–100–50% Load

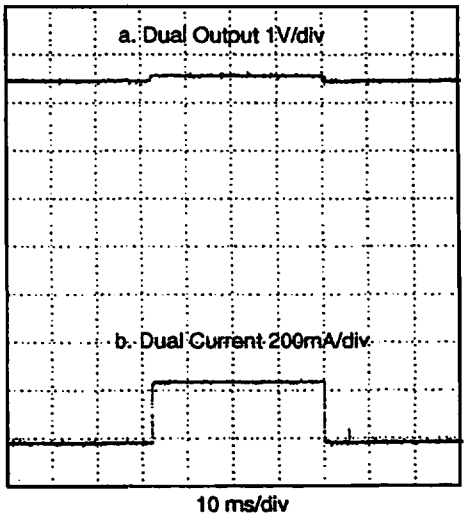


Figure J **Load Step Response**
Dual Outputt Stepped
50–100–50% Load

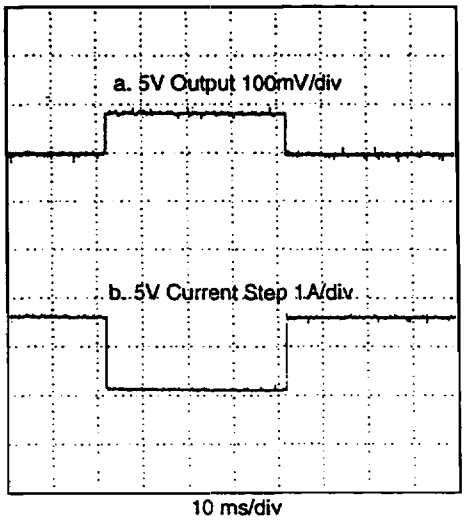


Figure K **Load Step Response**
5V Output Stepped
10–50–10% Load

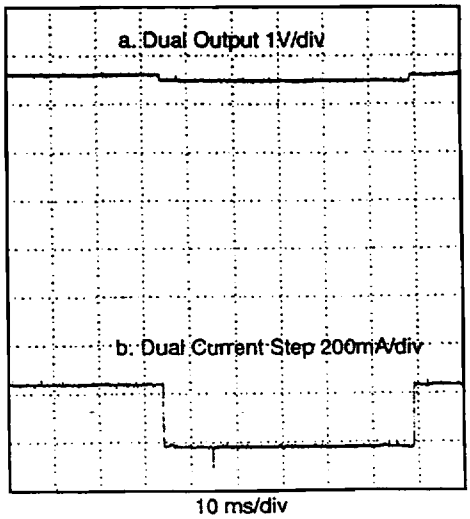


Figure L **Load Step Response**
Dual Output Sttepped
10–50–10% Load

TYPICAL CHARACTERISTICS (Continued)

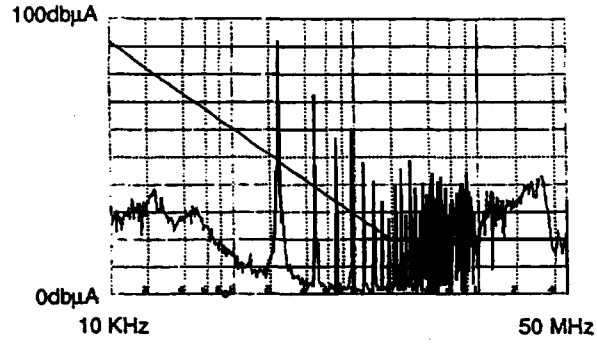


Figure M **Conducted Emissions**
Internal "LC" Filter

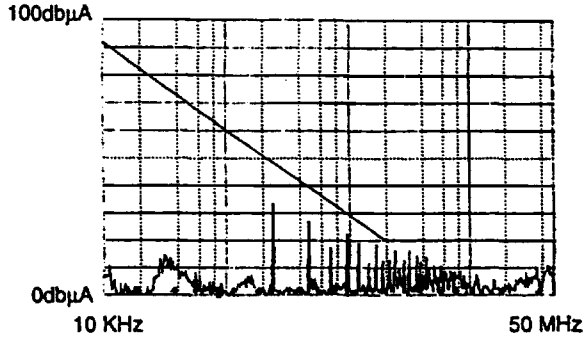


Figure N **Conducted Emissions**
External EMI Filter

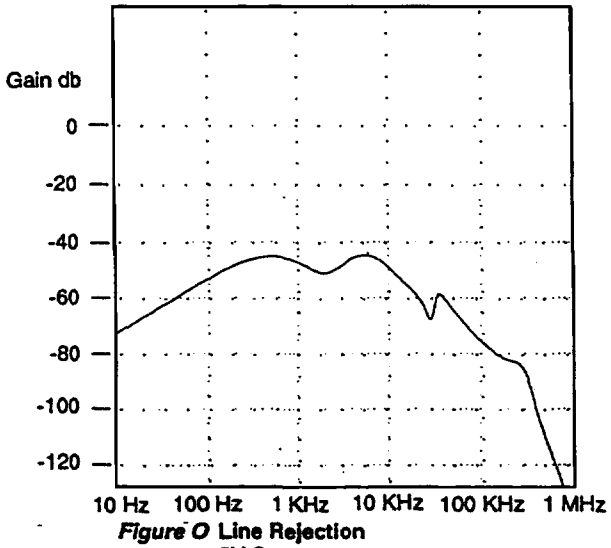


Figure O **Line Rejection**
5V Output

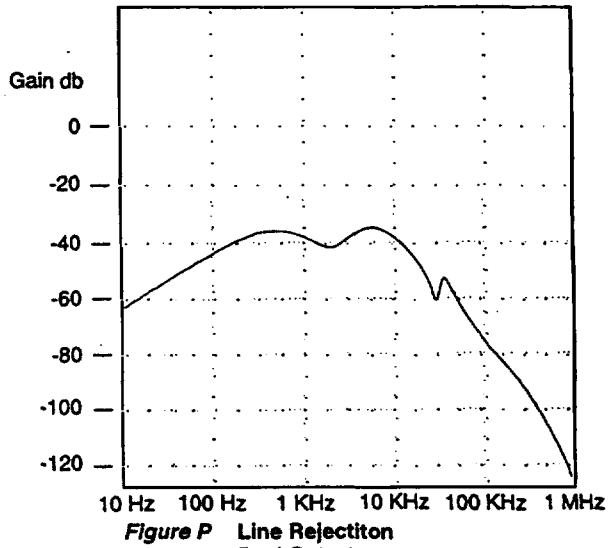


Figure P **Line Rejectiton**
Dual Outputs

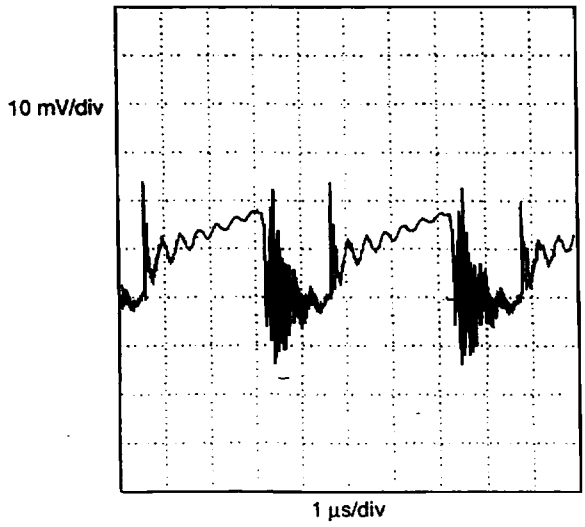


Figure Q **Output Ripple**
5V Output

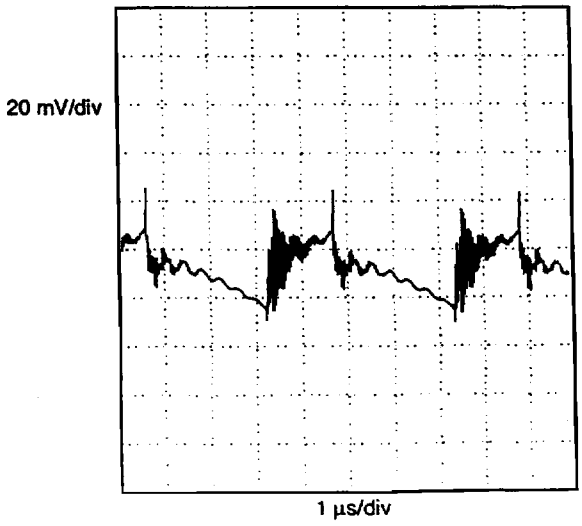


Figure R **Output Ripple**
Dual Output

TYPICAL CHARACTERISTICS (continued)

Waveforms shown are for ART2815T

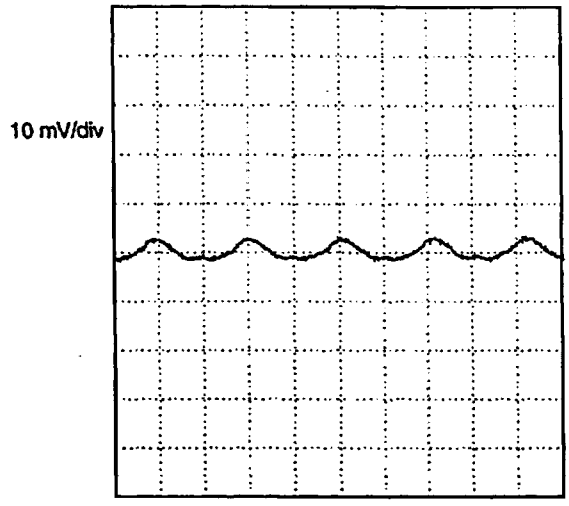


Figure S **5V Output with External Filter**

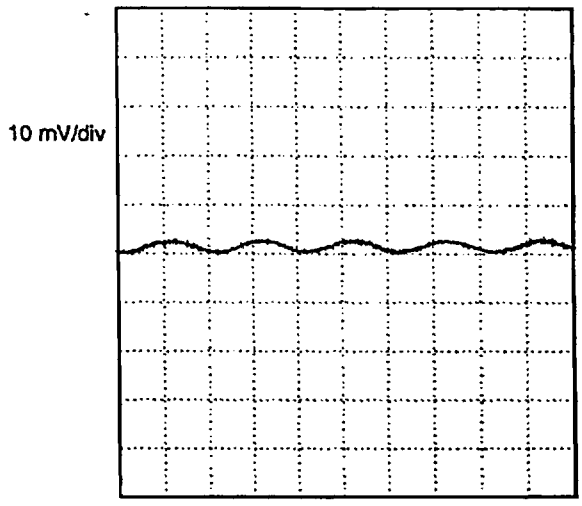


Figure T **Dual Output with External Filter**

LAMBDA ADVANCED ANALOG INC.

MIL-STD-1772
Qualified

2270 Martin Avenue
Santa Clara CA 95050-2781
(408) 988-4930 FAX (408) 988-2702