MICRO NETWORKS

ADS7800

3μsec, 12-Bit
SAMPLING A/D CONVERTER

FEATURES

- 333kHz Over Temperature
- ±5V and ±10V Input Ranges
- AC and DC Performance Completely Specified
- Internal Sample/Hold, Clock, Reference, 3-State Buffer
- 215mW Power Dissipation
- No-Missing-Codes Over Temperature
- 8-Bit or 12-Bit Output Format
- Package Options
  - Plastic DIP
  - Hermetic DIP
  - SOIC

DESCRIPTION

The ADS7800 is a complete, low-cost, 12-bit successive-approximation A/D converter with an internal sample/hold function. The ADS7800 uses an innovative, capacitor-array internal D/A converter, based on CMOS technology. The use of a CMOS architecture results in extremely low power consumption. Total acquisition and conversion time of 3μsec results in a 333kHz sampling rate, over the entire operating temperature range. AC and DC performance are completely specified.

The ADS7800 is complete with internal clock, reference, control logic, and 3-state output buffer. The interface logic provides for easy handshaking with most popular 8- and 16-bit microprocessors. The ADS7800's 3-state output buffer connects directly to the μP's data bus, and is readable as either one 12-bit word or two 8-bit bytes. Chip select, high-byte enable, and read/write (read/convert) control inputs enable the ADS7800 to connect directly to a system address bus and control lines, and to operate totally under processor control.

Internal scaling resistors allow a pin-selectable choice of two input ranges: ±5V and ±10V. The ADS7800 is available for operation over the commercial (0°C to +70°C) and industrial (−40°C to +85°C) temperature ranges. Package options include 24-pin single (0.300″) plastic or hermetic ceramic DIPs, and 24-pin plastic SOIC. The ADS7800 operates from a +5V supply and either a −12V or −15V supply.

Model Number	Package	Temperature Range	Linearity Error Max (T_{min} to T_{max})	SINAD* (dB Min.)
ADS7800JP	Plastic DIP	0°C to +70°C	±1	67
ADS7800KP	Plastic DIP	0°C to +70°C	±½	69
ADS7800JU	Plastic SOIC	0°C to +70°C	±1	67
ADS7800KU	Plastic SOIC	0°C to +70°C	±½	69
ADS7800AH	Ceramic DIP	−40°C to +85°C	±1	67
ADS7800BH	Ceramic DIP	−40°C to +85°C	±½	69

*Signal-to-(Noise+Distortion) Ratio.

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

ADS7800 12-Bit SAMPLING A/D CONVERTER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range:	
J, K Grades	0°C to +70°C
A, B Grades	−40°C to +85°C
Storage Temperature Range:	−65°C to +150°C
$+V_S$ to Digital Ground	+7V
$-V_S$ to Analog Ground	−16.5V
$+V_{SA}$ to $+V_{SD}$	±0.3V
Analog Ground to Digital Ground	±1V
Control Inputs to Digital Ground	−0.3V to V_S +0.3V
Analog Input to Voltage	±20V
Junction Temperature	+160°C
Lead Temperature (Soldering, 10 sec)	+300°C
Power Dissipation	750mW
Thermal Resistance Θ_{JA}:	
Plastic DIP	100°C/W
SOIC	100°C/W
Ceramic DIP	50°C/W

ORDERING INFORMATION

PART NUMBER ——— **ADS7800 J P**

Select suffix J, K, A or B for desired performance and specific temperature range.

Select suffix P, U or H for desired package option.

DESIGN SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $V_S = +5V$, $V_S = -15V$, $f_S = 333kHz$, unless otherwise indicated)

ANALOG INPUTS	MIN.	TYP.	MAX.	UNITS
Input Voltage Range		±10 and ±5		Volts
Input Impedance: ±10V	4.4	6.3	8.1	kΩ
±5V	2.9	4.2	5.4	kΩ
DIGITAL INPUTS CS, R/C, HBE				
Logic Levels: Logic "1"	+2.4		+5.3	Volts
Logic "0"	−0.3		+0.8	Volts
Loading: Logic "1"			+5	μA
Logic "0"			−5	μA
DIGITAL OUTPUTS DB0 to DB11, BUSY				
Output Format		12-Bit Parallel or 8-Bit/4-Bit		
Output Coding		Offset Binary		
Logic Levels: Logic "1" (I_{SOURCE} = 500μA)	+2.4		+5.0	Volts
Logic "0" (I_{SINK} = 1.6mA)	0		+0.4	Volts
Leakage (High-Impedance State)		±0.1	±5	μA
INTERNAL REFERENCE				
Reference Output Voltage (Pin 3)	1.9	2.0	2.1	Volts
Available Output Source Current		10		μA
POWER SUPPLY REQUIREMENTS				
Power Supply Range: $-V_S$ Supply	−11.4	−15	−16.5	Volts
Power Supply Range: $+V_S$ Supply	+4.75	+5.0	+5.25	Volts
Current Drains: $-I_S$		3.5	6	mA
$+I_S$ (Total)		18	25	mA
Power Dissipation		135	215	mW
DYNAMIC CHARACTERISTICS				
Aperture Delay		13		nsec
Aperture Uncertainty (Jitter)		150		psec, rms
Transient Response, Full-Scale Step (Note 1)		130		nsec
Overvoltage Recovery, 2 X FS (Note 2)		150		nsec
CONVERSION TIME				
Conversion Only		2.5	2.7	μsec
Conversion + Acquisition		2.6	3.0	μsec
Throughput Rate	333	380		kHz

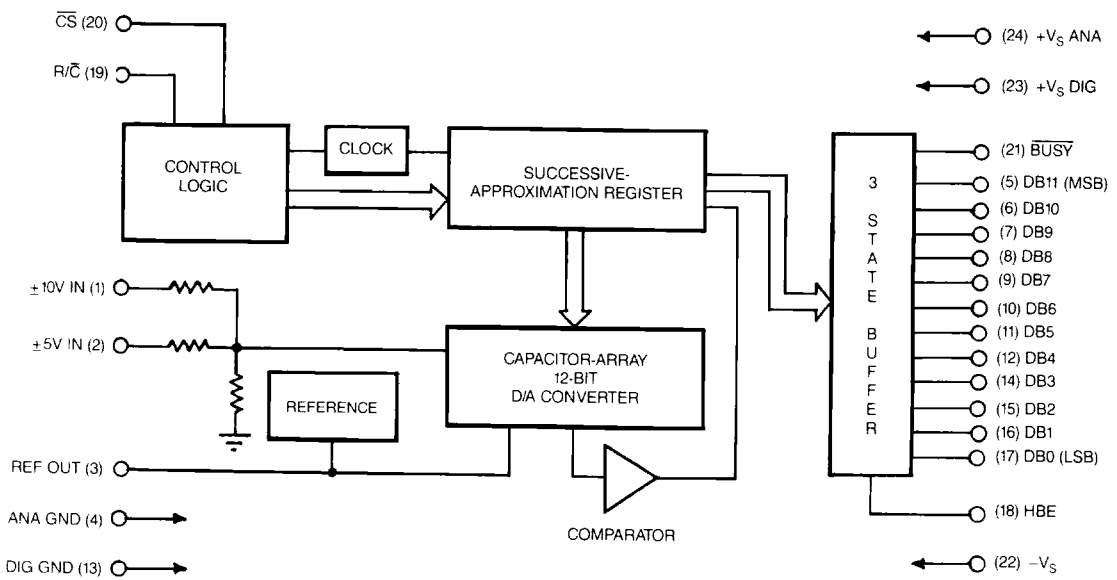
SPECIFICATION NOTES:

1. For 12-bit accuracy in specified time.
2. To specified performance in specified time.
3. Adjustable to zero with external trimpot.
4. Least Significant Bit. 1LSB=2.44mV for the ±5V range; 4.88mV for the ±10V range.
5. Characterized over T_{MIN} to T_{MAX} at +FS, 0V, and −FS. 0.1LSB is typical rms noise with worst-case conditions: +FS at +125°C.
6. All dB figures refer to ±10V or ±5V full-scale input.

CAUTION: These Devices are sensitive to electrostatic discharge. Proper anit-ESD IC handling procedures should be followed.

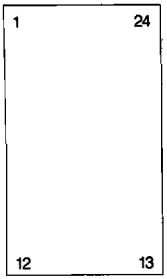
PERFORMANCE SPECIFICATIONS ($T_A = T_{MIN}$ to T_{MAX}, $+V_S = +5V$, $-V_S = -15V$, $f_S = 333kHz$, unless otherwise indicated)

MODEL	ADS7800JP/JU/AH			ADS7800KP/KU/BH			
TRANSFER CHARACTERISTICS	**MIN.**	**TYP.**	**MAX.**	**MIN.**	**TYP.**	**MAX.**	**UNITS**
RESOLUTION			12			12	Bits
TRANSFER CHARACTERISTICS							
Full-Scale Error			±0.50			±0.35	%
Full-Scale Error Drift		6			6		ppm/°C
Integral Nonlinearity			±1			±½	LSB(Note 4)
Differential Nonlinearity			±1			±¾	LSB
Resolution for No Missing Codes	12			12			Bits
Bipolar Zero Error (Note 3)			±4			±2	LSB
Bipolar Zero Error Drift		1			1		ppm/°C
Transition Noise (Note 5)		0.1			0.1		LSB
AC ACCURACY (Note 6)							
Spurious-Free Dynamic Range	74	77		77	80		dB
Total Harmonic Distortion		−77	−74		−80	−77	dB
Signal-to-Noise Ratio	68	71		70	73		dB
Signal-to-(Noise+Distortion) Ratio (SINAD)	67	70		69	72		dB
Intermodulation Distortion (−6dB Signals) (f_{IN1} = 24.4kHz; f_{IN2} = 28.5kHz)		−77	−74		−77	−74	dB
POWER SUPPLY SENSITIVITY							
$-V_S = -13.5V$ to $-16.5V$			±½			±½	LSB
$-V_S = -11.4V$ to $-12.6V$			±½			±½	LSB
$+V_S = +4.75V$ to $+5.25V$			±1			±½	LSB
TEMPERATURE RANGE							
Specified: JP/JU/KP/KU Models	0		+70	0		+70	°C
AH/BH/ Models	−40		+85	−40		+85	°C
Storage	−65		+150	−65		+150	°C



ADS7800 BLOCK DIAGRAM

PIN DESIGNATIONS



1 ±10V Analog Input. Ground for ±5 range.
2 ±5V Analog Input. Ground for ±10V range.
3 +2V Reference Output
4 Analog Ground. Connect to Pin 13.
5 Data Bit 11 (MSB)
6 Data Bit 10
7 Data Bit 9
8 Data Bit 8
9 Data Bit 7 if HBE Low; "0" if HBE High.
10 Data Bit 6 if HBE Low; "0" if HBE High.
11 Data Bit 5 if HBE Low; "0" if HBE High.
12 Data Bit 4 if HBE Low; "0" if HBE High.
24 +5V Analog Power Supply. Connect to Pin 23.
23 +5V Digital Power Supply. Connect to Pin 24
22 −12V or −15V Negative Power Supply
21 $\overline{BUSY}$
20 $\overline{CS}$ Chip Select
19 R/C Read/Convert
18 HBE High Byte Enable
17 Data Bit 0 (LSB) if HBE Low, Data Bit 8 if HBE High.
16 Data Bit 1 if HBE Low; Data Bit 9 if HBE High.
15 Data Bit 2 if HBE Low; Data Bit 10 if HBE High.
14 Data Bit 3 if HBE Low; Data Bit 11 if HBE High.
13 Digital Ground. Connect to Pin 4.

DESCRIPTION OF OPERATION

The ADS7800 is a complete 12-bit A/D converter. It uses the successive-approximation conversion technique and incorporates all required function blocks — capacitor-array D/A converter, comparator, clock, reference, and control logic. The CMOS-based capacitor-array architecture provides an inherent sample/hold function. The device mates directly to most popular 8-, 16-, and 32-bit microprocessors and contains all the necessary address-decoding logic, control logic, and 3-state output buffering to operate completely under processor control. In most cases, the ADS7800 will require only power supplies and bypass capacitors to provide the complete A/D conversion function. The completeness of the device makes it most convenient to think of the ADS7800 as a function block with specific input/output transfer characteristics; it is thus quite unnecessary to be concerned with its inner workings.

BASIC OPERATION — Figure 1 gives the basic connections for operating the ADS7800 with the ±10V input range in Convert mode. The Convert command R/$\overline{C}$, applied to Pin 19, puts the ADS7800 in Hold mode and initiates the conversion. R/$\overline{C}$ must hold Pin 19 low for at least 40nsec. The $\overline{BUSY}$ signal on Pin 21 is held low during the conversion, and goes high after the conversion is completed and the data is transferred to the output latches. The rising edge of the signal on Pin 21 can thus serve to read the converted data.

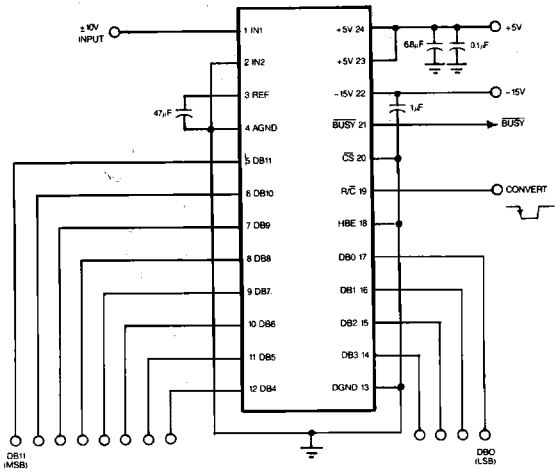


Figure 1. Basic ±10V Connection Diagram

During the conversion, the $\overline{BUSY}$ signal imposes the high-impedance state on the output data lines and also inhibits input lines. The inhibition causes Pin 19 to ignore any pulses, so new conversions cannot be initiated while a conversion is taking place, whether the pulses result from spurious sources or an attempt to short-cycle the conversion.

In Read mode, Pin 19 is held low, and a high-going pulse serves to read data and initiate a conversion. In Read mode, the rising edge of the R/$\overline{C}$ signal on Pin 19 enables the output data pins, thus validating the data from the previous conversion. The falling edge of R/$\overline{C}$ then puts the ADS7800 in Hold mode and initiates a new conversion. The ADS7800 will begin acquiring a new signal upon the completion of the conversion, even before the $\overline{BUSY}$ signal rises on Pin 21, and will track the input signal until the start of the next conversion, whether the ADS7800 is in Convert or Read mode.

The signal HBE on Pin 18 allows the ADS7800 to be used with an 8-bit bus. At the end of a conversion, a low input on Pin 18 loads the eight LSBs of data into the latches of Pins 9 through 12 and 14 through 17. A high signal on Pin 18 then loads the four MSBs into the latches of Pins 14 through 17, and Pins 9 through 12 are forced low. Figure 2 and Table 1 give the timing parameters for the basic acquisition and conversion operations.

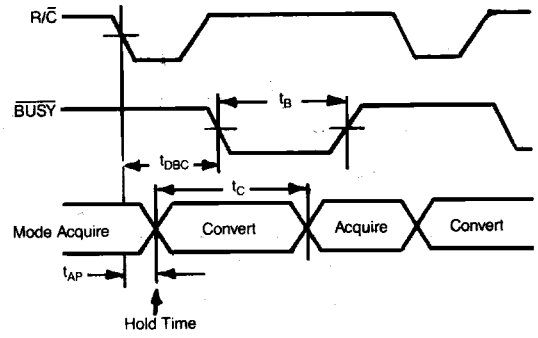


Figure 2. Conversion and Acquisition Timing

Symbol	Parameter	Typ	Max	Units
t_{DBC}	$\overline{BUSY}$ Delay from R/C	80	150	nsec
t_B	$\overline{BUSY}$ Low	2.5	2.7	µsec
t_{AP}	Aperture Delay	13		nsec
Δt_{AP}	Aperture Jitter	150		psec, rms
t_C	Conversion Time	2.47	2.70	µsec

Table 1. Acquisition and Conversion Timing

CONTROL FUNCTIONS — The ADS7800 offers easy interface to most digital systems, whether microprocessor-based or other. The ADS7800 can operate under complete microprocessor control, or in a stand- alone mode, in which it is controlled only by the R/$\overline{C}$ input on Pin 19. Microprocessor control entails initiating the conversion and reading the output data, either in one 12-bit parallel word or in two 8-bit bytes. All control inputs ($\overline{CS}$, R/$\overline{C}$, and HBE) are TTL- and CMOS-compatible. Tables 2 and 3 detail the functions of the control inputs.

Pin No.	Symbol	Function
18	HBE	High Byte Enable. When held Low, data output has 12-bit parallel format. When held High, 4 MSBs appear on Pins 14 to 17; zeros appear on Pins 9 to 12. Must be Low to initiate conversion.
19	R/$\overline{C}$	Read/Convert. Falling edge initiates conversion when $\overline{CS}$ is Low, HBE is Low, and $\overline{BUSY}$ is High.
20	$\overline{CS}$	Chip Select. Outputs in High-Z state when $\overline{CS}$ is High. Must be Low to initiate conversion or read data.
21	$\overline{BUSY}$	Busy, Output Low during conversion. Data valid on rising edge in Convert mode.

Table 2. Role of Control Functions

$\overline{CS}$	R/$\overline{C}$	HBE	$\overline{BUSY}$	Operation
1	X	X	1	None — Outputs in High-Z State.
0	1→0	0	1	Holds Signal and Starts Conversion.
0	1	0	1	3-State Output Buffers Enabled Upon End of Conversion.
0	1	1	1	Enable High Byte in 8-Bit Bus Mode.
0	1→0	1	1	Inhibits Start of Conversion.
X	X	X	0	Conversion in Progress. Outputs in High-Z State. New Conversion Inhibited Until End of Present Conversion.

X="Don't Care".

Table 3. Control Functions

In stand-alone mode, a single control line connected to R/$\overline{C}$ controls the ADS7800. $\overline{CS}$ and HBE are grounded in this mode. The output data is in 12-bit parallel format. Stand-alone mode is useful in systems using dedicated input ports that do not require full bus-interface capability.

A high-to-low transition on R/$\overline{C}$ initiates a conversion. The 3-state output latches are enabled when R/$\overline{C}$ and $\overline{BUSY}$ are high. Thus, two modes of operation are possible: Either positive or negative pulses can initiate a conversion. Either way, the R/$\overline{C}$ pulse must remain low for at least 40nsec.

Figure 3 and Table 4 give timing details for a conversion initiated by a negative R/$\overline{C}$ pulse. In this case (referred to as Convert mode), the 3-state outputs revert to the high-impedance state in response to the falling edge of R/$\overline{C}$, and become enabled for data access after the completion of the conversion.

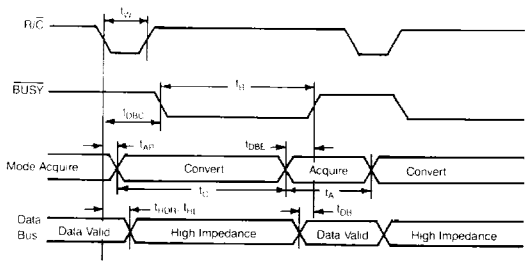


Figure 3. Timing with Negative R/C Pulse

Symbol	Parameter	Min.	Typ.	Max.	Units
t_W	R/$\overline{C}$ Pulse Width	40	10		nsec
t_{DBC}	$\overline{BUSY}$ Delay from R/$\overline{C}$		80	150	nsec
t_B	$\overline{BUSY}$ Low		2.5	2.7	μsec
t_{AP}	Aperture Delay		13		nsec
Δt_{AP}	Aperture Jitter		150		psec, rms
t_C	Conversion Time		2.47	2.7	μsec
t_{DBE}	$\overline{BUSY}$ from End of Conversion		100		nsec
t_{DB}	$\overline{BUSY}$ Delay after Data Valid	25	75	200	nsec
t_A	Acquisition Time		130	300	nsec
$t_A + t_C$	Total Throughput Time		2.6	3.0	μsec
t_{HDR}	Valid Data Held after R/$\overline{C}$ Low	20	50		nsec
t_S	$\overline{CS}$ or HBE Low before R/$\overline{C}$ 1→0 Transition	25	5		nsec
t_H	$\overline{CS}$ or HBE Low after R/$\overline{C}$ 1→0 Transition	25	0		nsec
t_{DD}	Data Valid from $\overline{CS}$ Low, R/$\overline{C}$ High, and HBE as Selected (100-pF Load)		65	150	nsec
t_{HDR}	Valid Data Held after R/$\overline{C}$ Low	20	50		nsec
t_{HL}	Delay to High-Z State after R/$\overline{C}$ Falls or $\overline{CS}$ Rises (3kΩ Pullup or Pulldown)		50	150	nsec

Table 4. Timing Specifications Over T_{MIN} to T_{MAX}.

Figure 4 and Table 4 detail the timing considerations for a conversion initiated by a positive R/$\overline{C}$ pulse. In this case (referred to as Read mode), output data from a previous conversion is enabled during the high portion of R/$\overline{C}$. The falling edge of R/$\overline{C}$ initiates a new conversion, and the 3-state outputs revert to the high-impedance state until R/$\overline{C}$ again attains a high state.

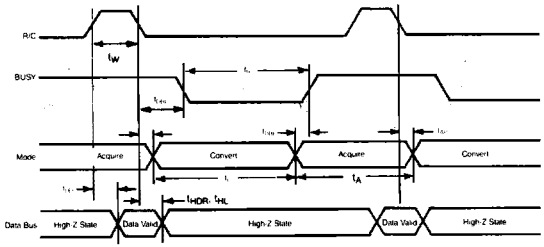


Figure 4. Timing with Positive R/$\overline{C}$ Pulse

TIMING — INITIATING CONVERSIONS — As seen in Table 1, only a negative-going transition on R/$\overline{C}$–no other combination of states or transitions–can initiate a conversion in the ADS7800. $\overline{CS}$ or HBE high, or $\overline{BUSY}$ low, will inhibit conversion. $\overline{CS}$ and HBE should be stable for at least 25 nsec prior to the R/$\overline{C}$ transition. Figure 5 shows the timing details for initiation of a conversion.

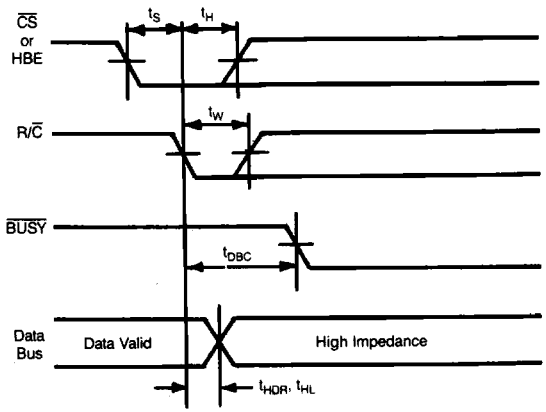


Figure 5. Conversion Initiation Timing

The $\overline{BUSY}$ line, in a low state only during a conversion, shows the status of the converter. During the conversion, the 3-state output latches remain in a high-impedance state; therefore, data is inaccessible during a conversion. During the conversion, the digital inputs $\overline{CS}$, R/$\overline{C}$, and HBE are immune to additional transitions, so conversions cannot be prematurely terminated or restarted.

TIMING — READING DATA — After the start of a conversion, the 3-state output buffers remain in a high-impedance state until the following logic combination exists: R/$\overline{C}$ is high, $\overline{BUSY}$ is high, and $\overline{CS}$ is low. When this combination occurs, the 3-state data lines are enabled in accordance with the state of HBE. Figure 6 and Table 4 give details of the timing relationships and specifications for reading data.

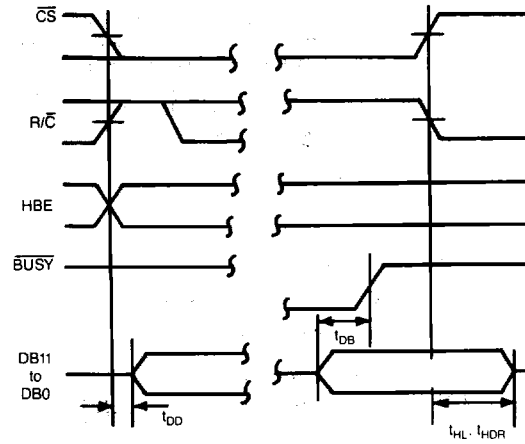


Figure 6. Read Cycle Timing

INTERNAL CLOCK — A factory-trimmed internal clock in the ADS7800 yields a typical conversion time of 2.47μsec at 25°C, and a maximum conversion time of 2.7μsec over the entire operating temperature range. This conversion time, coupled with a guaranteed maximum acquisition time of 300nsec, ensures a 333kHz minimum throughput rate under all conditions.

BIPOLAR OPERATION AND CALIBRATION — Analog input connections and calibration circuits for the ADS7800 are shown in Figure 7. If the ±5V input range is to be used, apply the analog input to Pin 2 and ground Pin 1. If the ±10V range is to be used, apply the analog input to Pin 1 and ground Pin 2. If either offset or gain adjustments are not to be used, the ADS7800 will perform to the limits in the specification table.

Bipolar offset (zero) error can be defined as the accuracy of the 0111 1111 1111 to 1000 0000 0000 transition voltage (-2.44mV for the ±10V range; -1.22mV for the ±5V range). With the ADS7800 converting continuously, adjust the 10kΩ trimpot "up" until the output code is 1000 0000 0000, then adjust "down" until all bits are "flickering" between "0" and "1".

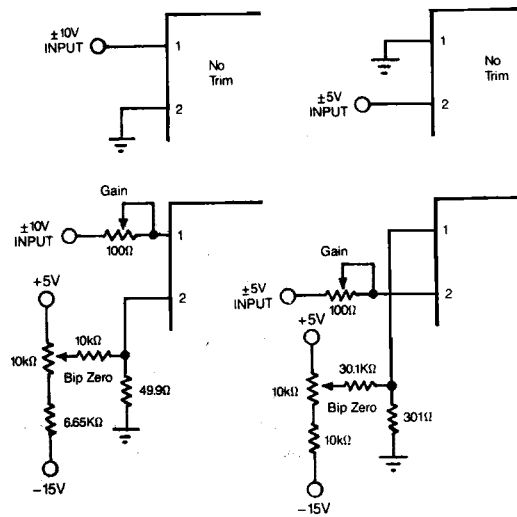


Figure 7. Connections and Calibration

Bipolar gain error can be defined as the accuracy of the 1111 1111 1110 to 1111 1111 1111 digital output transition after the bipolar offset adjustment has been effected. Ideally, this transition should occur 1½LSBs below the nominal positive full-scale value of the selected input range. This corresponds to +4.9963V and +9.9927V for the ±5V and ±10V ranges, respectively. Gain trimming is accomplished by applying either of these voltages and adjusting the gain trimpot "up" until the digital outputs are all ones, then adjusting "down" until the LSB "flickers" between "1" and "0".

LAYOUT CONSIDERATIONS AND GROUNDING — The ADS7800 has two +5V supply pins: V_{SA} (Pin 24) and V_{SD} (Pin 23). To achieve maximum accuracy in the ADS7800, these supplies are not connected internally. They should be connected together on the printed- circuit board, at a point as close as possible to the ADS7800. Both supply lines should be well isolated from digital supplies that are subject to large load variations. As a general rule, it is good practice to isolate the analog portions of a system from the effects of digital switching by running a separate +5V supply line from a supply regulator to the analog components.

To minimize noise, the tied-together V_S Pins 23 and 24 should be bypassed to ground with a 6.8μF tantalum capacitor in parallel with a 0.1μF multilayer ceramic capacitor. The $-V_S$ Pin 22 should also be bypassed to ground with a 1μF tantalum capacitor. All bypass capacitors should be connected as close as possible to the ADS7800.

These bypassing measures are extremely important, as noise on the power-supply lines can degrade converter performance. It is necessary to pay special attention to filtering out noise and spikes when a switching power supply is used.

The analog (Pin 4) and digital (Pin 13) ground pins are also not connected internally, and should be connected together as close as possible to the ADS7800. The use of a ground plane on the printed- circuit board is highly recommended, as it optimizes high- frequency ground characteristics and reduces noise coupling into sensitive converter circuitry. It is especially important to reference the analog input to the analog ground on Pin 4, to eliminate from the input circuitry any voltage drops that might occur in the power-supply ground returns.

It is necessary to take the input impedance of the ADS7800 into account when designing the analog drive circuitry. The output impedance of the driver should be negligible with respect to the 6.3kΩ (±10V range) or 4.2kΩ (±5V range) input impedance of the ADS7800, or at least invariant with respect to signal level. Further, it is crucial to prevent any coupling between the analog input lines and digital signal lines. If these lines must cross, it is recommended that they do so at right angles, and with a minimum of crossover area. If they must run parallel for any distance, it is good design practice to insert a ground pattern between them as a shield. Any external trimpots used for full-scale or offset adjustments should be mounted as close to the converter as possible.

It is necessary to bypass the reference output (Pin 3) with a 22μF to 47μF, 2V tantalum capacitor. The drive capability of this pin is limited (10μA typ), so it is necessary to provide buffering if this reference voltage is to be used in other parts of the system.

POWER-SUPPLY SEQUENCING PRECAUTIONS — If the two +5V supply inputs of the ADS7800 are powered-up sequentially instead of simultaneously, the converter may experience latch-up and draw excessive current. Connecting the two supply pins together on the printed-circuit board will normally prevent this problem. However, the phenomenon can occur if the ADS7800 is plugged into a live socket– for example, during incoming inspection or lab evaluation. In these cases, it is necessary to ensure that power is applied only after the ADS7800 has been plugged in.

AVOIDING TRANSIENT PHENOMENA — Various transients coupled into the ADS7800 can cause errors that may difficult to diagnose. If errors persist despite careful grounding and bypassing measures, they might find their origins in one or more not-so-obvious transient phenomena. A checklist of several transient-avoidance steps can be useful in designing a new system.

Transients that occur during critical periods in the conversion process can produce errors. For example, a clean, sharp Hold command ("1" to "0" transition on R/C) signal is crucial to error- free operation. This edge should be clean and sharp and free from significant ringing, especially in the 20nsec period after it occurs. Another not-so-obvious helpful design practice is to avoid any transitions on digital lines during the bit decisions in the conversion process. So it is prudent to avoid any changes in R/C at the time of any bit decisions. Keeping the R/C pulse short (< 100nsec) will avoid a transition at the time of the MSB decision, or keeping it long (> 2.7μsec) will avoid affecting the LSB decision.

High-speed bus transients can also couple into the ADS7800 via the data outputs, even when the output buffers are in the high- impedance state. If such transients exist, it is good practice to isolate them from the converter by providing additional buffering to the data outputs. The BUSY line can serve to enable these added buffers.

It goes without saying that transients on the analog inputs are to be avoided scrupulously, especially in the interval within ±20nsec of the "1"-to-"0" transition of R/C, when they may affect the charge transferred to the capacitor array. Careful layout and design of the analog drive circuitry are necessary to avoid these transients. Finally, in multiplexed systems, it is most prudent to switch channels in the multiplexer only after the conversion is complete. Otherwise, glitches or ringing in the switched signal may be coupled into the ADS7800 during the conversion process.

DIGITAL OUTPUT CODING

ANALOG INPUT (Volts)		DIGITAL OUTPUT	
±5V	±10V	MSB	LSB
+5.0000	+10.0000	1111 1111	1111
+4.9963	+9.9927	1111 1111	111Ø *
+0.0012	+0.0024	1000 0000	000Ø *
−0.0012	−0.0024	ØØØØ ØØØØ	ØØØØ *
−0.0037	−0.0073	0111 1111	111Ø *
−4.9988	−9.9976	0000 0000	000Ø *
−5.0000	−10.0000	0000 0000	0000

DIGITAL OUTPUT CODING NOTES:

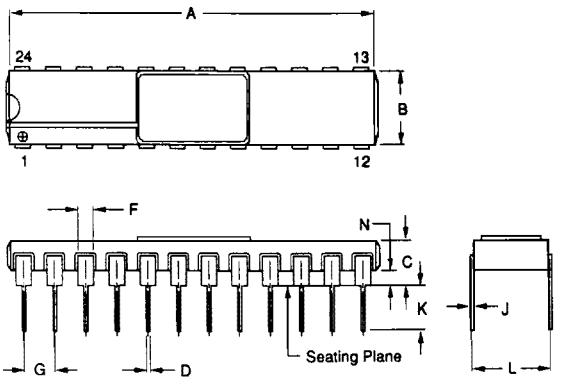
1. Output coding is offset binary.
2. For ±5V input range, 1LSB for 12 bits = 2.44mV. 1LSB for 11 bits = 4.88mV.
3. For ±10V input range, 1LSB for 12 bits = 4.88mV. 1LSB for 11 bits = 9.77mV.

* Voltages given are the theoretical values for the transitions indicated. Ideally, with the converter continuously converting, the output bits indicated as Ø will change from a logic "1" to a logic "0" or visa versa as the input voltage passes through the level indicated.

EXAMPLE: For an ADS7800 operating on its ±10V input range, the transition from digital output 0000 0000 0001 (or vice versa) will ideally occur at an input voltage of −9.9976 volts. Subsequently, any input voltage more negative than −9.9976 volts will give a digital output of all "0's". The transition from digital output 1000 0000 0000 to 0111 1111 1111 will ideally occur at an input of −0.0024 volts, and the 1111 1111 1111 to 1111 1111 1110 transition should occur at +9.9927 volts. An input more positive than +9.9927 volts will give all "1's".

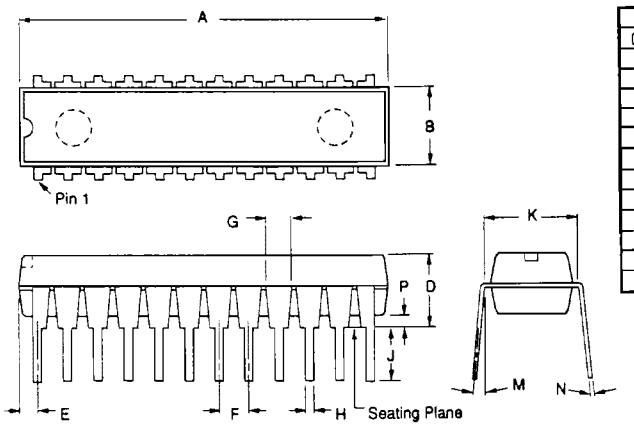
PACKAGE OUTLINES

PACKAGE H. CERAMIC HERMETIC DIP



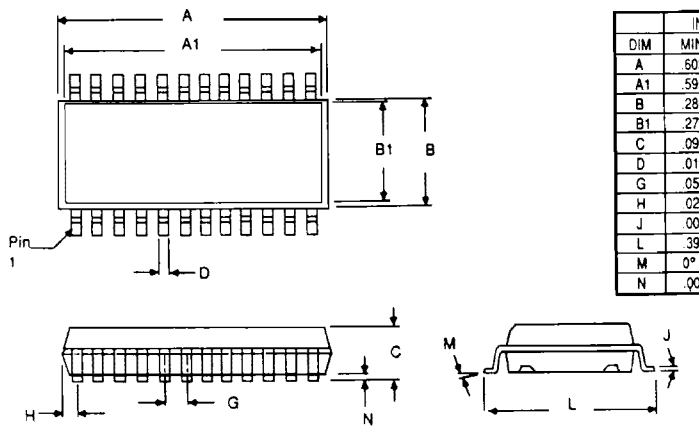
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.188	1.212	30.18	30.78
B	.300	.320	7.62	8.13
C	—	.160	—	4.06
D	.016	.020	0.41	0.51
F	.050 TYP		1.27 TYP	
G	.095	.105	2.41	2.67
J	.009	.012	0.23	0.31
K	.170 BASIC		4.32 BASIC	
L	.290	.310	7.37	7.87
N	.040	.060	1.02	1.52

PACKAGE P. PLASTIC DIP



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.125	1.255	28.58	31.88
B	.250	.290	6.35	7.37
D	.150	.170	3.81	4.32
E	.010	.080	.25	2.03
F	.100 BASIC		2.54 BASIC	
G	.050	.070	1.27	1.78
H	.016	.020	0.41	0.51
J	.125		3.18	
K	.300 BASIC		7.63 BASIC	
M	0°	15°	0°	15°
N	.008	.015	0.20	0.38
P	.010	.030	.25	.76

PACKAGE U. PLASTIC SOIC



	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	.602	.618	15.29	15.70
A1	.595	.618	15.11	15.70
B	.286	.302	7.26	7.67
B1	.270	.285	6.86	7.24
C	.093	.108	2.36	2.74
D	.015	.019	0.38	0.48
G	.050 BASIC		1.27 BASIC	
H	.026	.034	0.66	0.86
J	.008	.012	0.20	0.30
L	.390	.422	9.91	10.72
M	0°	10°	0°	10°
N	.000	.012	0.00	0.30