CS4207

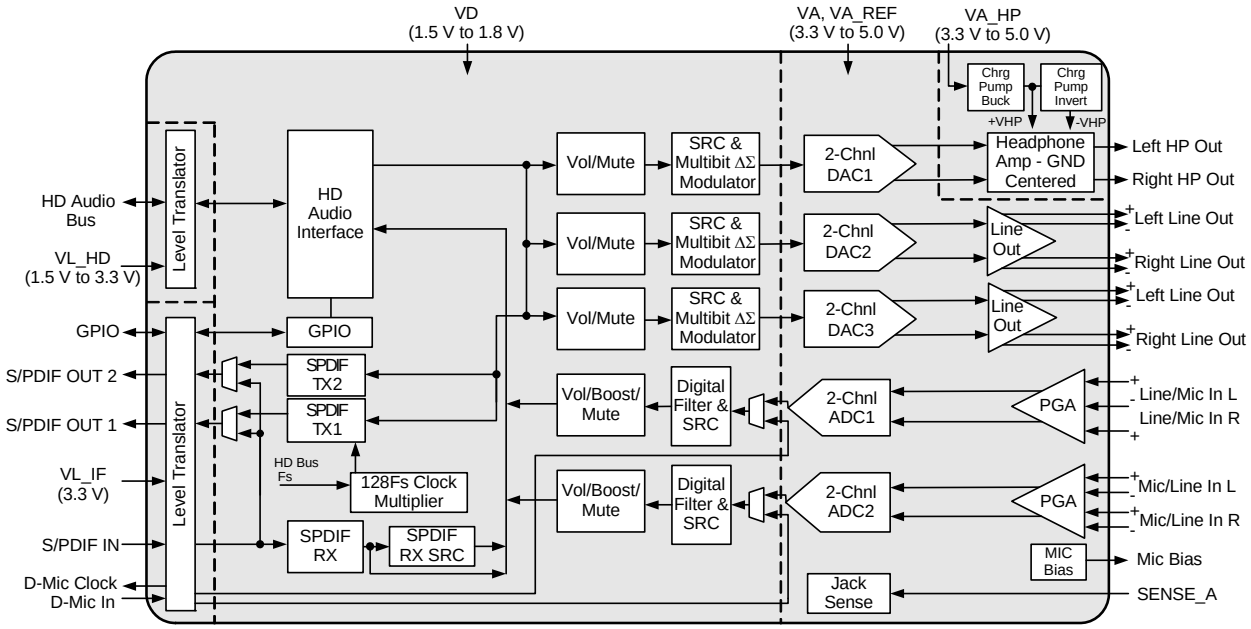
Low-power, 4-in / 6-out HD Audio Codec with Headphone Amp

DIGITAL to ANALOG FEATURES

- DAC1 (Headphone)
  - 101 dB Dynamic Range (A-wtd)
  - -89 dB THD+N
- Headphone Amplifier - GND Centered
  - Integrated Negative-voltage Regulator
  - No DC-blocking Capacitor Required
  - 50 mW Power/Channel into 16 Ω
- DAC2 & DAC3 (Line Outs)
  - 110 dB Dynamic Range (A-wtd)
  - -94 dB THD+N
  - Differential Balanced or Single-ended
- Each DAC Supports 32 kHz to 192 kHz Sample Rates Independently.
- Digital Volume Control
  - +6.0 dB to -57.5 dB in 0.5 dB Steps
  - Zero Cross and/or Soft Ramp Transitions
- Independent Support of D0 and D3 Power States for Each DAC
- Fast D3 to D0 Transition
  - Audio Playback in Less Than 50 ms

ANALOG to DIGITAL FEATURES

- ADC1 & ADC2
  - 105 dB Dynamic Range (A-wtd)
  - -88 dB THD+N
  - Differential Balanced or Single-ended Inputs
  - Analog Programmable Gain Amplifier (PGA) ±12 dB, 1.0 dB Steps, with Zero Cross Transitions and Mute
- MIC Inputs
  - Pre-amplifier with Selectable 0 dB, +10 dB, +20 dB, and +30 dB Gain Settings
  - Programmable, Low-noise MIC Bias Level
- Each ADC Supports 8 kHz to 96 kHz Sample Rates Independently
- Additional Digital Attenuation Control
  - -13.0 dB to -51.0 dB in 1.0 dB steps
  - Zero Cross and/or Soft Ramp Transitions
- Digital Interface for Two Dual Digital Mic Inputs
- Independent Support of D0 and D3 Power States for Each ADC



Digital Audio Interface Receiver

- Complete EIAJ CP1201, IEC 60958, S/PDIF Compatible Receiver
- 32 kHz to 192 kHz Sample Rate Range
- Automatic Detection of Compressed Audio Streams
- Integrated Sample Rate Converter
  - 128 dB Dynamic Range
  - -120 dB THD+N
  - Supports Sample Rates up to 192 kHz
  - 1:1 Input/Output Sample Rate Ratios

Digital Audio Interface Transmitters

- Two Independent EIAJ CP1201, IEC-60958, S/PDIF Compatible Transmitters
- 32 kHz to 192 kHz Sample Rate Range

System Features

- Very Low D3 Power Dissipation of <7 mW
  - Jack Detect Active in D3
  - HDA BITCLK Not Required for D3 State
- Jack Detect Does Not Require HDA Bus BITCLK
- All Configuration Settings are Preserved in D3 State
- Pop/Click Suppression in State Transitions
- Detects Wake Event and Generates Power State Change Request when HDA Bus Controller is in D3
- Variable Power Supplies
  - 1.5 V to 1.8 V Digital Core Voltage
  - 3.3 V to 5.0 V Analog Core Voltage
  - 3.3 V to 5.0 V Headphone Drivers
  - 1.5 V to 3.3 V HD Bus Interface Logic
  - 3.3 V Interface Logic levels for GPIO, S/PDIF, and Digital Mic
- Individual Power-down Managed
  - ADCs, DACs, PGAs, Headphone Driver, S/PDIF Receiver, and Transmitters

General Description

The CS4207 is a highly integrated multi-channel low-power HD Audio Codec featuring 192 kHz DACs, 96 kHz ADCs, 192 kHz S/PDIF Transmitters and Receiver, Microphone pre-amp and bias voltage, and a ground centered Headphone driver. Based on multi-bit, delta-sigma modulation, it allows infinite sample rate adjustment between 32 kHz and 192 kHz.

The ADC input path allows control of a number of features. The microphone input path includes a selectable programmable-gain pre-amplifier stage and a low-noise MIC bias voltage supply. A PGA is available for line and microphone inputs and provides analog gain with soft ramp and zero cross transitions. The ADC also features an additional digital volume attenuator with soft ramp transitions.

The stereo headphone amplifier is powered from a separate internally generated positive supply, with an integrated charge pump providing a negative supply. This allows a ground-centered analog output with a wide signal swing and eliminates external DC-blocking capacitors.

The integrated digital audio interface receiver and transmitters utilize a 24-bit, high-performance, monolithic CMOS stereo asynchronous sample rate converter to clock align the PCM samples to/from the S/PDIF interfaces. Auto detection of non-PCM encoded data disables the sample rate conversion to preserve bit accuracy of the data.

In addition to its many features, the CS4207 operates from a low-voltage analog and digital core, making this part ideal for portable systems that require low power consumption in a minimal amount of space.

The CS4207 is available in a 48-pin WQFN package in both Automotive (-40°C to +105°C) and Commercial (-40°C to +85°C) grades. The CS4207 Customer Demonstration board is also available for device evaluation and implementation suggestions. Please refer to "Ordering Information" on p 147 for complete ordering information.

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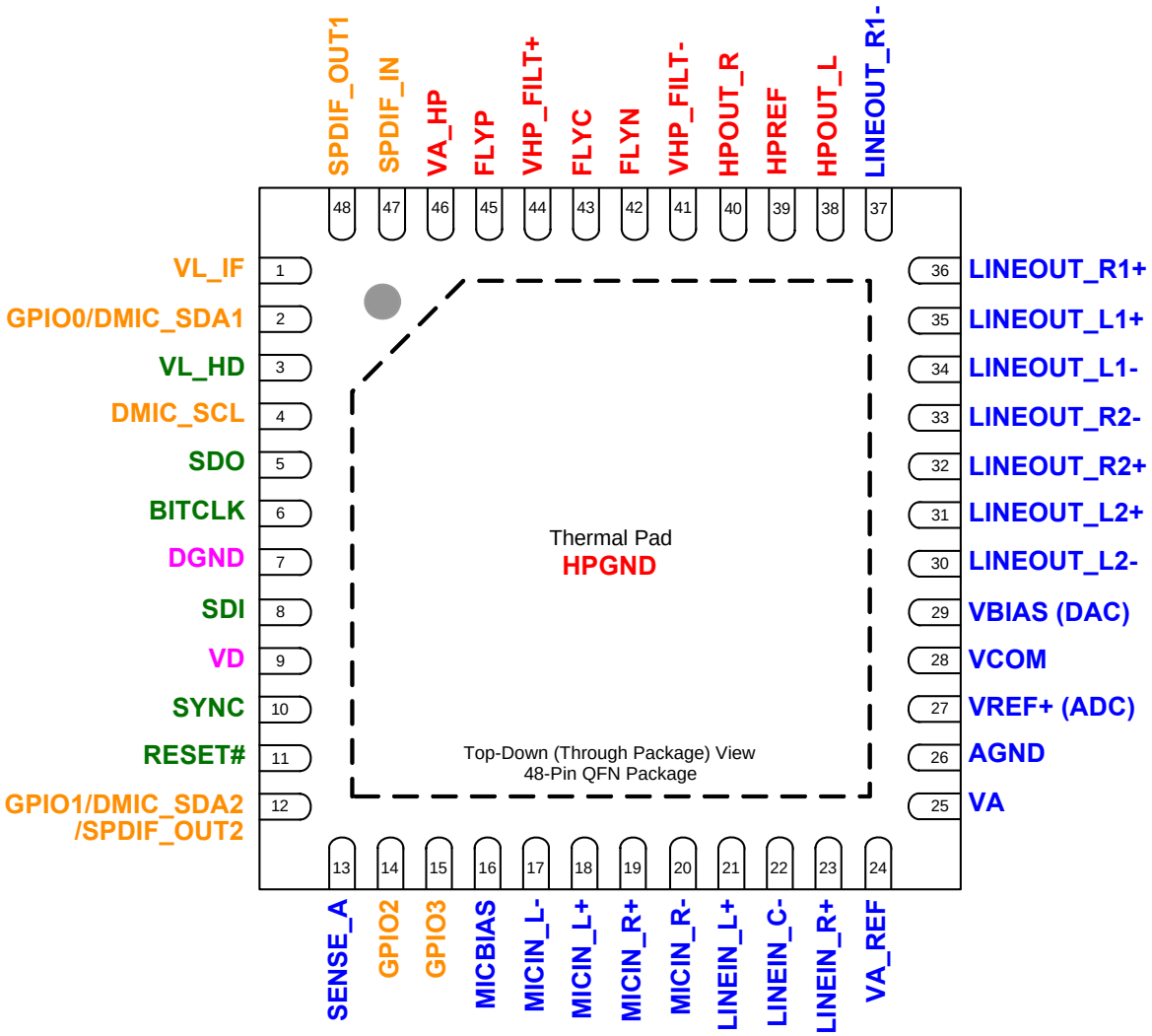
1. PIN DESCRIPTIONS

1.1 CS4207 48-pin QFN Pinout:



Pin Name	QFN	Pin Description
VL_IF	1	**Digital Interface Signal Level** (*Input*) - Digital supply for the GPIO, S/PDIF and Digital Mic interfaces. Refer to the Recommended Operating Conditions for appropriate voltages.
GPIO0/ DMIC_SDA1	2	**General Purpose I/O** (*Input/Output*) - General purpose input or output line, or **Digital Mic Data Input** (*Input*) - The first data input line from a digital microphone.
VL_HD	3	**Digital Interface Signal Level** (*Input*) - Digital supply for the HD Audio interface. Refer to the Recommended Operating Conditions for appropriate voltages.
DMIC_SCL	4	**Digital Mic Clock** (*Output*) - The high speed clock output to the digital microphone.
SDO	5	**Serial Data Input** (*Input*) - Serial data input stream from the HD Audio Bus.
BITCLK	6	**Bit Clock** (*Input*) - 24 MHz bit clock from the HD Audio Bus.
DGND	7	**Digital Ground** (*Input*) - Ground reference for the internal digital section.
SDI	8	**Serial Data Output** *(Input/Output*) - Serial data output stream to the HD Audio Bus.
VD	9	**Digital Power** (*Input*) - Positive power for the internal digital section.
SYNC	10	**Sync Clock** (*Input*) - 48 kHz sync clock from the HD Audio Bus.

Pin Name	QFN	Pin Description
RESET#	11	**Reset** (*Input*) - The device enters a low power mode when this pin is driven low.
GPIO1/ DMIC_SDA2/ SPDIF_OUT2	12	**General Purpose I/O** (*Input/Output*) - General purpose input or output line, or **Digital Mic Data Input** (*Input*) - The second data input line from a digital microphone, or **S/PDIF Output** (*Output*) - Output from internal S/PDIF Transmitter.
SENSE_A	13	**Jack Sense Pin** (*Input/Output*) - Jack sense detect.
GPIO2	14	**General Purpose I/O** (*Input/Output*) - General purpose input or output lines.
GPIO3	15	**General Purpose I/O** (*Input/Output*) - General purpose input or output lines.
MICBIAS	16	**Microphone Bias** (*Output*) - Provides a low noise bias supply for an external microphone. Electrical characteristics are specified in the DC Electrical Characteristics table.
MICIN_L- MICIN_L+ MICIN_R+ MICIN_R-	17 18 19 20	**Microphone Input Left/Right** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
LINEIN_L+ LINEIN_C- LINEIN_R+	21 22 23	**Analog Input** (*Input*) - The full-scale level is specified in the ADC Analog Characteristics specification table.
VA_REF VA	24 25	**Analog Power** (*Input*) - Positive power for the internal analog section. VA_REF is the return pin for the VBIAS cap.
AGND	26	**Analog Ground** (*Input*) - Ground reference for the internal analog section.
VREF+	27	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal ADCs.
VCOM	28	**Quiescent Voltage** (*Output*) - Filter connection for internal quiescent voltage.
VBIAS	29	**Positive Voltage Reference** (*Output*) - Positive reference voltage for the internal DACs.
LINEOUT_L2- LINEOUT_L2+ LINEOUT_R2+ LINEOUT_R2- LINEOUT_L1- LINEOUT_L1+ LINEOUT_R1+ LINEOUT_R1-	30 31 32 33 34 35 36 37	**Analog Audio Output** (*Output*) - The full-scale output level is specified in the DAC Analog Characteristics specification table
HPOUT_L HPOUT_R	38 40	**Analog Headphone Output** *(Output)* **-** The full-scale output level is specified in the DAC Analog Characteristics specification table.
HPREF	39	**Pseudo Diff. Headphone Reference** (*Input*) - Ground reference for the headphone amplifiers.
VHP_FILT-	41	**Inverting Charge Pump Filter Connection** *(Output)* **-** Power supply from the inverting charge pump that provides the negative rail for the headphone amplifier.
FLYN	42	**Charge Pump Cap Negative Node** *(Output)* **-** Negative node for the inverting charge pump's flying capacitor.
FLYC	43	**Charge Pump Cap Common Node** *(Output)* **-** Common positive node for the step-down and inverting charge pumps' flying capacitor.
VHP_FILT+	44	**Non-Inverting Charge Pump Filter Connection** *(Output)* **-** Power supply from the step-down charge pump that provides the positive rail for the headphone amplifier.
FLYP	45	**Charge Pump Cap Positive Node** *(Output)* **-** Positive node for the step-down charge pump's flying capacitor.
VA_HP	46	**Analog Power For Headphone** *(Input)* **-** Positive power for the internal analog headphone section.
SPDIF_IN	47	**S/PDIF Input** (*Input*) - Input to internal S/PDIF Receiver.
SPDIF_OUT1	48	**S/PDIF Output** (*Output*) - Output from internal S/PDIF Transmitter.
HPGND	TP	**HP Ground** (*Input*) - Ground reference for the internal headphone section. See "QFN Thermal Pad" on page 144 for more information.

1.2 Digital I/O Pin Characteristics

Input and output levels and associated power supply voltage are shown in the table below. Logic levels should not exceed the corresponding power supply voltage.

Power Supply	Pin Name SW/(HW)	I/O	Driver	Receiver
VL_HD	RESET#	Input	-	1.5 V - 3.3 V
	SDO	Input	-	1.5 V - 3.3 V
	BITCLK	Input	-	1.5 V - 3.3 V
	SDI (Note 1)	Input/Output	1.5 V - 3.3 V	1.5 V - 3.3 V
	SYNC	Input	-	1.5 V - 3.3 V
VA	SENSE_A	Input	-	3.3 V - 5.0 V
VL_IF	GPIO1/ DMIC_SDA2	Input/Output	3.3 V	3.3 V
	GPIO2	Input/Output	3.3 V	3.3 V
	GPIO3	Input/Output	3.3 V	3.3 V
	SPDIF_IN	Input	-	3.3 V
	SPDIF_OUT	Output	3.3 V	-
	GPIO0/ DMIC_SDA1	Input/Output	3.3 V	3.3 V
	DMIC_SCL	Output	3.3 V	-

Notes:

1. SDI output functionality also requires the VA and VL_IF rails to be at nominal levels.

2. TYPICAL CONNECTION DIAGRAMS

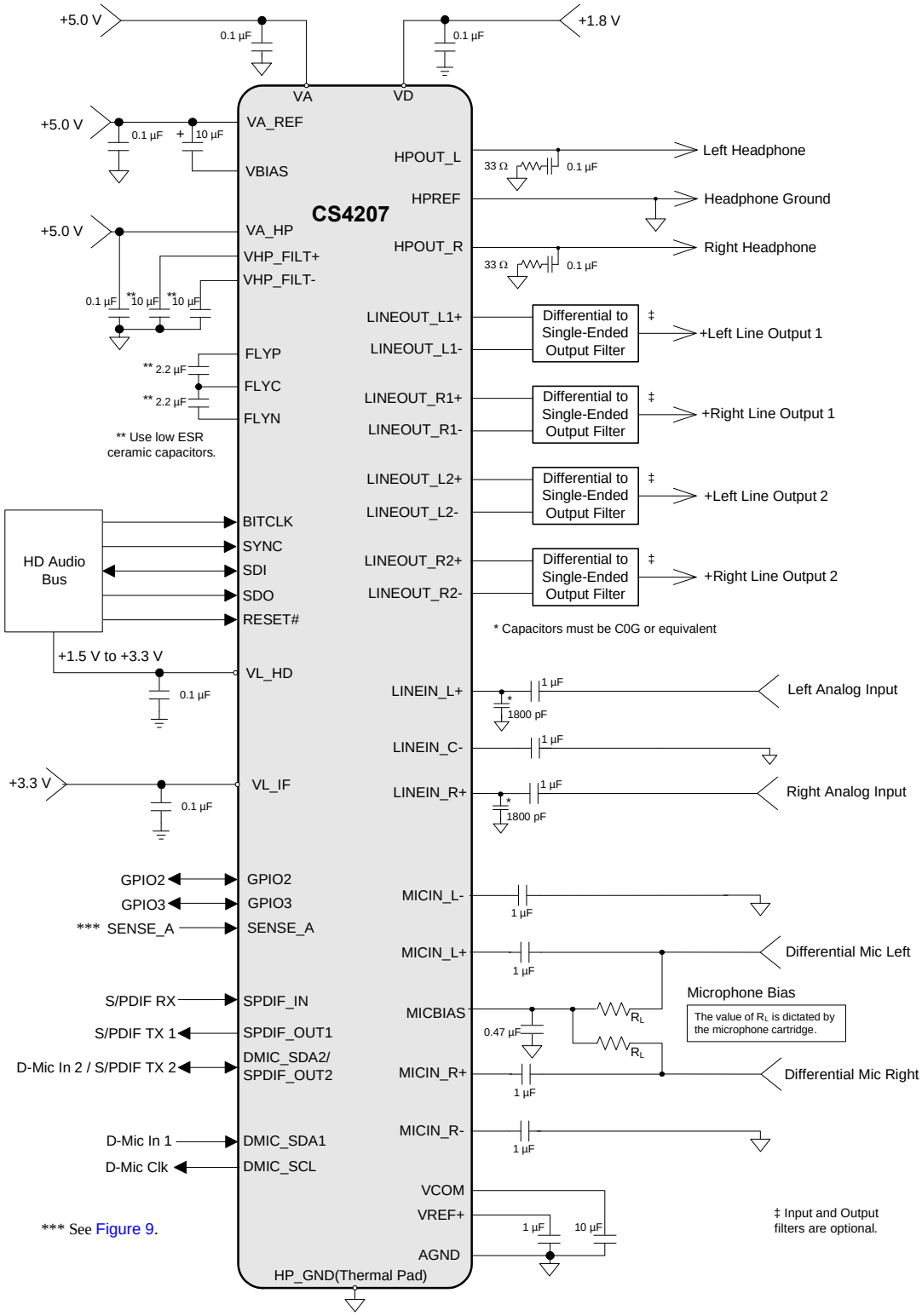


Figure 1. Typical Connection Diagram - Desktop System

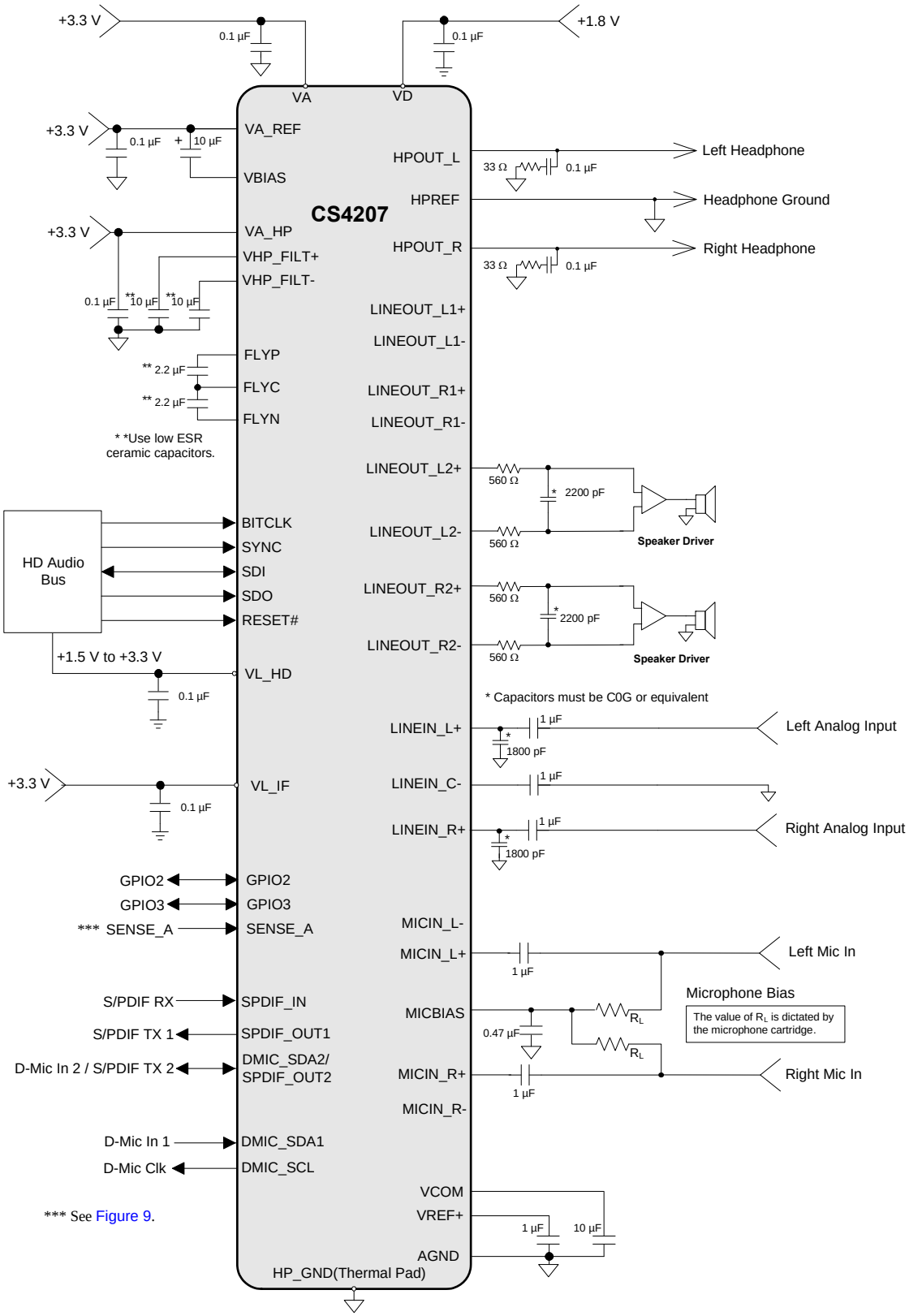


Figure 2. Typical Connection Diagram - Portable System

3. CHARACTERISTICS AND SPECIFICATIONS

RECOMMENDED OPERATING CONDITIONS

(AGND=DGND=0 V, all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply (Note 1)				
Analog Core	VA	2.97	5.25	V
DAC Reference	VA_REF	2.97	5.25	V
Headphone Amplifier	VA_HP	2.97	5.25	V
Digital Core	VD	1.42	1.89	V
HD Audio Bus Interface	VL_HD	1.42	3.47	V
GPIO, S/PDIF and Digital Mic Interface	VL_IF	2.97	3.47	V
Ambient Temperature Commercial - CNZ	T_A	-40	+85	°C
Ambient Temperature Automotive - DNZ	T_A	-40	+105	°C

ABSOLUTE MAXIMUM RATINGS

(AGND = DGND = 0 V; all voltages with respect to ground.)

Parameters	Symbol	Min	Max	Units
DC Power Supply Analog Core	VA	-0.3	5.5	V
DAC Reference	VA_REF	-0.3	5.5	V
Headphone Amplifier	VA_HP	-0.3	5.5	V
Digital Core	VD	-0.3	3.0	V
HD Audio Interface	VL_HD	-0.3	4.0	V
GPIO, S/PDIF and Digital Mic Interface	VL_IF	-0.3	4.0	V
Input Current (Note 2)	I_{in}	-	±10	mA
Analog Input Voltage (Note 3)	V_{IN}	AGND-0.7	VA+0.7	V
Digital Input Voltage (Note 3) HD Audio Interface	V_{IND}	-0.3	VL_HD+0.4	V
GPIO, S/PDIF and Digital Mic Interface	V_{IND}	-0.3	VL_IF+0.4	V
Ambient Operating Temperature (power applied)	T_A	-55	+115	°C
Storage Temperature	T_{stg}	-65	+150	°C

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

Notes:

1. The device will operate properly over the full range of the analog, digital and interface supplies.
2. Any pin except supplies. Transient currents of up to ±100 mA on the analog input pins will not cause SCR latch-up.
3. The maximum over/under voltage is limited by the input current.

ANALOG INPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full-scale): 1 kHz through passive input filter; VA_HP = VA; VL_HD = VL_IF = 3.3; VD = 1.8 V; T_A = +25°C; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
Line In to PGA to ADC (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	99/96	105/102	-	95/93	101/99	-	dB
	unweighted	96/93	102/99	-	92/90	98/96	-	dB
PGA Setting: +12 dB	A-weighted	95/86	101/92	-	92/83	98/89	-	dB
	unweighted	92/83	98/89	-	89/80	95/86	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88/-88	-82/-82	-	-95/-92	-89/-86	dB
	-60 dBFS	-	-42/-39	-36/-33	-	-38/-36	-32/-30	dB
PGA Setting: +12 dB	-1 dBFS	-	-88/-88	-82/-82	-	-92/-86	-86/-80	dB
Mic In to PGA to ADC (+20 dB) (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)								
Dynamic Range								
	A-weighted	86/78	92/84	-	83/75	89/81	-	dB
	unweighted	83/75	89/81	-	80/72	86/78	-	dB
Total Harmonic Distortion + Noise								
	-1 dBFS	-	-89/-82	-83/-76	-	-86/-78	-80/-72	dB
Other Analog Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	High Pass Filter On	-	352	-	-	352	-	LSB
Interchannel Isolation		-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation								
	R_L = 10 kΩ	-	100	-	-	100	-	dB
	R_L = 16 Ω	-	70	-	-	70	-	dB
Full-scale Input Voltage - Line In/Mic In (Differential Inputs)	PGA(0dB)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Full-scale Input Voltage - Line In (Single-ended Inputs)	PGA (0dB)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
	PGA (+12dB)		0.21•VA			0.21•VA		Vpp
Full-scale Input Voltage - Mic In								
	PGA+Boost(0dB)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
(Single-ended Inputs)	PGA+Boost(+20dB)		0.08•VA			0.08•VA		Vpp
Input Impedance (Note 5)								
	Mic In (Differential or Pseudo-Diff)	-	43.5	-	-	43.5	-	kΩ
	Line In (Pseudo-Diff, PGA = -12/0/+12 dB)	-	93/99/103	-	-	93/99/103	-	kΩ
	Mic/Line In (Single-Ended, PGA = -12/0/+12 dB)	-	27/33/37	-	-	27/33/37	-	kΩ
Common Mode Rejection (Differential Inputs)		-	60	-	-	60	-	dB

ANALOG INPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test Conditions (unless otherwise specified): Input sine wave (relative to digital full-scale): 1 kHz through passive input filter; VA_HP = VA; VL_HD = VL_IF = 3.3; VD = 1.8 V; T_A = -40 to +85°C; Measurement Bandwidth is 10 Hz to 20 kHz unless otherwise specified. Sample Frequency = 48 kHz)

Parameter (Note 4)		VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
Line In to PGA to ADC (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)								
Dynamic Range								
PGA Setting: 0 dB	A-weighted	99/96	105/102	-	95/93	101/99	-	dB
	unweighted	96/93	102/99	-	92/90	98/96	-	dB
PGA Setting: +12 dB	A-weighted	95/86	101/92	-	92/83	98/89	-	dB
	unweighted	92/83	98/89	-	89/80	95/86	-	dB
Total Harmonic Distortion + Noise								
PGA Setting: 0 dB	-1 dBFS	-	-88/-88	-82/-82	-	-95/-92	-89/-86	dB
	-60 dBFS	-	-42/-39	-36/-33	-	-38/-36	-32/-30	dB
PGA Setting: +12 dB	-1 dBFS	-	-88/-88	-82/-82	-	-92/-86	-86/-80	dB
Mic In to PGA to ADC (+20 dB) (ADC1 or ADC2; differential perf. characteristics only valid for ADC2)								
Dynamic Range								
	A-weighted	86/78	92/84	-	83/75	89/81	-	dB
	unweighted	83/75	89/81	-	80/72	86/78	-	dB
Total Harmonic Distortion + Noise								
	-1 dBFS	-	-89/-82	-83/-76	-	-86/-78	-80/-72	dB
Other Analog Characteristics								
DC Accuracy								
Interchannel Gain Mismatch		-	0.2	-	-	0.2	-	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
Offset Error	High Pass Filter On	-	352	-	-	352	-	LSB
Interchannel Isolation		-	90	-	-	90	-	dB
HP Amp to Analog Input Isolation								
	R_L = 10 kΩ	-	100	-	-	100	-	dB
	R_L = 16 Ω	-	70	-	-	70	-	dB
Full-scale Input Voltage - Line In/Mic In (Differential Inputs)	PGA(0dB)	1.58•VA	1.66•VA	1.74•VA	1.58•VA	1.66•VA	1.74•VA	Vpp
Full-scale Input Voltage - Line In (Single-ended Inputs)	PGA(0dB)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
	PGA(+12dB)		0.21•VA			0.21•VA		Vpp
Full-scale Input Voltage - Mic In								
	PGA+Boost(0dB)	0.79•VA	0.83•VA	0.87•VA	0.79•VA	0.83•VA	0.87•VA	Vpp
(Single-ended Inputs)	PGA+Boost(+20dB)		0.08•VA			0.08•VA		Vpp
Input Impedance (Note 5)		-		-	-		-	
	Mic In (Differential or Pseudo-Diff)		43.5			43.5		kΩ
	Line In (Pseudo-Diff, PGA = -12/0/+12 dB)		93/99/103			93/99/103		kΩ
	Mic/Line In (Single-Ended, PGA = -12/0/+12 dB)		27/33/37			27/33/37		kΩ
Common Mode Rejection (Differential Inputs)		-	60	-	-	60	-	dB

4. Referred to the typical full-scale voltage. Applies to all THD+N and Dynamic Range values in the table.
5. Measured between [LINE/MIC]IN_[L/R]+ and [LINE/MIC]IN_[C/L/R]- for differential and pseudo-differential inputs, and between [LINE/MIC]IN_[L/R]+ and AGND for single-ended inputs.

ADC DIGITAL FILTER CHARACTERISTICS

Parameter (Note 6)		Min	Typ	Max	Unit
Passband (Frequency Response)	to -0.1 dB corner	0	-	.4535	Fs
Passband Ripple		-0.09	-	0.17	dB
Stopband		0.6	-	-	Fs
Stopband Attenuation		70	-	-	dB
Total Group Delay		-	7.6/Fs	-	s
***High-Pass Filter Characteristics* (48 kHz Fs)**					
Frequency Response	-3.0 dB -0.13 dB	- -	3.6 24.2	- -	Hz Hz
Phase Deviation	@ 20 Hz	-	10	-	Deg
Passband Ripple		-	-	0.17	dB
Filter Settling Time		-	10^5/Fs	0	s

6. Response is clock dependent and will scale with Fs.

ANALOG OUTPUT CHARACTERISTICS (COMMERCIAL - CNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; VD = 1.8 V; VL_HD = VL_IF = 3.3V; T_A = +25°C; Measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output and test load R_L = 16 Ω, C_L = 10 pF for the headphone output (see Figure 3); DAC Gain = 0 dB).

Parameter (Note 4)		VA, VA_REF = 5.0 V VA_HP = 5.0 V (Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V VA_HP = 3.3 V (Single-ended) Min	Typ	Max	Unit
DAC1; R_L = 16 Ω; DAC Gain = -5 dB								
Dynamic Range								
18 to 24-Bit	A-weighted	95	101	-	93	99	-	dB
	unweighted	92	98	-	90	96	-	dB
16-Bit	A-weighted	-	93	-	-	93	-	dB
	unweighted	-	90	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-89	-83	-	-93	-87	dB
	-20 dB	-	-78	-72	-	-76	-70	dB
	-60 dB	-	-38	-32	-	-36	-30	dB
16-Bit	0 dB	-	-89	-	-	-90	-	dB
	-20 dB	-	-70	-	-	-70	-	dB
	-60 dB	-	-30	-	-	-30	-	dB
DAC1; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	100	106	-	98	104	-	dB
	unweighted	97	103	-	95	101	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-88	-82	-	-90	-84	dB
	-20 dB	-	-83	-77	-	-81	-75	dB
	-60 dB	-	-43	-37	-	-41	-35	dB
16-Bit	0 dB	-	-88	-	-	-90	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC1; R_L = 16 Ω or 10 kΩ								
Full-scale Output Voltage, R_L = 10 kΩ		0.80•VA	0.84•VA	0.88•VA	0.80•VA	0.84•VA	0.88•VA	Vpp
Output Power, THD+N = -75 dB, R_L = 16 Ω		-	38	-	-	17	-	mW_{rms}
Output Power, THD+N = 1%, R_L = 16 Ω		-	50	-	-	23	-	mW_{rms}
Output Power,THD+N = 10%, R_L = 16 Ω		-	74	-	-	35	-	mW_{rms}
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Output Offset Voltage	DAC to HPOUT	-	2	4	-	2	4	mV
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 7)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 7)	-	-	150	-	-	150	pF
Output Impedance		-	300	-	-	300	-	mΩ

Parameter (Note 4)		VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
DAC2/DAC3; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	104/100	110/106	-	101/97	107/103	-	dB
	unweighted	101/97	107/103	-	98/94	104/100	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-94/-91	-88/-85	-	-96/-94	-90/-88	dB
	-20 dB	-	-87/-83	-81/-77	-	-84/-80	-78/-74	dB
	-60 dB	-	-47/-43	-41/-37	-	-44/-40	-38/-34	dB
16-Bit	0 dB	-	-92	-	-	-92	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC2/DAC3; R_L = 10 kΩ								
Full-scale Output Voltage		1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 7)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 7)	-	-	100	-	-	100	pF
Output Impedance		-	100	-	-	100	-	Ω

7. See Figure 3 and Figure 4. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity.

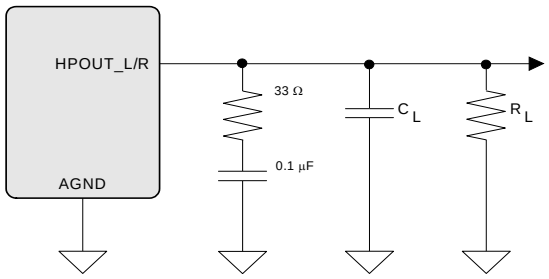


Figure 3. Output Test Load, Headphone Out

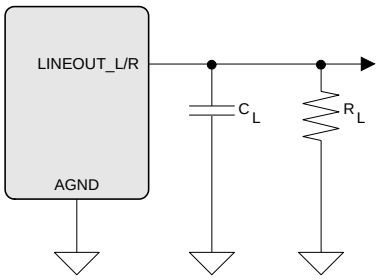


Figure 4. Output Test Load, Line Out

ANALOG OUTPUT CHARACTERISTICS (AUTOMOTIVE - DNZ)

(Test conditions (unless otherwise specified): Input test signal is a full-scale 997 Hz sine wave; VD = 1.8 V; VL_HD = VL_IF = 3.3V; T_A = -40 to +85°C; Measurement bandwidth is 10 Hz to 20 kHz; test load R_L = 10 kΩ, C_L = 10 pF for the line output and test load R_L = 16 Ω, C_L = 10 pF for the headphone output (see Figure 5); DAC Gain = 0 dB).

Parameter (Note 4)		VA, VA_REF = 5.0 V VA_HP = 5.0 V (Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V VA_HP = 3.3 V (Single-ended) Min	Typ	Max	Unit
DAC1; R_L = 16 Ω; DAC Gain = -5 dB								
Dynamic Range								
18 to 24-Bit	A-weighted	95	101	-	93	99	-	dB
	unweighted	92	98	-	90	96	-	dB
16-Bit	A-weighted	-	93	-	-	93	-	dB
	unweighted	-	90	-	-	90	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-89	-83	-	-93	-87	dB
	-20 dB	-	-78	-72	-	-76	-70	dB
	-60 dB	-	-38	-32	-	-36	-30	dB
16-Bit	0 dB	-	-89	-	-	-90	-	dB
	-20 dB	-	-70	-	-	-70	-	dB
	-60 dB	-	-30	-	-	-30	-	dB
DAC1; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	100	106	-	98	104	-	dB
	unweighted	97	103	-	95	101	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-88	-82	-	-90	-84	dB
	-20 dB	-	-83	-77	-	-81	-75	dB
	-60 dB	-	-43	-37	-	-41	-35	dB
16-Bit	0 dB	-	-88	-	-	-90	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC1; R_L = 16 Ω or 10 kΩ								
Full-scale Output Voltage, R_L = 10 kΩ		0.80•VA	0.84•VA	0.88•VA	0.80•VA	0.84•VA	0.88•VA	Vpp
Output Power, THD+N = -75 dB, R_L = 16 Ω		-	38	-	-	17	-	mW_{rms}
Output Power, THD+N = 1%, R_L = 16 Ω		-	50	-	-	23	-	mW_{rms}
Output Power,THD+N = 10%, R_L = 16 Ω		-	74	-	-	35	-	mW_{rms}
Interchannel Isolation (1 kHz)	16 Ω	-	80	-	-	80	-	dB
	10 kΩ	-	95	-	-	93	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Output Offset Voltage	DAC to HPOUT	-	2	5	-	2	5	mV
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 8)	16	-	-	16	-	-	Ω
Load Capacitance (C_L)	(Note 8)	-	-	150	-	-	150	pF
Output Impedance		-	300	-	-	300	-	mΩ

Parameter (Note 4)		VA, VA_REF = 5.0 V (Differential/Single-ended) Min	Typ	Max	VA, VA_REF = 3.3 V (Differential/Single-ended) Min	Typ	Max	Unit
DAC2/DAC3; R_L = 10 kΩ								
Dynamic Range								
18 to 24-Bit	A-weighted	104/100	110/106	-	101/97	107/103	-	dB
	unweighted	101/97	107/103	-	98/94	104/100	-	dB
16-Bit	A-weighted	-	96	-	-	96	-	dB
	unweighted	-	93	-	-	93	-	dB
Total Harmonic Distortion + Noise								
18 to 24-Bit	0 dB	-	-94/-91	-88/-85	-	-96/-94	-88/-88	dB
	-20 dB	-	-87/-83	-81/-77	-	-84/-80	-78/-74	dB
	-60 dB	-	-47/-43	-41/-37	-	-44/-40	-38/-34	dB
16-Bit	0 dB	-	-92	-	-	-92	-	dB
	-20 dB	-	-73	-	-	-73	-	dB
	-60 dB	-	-33	-	-	-33	-	dB
Other Characteristics for DAC2/DAC3; R_L = 10 kΩ								
Full-scale Output Voltage		1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	1.60•VA/ 0.80•VA	1.68•VA/ 0.84•VA	1.76•VA/ 0.88•VA	Vpp
Interchannel Isolation (1 kHz)		-	100	-	-	100	-	dB
Interchannel Gain Mismatch		-	0.1	0.25	-	0.1	0.25	dB
Gain Drift		-	±100	-	-	±100	-	ppm/°C
AC-Load Resistance (R_L)	(Note 8)	3	-	-	3	-	-	kΩ
Load Capacitance (C_L)	(Note 8)	-	-	100	-	-	100	pF
Output Impedance		-	100	-	-	100	-	Ω

8. See Figure 5 and Figure 6. R_L and C_L reflect the recommended minimum resistance and maximum capacitance required for the internal op-amp's stability and signal integrity.

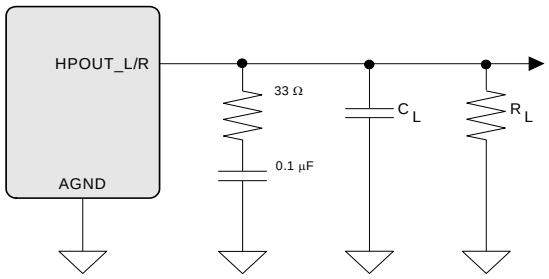


Figure 5. Output Test Load, Headphone Out

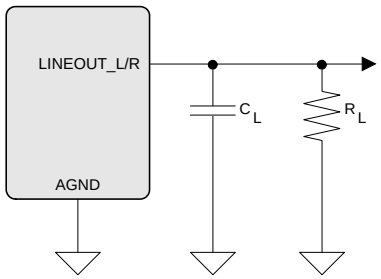


Figure 6. Output Test Load, Line Out

COMBINED DAC INTERPOLATION & ON-CHIP ANALOG FILTER RESPONSE

Parameter		Min	Typ	Max	Unit
Frequency Response 10 Hz to 20 kHz		-0.01	-	+0.01	dB
Passband	to -0.01 dB corner	0	-	21792	Hz
	to -3 dB corner	0	-	23952	Hz
StopBand		-	26256	-	Hz
StopBand Attenuation (Note 9)		-	102	-	dB
Total Group Delay		-	0.196	-	ms

9. Measurement Bandwidth is from Stopband to 100 kHz.

DC ELECTRICAL CHARACTERISTICS

(AGND = 0 V; all voltages with respect to ground.)

Parameters		Min	Typ	Max	Units
VCOM Characteristics					
Nominal Voltage		-	0.5•VA	-	V
Output Impedance		-	23	-	kΩ
DC Current Source/Sink (Note 10)		-	-	10	µA
VHP_FILT+ Characteristics					
Nominal Voltage		-	0.5•VA_HP	-	V
VHP_FILT- Characteristics					
Nominal Voltage		-	-0.5•VA_HP	-	V
MIC BIAS Characteristics					
Nominal Voltage	VREFE = 000b	-	Hi-Z	-	V
	VREFE = 001b	-	0.5•VA	-	V
	VREFE = 010b	-	GND	-	V
	VREFE = 100b	-	0.8•VA	-	V
DC Current Source	(VA=5.0V)	-	5	-	mA
	(VA=3.3V)	-	3	-	mA
Power Supply Rejection Ratio (PSRR) (Note 11)	1 kHz	-	60	-	dB

10. The DC current draw represents the allowed current draw from the VCOM pin due to typical leakage through electrolytic de-coupling capacitors.
11. Valid with the recommended capacitor values on VBIAS. Increasing the capacitance will also increase the PSRR.

DIGITAL MICROPHONE INTERFACE CHARACTERISTICS

Test conditions: Inputs: Logic 0 = GND = 0 V, Logic 1 = VL_IF; T_A = +25 °C; C_{LOAD} = 30 pF.

Parameters		Symbol	Min	Typ	Max	Units
DMIC_SCL Period (Fs_{ADC} >= 44.1 kHz)	(Note 12)	t_P	-	8 • T_cyc	-	ns
DMIC_SCL Period (Fs_{ADC} <= 32.0 kHz)	(Note 12)	t_P	-	12 • T_cyc	-	ns
DMIC_SCL Duty Cycle		-	45	-	55	%
DMIC_SCL Rise Time	(Note 13)	t_r	-	-	10	ns
DMIC_SCL Fall Time	(Note 13)	t_f	-	-	10	ns
DMIC_SDA Setup Time Before DMIC_SCL Rising Edge		$t_{s(SD-CLKR)}$	40	-	-	ns
DMIC_SDA Hold Time After DMIC_SCL Rising Edge		$t_{h(CLKR-SD)}$	5	-	-	ns
DMIC_SDA Setup Time Before DMIC_SCL Falling Edge		$t_{s(SD-CLKF)}$	40	-	-	ns
DMIC_SDA Hold Time After DMIC_SCL Falling Edge		$t_{h(CLKF-SD)}$	6	-	-	ns

Notes:

12. The output clock frequency will follow the Bit Clock (BITCLK) frequency divided by 8 or 12, depending on the sample rate of the ADC. Any deviation of the Bit Clock source from the nominal supported rates will be directly imparted to the output clock rate by the same factor (e.g. +100 ppm offset in the frequency of BIT-CLK will become a +100 ppm offset in DMIC_SCL). For the nominal value of T_cyc reference HDA024-A (see Note 4 in "References" on page 147).
13. Rise and fall times are measured from 0.1 • VL_IF to 0.9 • VL_IF.

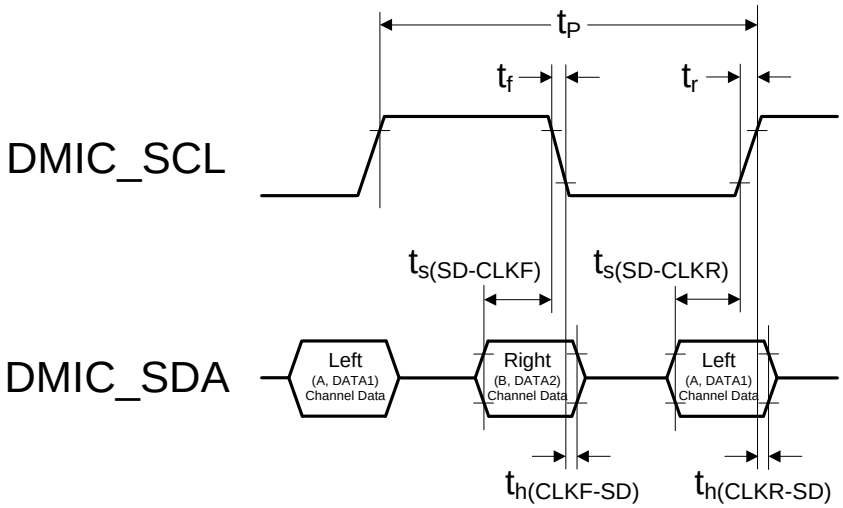


Figure 7. Digital MIC Interface Timing

DIGITAL INTERFACE SPECIFICATIONS & CHARACTERISTICS

Parameters (Note 14)	Symbol	Min	Max	Units
Input Leakage Current	I_{in}	-	±10	µA
Input Pin Capacitance	C_{in}	-	7.5	pF
VL_HD = 1.5 V				
High-Level Input Voltage	V_{IH}	0.60•VL_HD	-	V
Low-Level Input Voltage	V_{IL}	-	0.40•VL_HD	V
High-Level Output Voltage (I_{OUT} = -500 µA)	V_{OH}	0.90•VL_HD	-	V
Low-Level Output Voltage (I_{OUT} = 1500 µA)	V_{OL}	-	0.10•VL_HD	V
VL_HD = 3.3 V				
High-Level Input Voltage	V_{IH}	0.65•VL_HD	-	V
Low-Level Input Voltage	V_{IL}	-	0.35•VL_HD	V
High-Level Output Voltage (I_{OUT} = -500 µA)	V_{OH}	0.90•VL_HD	-	V
Low-Level Output Voltage (I_{OUT} = 1500 µA)	V_{OL}	-	0.10•VL_HD	V
VL_IF = 3.3 V				
High-Level Input Voltage	V_{IH}	0.65•VL_IF	-	V
Low-Level Input Voltage	V_{IL}	-	0.35•VL_IF	V
High-Level Output Voltage (I_{OH} = -100 µA)	V_{OH}	VL_IF - 0.2	-	V
Low-Level Output Voltage (I_{OL} = 100 µA)	V_{OL}	-	0.2	V

14. See "Digital I/O Pin Characteristics" on p 10 for HD Audio I/F and control power rails.

HD AUDIO BUS SPECIFICATIONS & CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
BITCLK Period	T_{CYC}	41.163	41.67	42.171	ns
BITCLK High Time	T_{HIGH}	17.50		24.16	ns
BITCLK Low Time	T_{LOW}	17.50		24.16	ns
BITCLK Jitter			150	500	ps
SDI Valid After BITCLK Rising	T_{TCO}	3		11	ns
SDO Setup Time	T_{SU}	5			ns
SDO Hold Time	T_H	5			ns

S/PDIF TRANSMITTER/RECEIVER SPECIFICATIONS & CHARACTERISTICS

Parameter	Symbol	Min	Typ	Max	Units
Transmitter Specifications & Characteristics					
AES3 Transmitter Output Jitter	$T_{JIT(rms)}$	meets IEC 60958-3			ps
Receiver Specifications & Characteristics					
PLL Clock Recovery Sample Rate Range	f_{rec}				kHz
Input Jitter Tolerance	$T_{JIT(rms)}$	meets IEC 60958-3			ps

POWER CONSUMPTION

(This table represents the power consumption for individual circuit blocks within the codec) (See (Note 15))

	Individual Block Operation	VA/ VA_HP	Typical Current (mA) i_{VA}	i_{VA_HP}	i_{VD} VD =1.8V	i_{VL_HD} VL_HD =3.3V	i_{VL_IF} VL_IF =3.3V	Total Power for individual block (mW)
1	Codec D3 State- unsolicited response capable (Note 16)	3.3	0.94	0.00	3.34	0.07	0.00	**9.35**
		5.0	1.20	0.00				**12.24**
2	ADC1 or ADC2 with PGA operation and Pseudo-Diff Inputs	3.3	5.47	0.00	7.27	0.17	0.00	**31.70**
		5.0	6.23	0.00				**44.80**
3	DAC1 with Headphone/Line Out (Note 17)	3.3	11.08	1.51	8.79	0.06	0.00	**57.57**
		5.0	14.06	1.76				**95.12**
4	DAC2 or DAC3 with Differential Line Out (Note 18)	3.3	10.72	0.00	8.72	0.06	0.00	**51.27**
		5.0	13.59	0.00				**83.84**
5	S/PDIF transmitter with SRC function	3.3	0.84	0.00	8.90	0.07	0.23	**19.78**
		5.0	1.10	0.00				**22.51**
6	S/PDIF receiver with SRC function	3.3	0.84	0.00	12.67	0.10	0.00	**25.91**
		5.0	1.10	0.00				**28.64**

15. Unless otherwise noted, test conditions are as follows: All zeros input, sample rate = 48 kHz; No load.
16. RESET# held HI, all HDA Bus clocks and data lines are running; HDA Interface running with support for unsolicited responses; All converters are in D3 state.
17. Full-scale single-ended output signal into a 10 kΩ load.
18. Full-scale differential output signal into a 10 kΩ load.

(The following table demonstrates the total power consumption for typical system operation. These total codec power numbers are derived from the individual block power consumption numbers in the previous table.)

	Typical Codec Operation	Power States ADC1	ADC2	DAC1	DAC2	DAC3	S/PDIF_OUT	S/PDIF_IN	VA/ VA_HP	Active Blocks	Total Codec Power (mW)
1	Stereo Record from Line In 1 (PGA/ADC1)	D0	D3	D3	D3	D3	D3	D3	3.3	HDA Interface + unsolicited response + ADC1	**41.04**
									5.0		**57.04**
2	Stereo Playback to Headphone (No Load)	D3	D3	D0	D3	D3	D3	D3	3.3	HDA Interface + unsolicited response + DAC1	**66.91**
									5.0		**107.36**
3	Stereo Playback to Headphone Out and S/PDIF Out	D3	D3	D0	D3	D3	D0	D3	3.3	HDA Interface + unsolicited response + DAC1+ S/PDIF OUT	**86.69**
									5.0		**129.87**
4	Receive from S/PDIF and Playback to S/PDIF Out	D3	D3	D3	D3	D3	D0	D0	3.3	HDA Interface + unsolicited response + S/PDIF IN/OUT	**55.04**
									5.0		**63.39**
5	Stereo Record & Playback Line In 1 / Line Out 1	D0	D3	D3	D0	D3	D3	D3	3.3	HDA Interface + unsolicited response + ADC1 + DAC2	**92.31**
									5.0		**140.88**

4. CODEC RESET AND INITIALIZATION

4.1 Link Reset

A Link Reset is a system controller generated assertion of the HD Audio Bus RESET# signal. A Link reset will cause some of the HD Audio bus interface logic to be initialized. Following a Link Reset, the CS4207 will perform the Codec Initialization request sequence. Many of the codec settings will remain unchanged following a Link Reset. See "Register Settings Across Reset Conditions" section on page 29 for more details.

When the codec has detected a Link Reset condition, all converter widgets and pin widgets will transition to a low power operating mode, if previously in D0. The actual power states reported will remain unchanged, i.e. if in D0 or D3 prior to Link Reset, the widget stays in D0 or D3. If enabled, presence detection will continue to sense any impedance changes and issue a power state change request to the Link prior to asserting an Unsolicited Response.

4.2 Function Group Reset

Because the CS4207 supports the Extended Power State Support (EPSS), a single occurrence of the **Function Group Reset** command will **NOT** cause the Audio Function unit and all associated widgets to initialize to the power-on reset values (as described in the HD Audio Specification, Rev. 1.0). When the CS4207 receives a single Function Group Reset verb, the codec will issue a response to the verb to acknowledge receipt, and reset each input/output converter widget's Stream Number and Lowest Channel Number to the default (0h). No other settings are modified. See "Register Settings Across Reset Conditions" section on page 29 for more details.

The CS4207 will respond to the newly created "Double Function Group Reset" (as defined in HDA015-B, March 1, 2007) and will reset most of the register settings to their power on defaults. This "Double Function Group Reset" will not affect the HD Audio bus interface logic or the unique codec physical address, which must be reset with the link RESET# signal. Therefore, the codec will not initiate a Codec Initialization sequence on the link. In addition, the Configuration Default settings will not be reset with a "Double Function Group Reset".

This new reset condition is created by sending two Function Group resets back to back. The "Double Function Group Reset" is defined as two (2) Function Group Reset verbs received without any other intervening verbs. The Function Group Reset verbs are not required to be received in sequential frames, but there must not be any other verbs received in frames between the receipt of the Function Group Reset verbs. There are no implied time outs between the time the first Function Group Reset is received and the second Function Group Reset verb.

4.3 Codec Initialization

Immediately following the completion of a Link Reset sequence, the CS4207 will initiate a codec initialization sequence. The purpose of this initialization sequence is to acquire a unique address by which the codec can thereafter be referenced with Commands on the SDO signal. During this sequence, the Controller provides the codec with a unique address using its attached SDI signal.

If the CS4207 codec is in a low power D3 state and enabled to support a presence detect event, it will retain its unique address while in that low power state. If RESET# is de-asserted high, and BITCLK and SYNC are running at the time of a presence detect event, the codec will signal an unsolicited response.

When put into the D3 low power state and enabled to support a presence detect event, with the link in the reset state (RESET# is asserted low), the CS4207 will post the occurrence of a wake event and request a power state change by signaling a power state change request and initialization request. It will reestablish the connection with the controller by performing a "Codec Initialization request".

If RESET# is asserted low, and BITCLK and SYNC are not running at the time (defined as link low power state), the codec will signal the power state change request and initialization request asynchronously by asserting SDI high continuously until it detects the de-assertion of RESET#. It will then asynchronously drive SDI low with the de-assertion of the RESET#. With the RESET# signal high, the codec will reestablish the connection with the controller by performing a “Codec Initialization request”.

4.4 D3 Lower Power State Support

The **D3** low power state allows for, but does not require, the lowest possible power consuming state under software control, in which Extended Power States Supported (EPSS) requirements can be met. While in the D3 state, the CS4207 will retain sufficient operational capability to properly respond to subsequent software Get/Set Power State commands (Verb ID=F05h/705h) to the Audio Function Group (Node ID = 01h). In addition, while in the D3 power state, Link Reset and “Double Function Group” reset are supported. All other Get/Set commands will be ignored while the codec is in the D3 power state.

Widgets reporting an EPSS of ‘1’b will transition from D3 state to D0 state in less than 10 ms. This interval is measured from the response to the Set Power State verb that caused the transition from D3 back to fully operational D0 state.

It is permissible for the audio fidelity for analog outputs to be slightly degraded if audio playback begins immediately once the fully operational state is entered. However, audio fidelity will not be degraded 75ms after the transitioning to D0 state.

4.5 Extended Power States Supported (EPSS)

EPSS indicates that the Audio Function Group or a particular Widget supports additional capabilities allowing better low power operation. The CS4207 will report EPSS support at the Function group level and will enable low power operation for all Input and Output Converter Widgets, and the following pin widgets which are capable of reporting presence detection:

- Headphone pin widget (node ID 09h)
- Line Out 1 pin widget (node ID 0Ah)
- Line In 1/Mic In 2 pin widget (node ID 0Ch)
- Mic In 1/Line In 2 pin widget (node ID 0Dh)
- S/PDIF Receiver Input pin widget (node ID 0Fh).

The following requirements will also be implemented by each input/output converter widget and the above listed pin widgets:

- Report PowerCntrl set to ‘1’b and support the Supported Power States verb.
- Jack Presence state change reporting (when enabled) will operate regardless of the Widget and Audio Function Group power state.
- Reporting of presence state change and issuing system wake when the link clock (BITCLK) is not operational is supported.
- The S/PDIF Receiver to S/PDIF Transmitter digital loop-through (no clock re-timing) will continue to operate (if enabled) even though any one, or all of the S/PDIF Receiver Input Converter Widget, S/PDIF Transmitter Output Converter Widget or S/PDIF Receiver Input Pin Widget enters into low power states. This digital loop-through will also continue to operate if the Audio Function Group is placed in the D3 low power state, during a Link Reset, and even if the HD Audio BITCLK is stopped.
- Dependencies between converter widgets and associated pin widgets will not cause unexpected results when one node of the dependency is placed into D3 state. The diagrams and tables below demonstrate typical audio streams.

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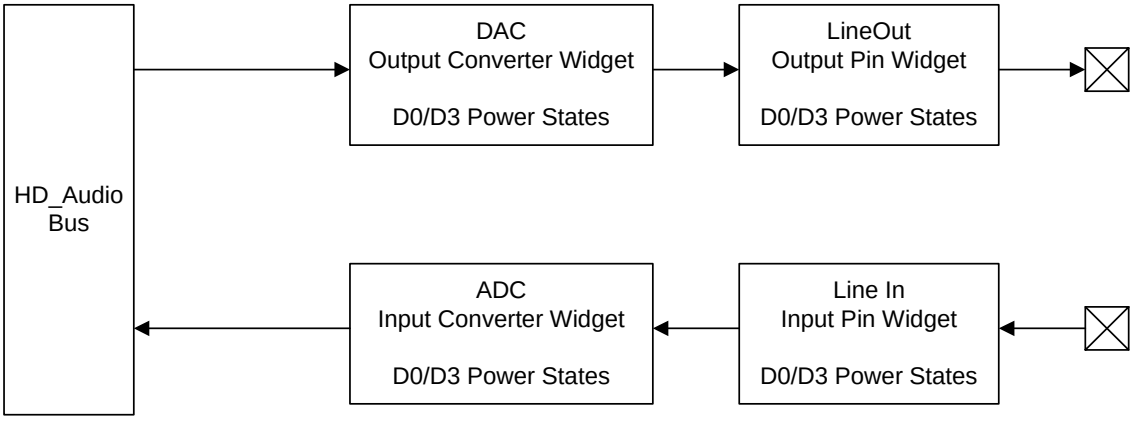


Output Path	Output Pin Widget D0	Output Pin Widget D3
Output Converter Widget D0	• Normal Operation in D0	• Converter widget continues to accept audio samples from the HD Audio bus. • Pin widget outputs a muted audio signal, supports presence detect if enabled and transitions to D3.
Output Converter Widget D3	• Converter widget stops accepting audio samples from the HD Audio bus, sends mute to the Pin widget and transitions to D3. • Pin widget outputs a muted audio signal and supports presence detect if enabled. Remains in D0 state.	• Converter and Pin Widgets are in low power D3 state. Supports presence detect if enabled.

Input Path	Input Pin Widget D0	Input Pin Widget D3
Input Converter Widget D0	• Normal Operation in D0	• Converter widget will send “muted” audio samples to the HD Audio bus. Remains in D0 state. • Pin widget outputs a muted audio signal, supports presence detect if enabled and transitions to D3.
Input Converter Widget D3	• Converter widget stops sending audio samples to the HD Audio bus and transitions to D3. • Pin widget shuts down and supports presence detect if enabled. Remains in D0 state.	• Converter and Pin Widgets are in low power D3 state. Supports presence detect if enabled.

4.6 Power State Settings Reset (PS-SettingsReset)

PS-SettingsReset is reported as set to one ‘1’b when, during any low power state transition the settings that were changed from the defaults (either through software or hardware) have been reset back to their default state. When these settings have not been reset, this is reported as ‘0’b. The conditions that may reset settings to their defaults are:

1. Power On; always sets the PS-SettingsReset to ‘1’b for all widgets that report EPSS set to ‘1’b and that have host programmable settings and reset all settings.
2. Double Function Group Reset: sets PS-SettingsReset to ‘1’b for all widgets that report EPSS set to one ‘1’b and that have host programmable settings and resets all settings.

Single Function Group Reset, Link Reset or BITCLK stopped will not cause the PS-SettingsReset bit to be set to ‘1’b. All settings will persist across these events.

The PS-SettingsReset will be reported at the individual widget level and at the Audio Function Group level. The PS-SettingsReset bit for the Audio Function Group is handled differently than at the widget level. For the Audio Function Group the PS-SettingsReset bit is set to ‘1’b when any widget sets its PS-SettingsReset to ‘1’b. The Audio Function Group’s PS-SettingsReset bit is the logical “or” of all the PS-SettingsReset bits, but is latched so that it can be reset independently and not require all the individual widget PS-SettingsReset bits be reset. This allows a simple poll by the host software to detect when some settings have been reset/changed. For widgets that do not support the EPSS bit, reporting PS-SettingsReset is not required.

If the PS-SettingsReset bit is set to ‘1’b, then this bit for individual widgets will be cleared to ‘0’b on receipt of any “Set” verb to that widget; or after responding to a “Get” Power State verb to that widget.

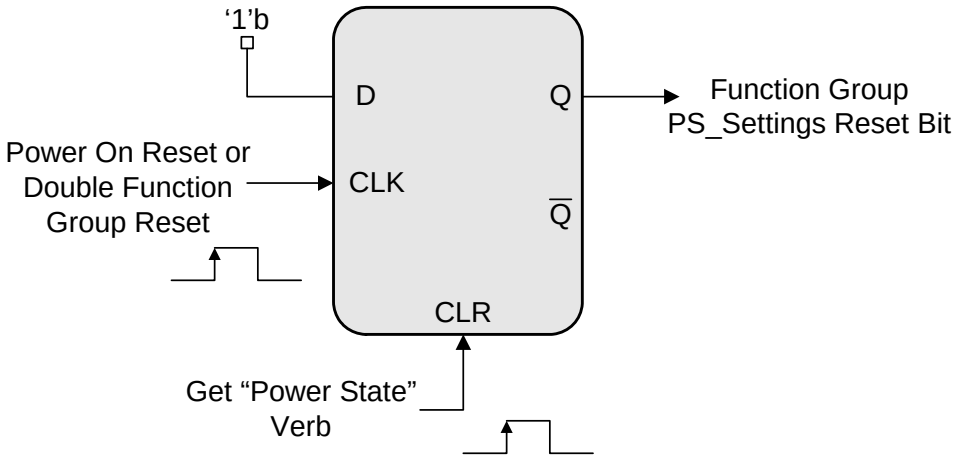


Figure 8. PS-Settings Reset Behavior

Bit settings within converters and pin widgets that software changed from their defaults will not be changed by hardware across any Dx state transition, single function group resets or link resets. Table 1 on page 29 outlines how the handling of setting persistence should be performed across Dx states, clock stopping and resets. Because the CS4207 supports EPSS, the use of PS-SettingsReset to report that settings have been reset (changed) is required.

4.7 Register Settings Across Resets

The CS4207 will perform a complete Power On Reset (POR) initialization if the voltage is cycled from off to on from the VD pin of the device. All registers will be initialized to the default state. For device behavior due to other system reset conditions or power state transitions events, see the table below.

Setting	Action with Link Reset	Action with "Double" Function Group reset	Action with "Single" Function Group reset	Action across D0/D3 state transitions or link BITCLK stopped
Unique codec physical address (SDI)	Requires codec initialization sequence to acquire new unique address.	Persist across "Double" FG reset.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Converter Format; Type, Base, Mult, Div, Bits Chan fields (verb ID = A00/2xx)	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Amplifier Gain/Mute (verb ID = Bxx/3xx)	Index, Mute and Gain settings persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Index, Mute and Gain settings persist across "Single" FG reset.	Index, Mute and Gain settings persist across Dx state transitions or BITCLK stopped.
Connection Select Control (verb ID = F01/701)	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Power States for the function group and individual widgets (verb ID = F05/705)	Power State persist across Link Reset.	Power State persist across "Double" FG reset.	Power State persist across "Single" FG reset.	Persist across BITCLK stopped. PS-Act and PS-Set will be updated to the current power state across Dx state transitions.
Converter Stream & Channel settings e.g. Stream number and lowest Channel number (verb ID = F06/706)	Reset to default by Link reset and does not set PS-SettingsReset to '1'b.	Reset to default by "Double" FG reset and does not set PS-SettingsReset to '1'b.	Reset to default by "Single" FG reset and does not set PS-SettingsReset to '1'b.	Reset to default across Dx state transitions and does not set PS-SettingsReset to '1'b.
Pin Widget Controls; In/Out Enables, Vref (verb ID = F07/707)	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Unsolicited Response control; Enable and Tag (verb ID = F08/708)	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.

Table 1. Register Settings Across Reset Conditions

Setting	Action with Link Reset	Action with "Double" Function Group reset	Action with "Single" Function Group reset	Action across D0/D3 state transitions or link BITCLK stopped
Pin Sense; Presence Detect Bit only. (verb ID = F09/709)	Update to reflect proper state and save any Unsolicited Response that has not been sent and send it after first verb is received.	Update to reflect proper state and issue an Unsolicited Response if enabled.	Update to reflect proper state and issue an Unsolicited Response if enabled.	Update to reflect proper state after transition back to full operation (D0).
EAPD/BTL enable; BTL (verb ID = F0C/70C)	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
S/PDIF Digital Converter Controls 1 & 2 (verb ID = F0D/70D-70E)	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
GPI/GPO Data, Enable Mask, Sticky Masks, Direction (verb ID = F15-F1A/715-71A)	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Configuration Default; all 32 bits (verb ID = F1C/71C-71F)	Persist across Link Reset.	Persist across "Double" FG reset.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Sub-System ID (verb ID = F20/720-723)	Persist across Link Reset.	Persist across "Double" FG reset.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Coefficient Index (verb ID = D/5)	Persist across Link Reset.	Settings are reset to POR default value.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Processing Coefficient (verb ID = C/4)	Persist across Link Reset.	Settings are reset to POR default value.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Coefficient Registers	Persist across Link Reset.	Settings are reset to POR default value. PS-SettingsReset set to '1'b.	Persist across "Single" FG reset.	Persist across Dx state transitions or BITCLK stopped.
Digital loop from S/PDIF Receiver pin widget to S/PDIF Transmitter pin widget	Digital Loop persists if enabled.	Digital Loop persists if enabled.	Digital Loop persists if enabled.	Digital Loop persists if enabled.

Table 1. Register Settings Across Reset Conditions

5. PRESENCE DETECTION

5.1 Jack Detection Circuit

The jack detection circuit provides attachment for to up to four pluggable jacks as described in the High Definition Audio Specification. Each jack has an isolated switch (normally open), as shown in Figure 9, which closes when a plug is inserted into that jack. A “power of two” parallel resistor network is connected to the SENSE_A pin as shown. The codec will measure the impedance of this network to determine which jacks have plugs inserted and set (or clear) the corresponding “Presence Detect” bit in the “Pin Sense” control for that Pin Widget. The jack detect circuitry will remove switch bounce of up to 250-ms duration.

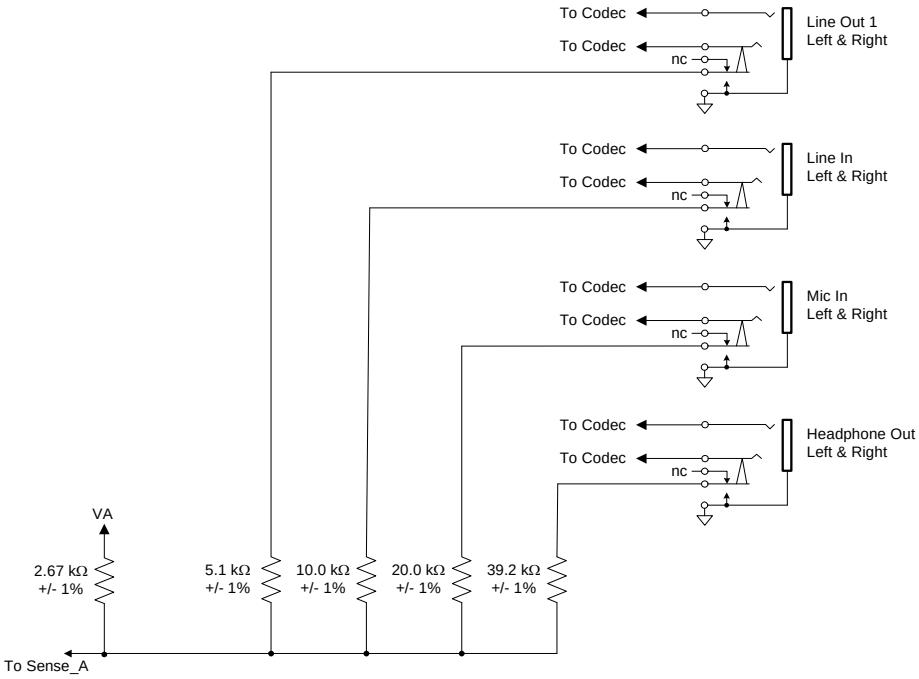


Figure 9. Jack Presence Detect Circuit

5.1.1 Presence Detection and Unsolicited Response

The Pin Widget, if enabled to generate an unsolicited response, will deliver one such response for each “de-bounced” state change of the “Presence Detect” bit. The “Presence Detect” bit will be stable and readable at the time an unsolicited response is issued. In sensing the insertion or removal of a jack the codec will measure the impedance continuously to determine when to report a change of state. Reporting of state change and change in the presence detect state bits will not occur until any impedance change has initially stabilized for approximately 250ms. Following this de-bounce period, the codec will report an unsolicited response, if enabled and the HD Audio BITCLK running, within 10ms. If the HD Audio BITCLK is not running, then the request to wake the Link will occur within 10ms.

Once an unplug or plug event has been signaled to the host via the unsolicited response, another change of the presence detection bits will not be generated unless the jack state has been sensed (de-bounced) continuously for at least 250ms.

Pin Widgets programmed to generate Unsolicited Responses for Presence Detection state changes will continue to function in all power states. When generating an Unsolicited Response for a plug event when the link is in a low power state (when RESET# is asserted low), sending of an Unsolicited Response will wait until after the power state change and initialization request and the codec initialization sequence are complete and the first verb is received to prevent the response from being lost due to software transition to active power state.

If the codec has detected that the link is entering a Link Reset state (see description below), all Unsolicited Response requests will be buffered. Once the link is in the Link Reset state, with RESET# asserted low, the codec will request a power state change and initialization request. Following the codec initialization cycle where a unique address is provided to the CS4207, the codec will then wait for the first verb to be received before issuing the Unsolicited Response to prevent the response from being lost due to software transition to active power state.

The Link Reset entry sequence is defined as follows:

1. The HD Audio Bus controller synchronously completes the current frame but does not signal Frame Sync (SYNC) during the last eight SDO bit times.
2. The HD Audio Bus controller synchronously asserts RESET# four (or more) BITCLK cycles after the completion of the current frame.
3. BITCLK is stopped a minimum of four clocks, four rising edges, after the assertion of RESET#.

In the event of a system bus (PCI Bus) reset, the above sequence does not complete, and RESET# is asynchronously asserted immediately and unconditionally.

When the codec returns to D0 from the D3 lower power state, the state of the presence detection bits will be correct. If the codec power has been removed, the state of the presence detection bits will be reset to the default value and the codec **WILL NOT** report this by setting the PS-SettingsReset bit for the affected Pin Widget(s). (HDA015-B, March 1, 2007 says that the PS-SettingsReset bit will be set for the affected Pin widget).

5.1.2 S/PDIF Receiver Presence Detect

The presence detect scheme for the S/PDIF Receiver will use the logic state transition of the “LOCK” or “UNLOCK” indicator for the incoming digital stream. The “LOCK” and “UNLOCK” indicators are sticky bits (edge-triggered) which indicate the current state of the receiver. These bits are located in the Vendor Processing Widget, see “S/PDIF RX/TX Interface Status (CIR = 0000h)” on p 129. When the S/PDIF Receiver Input Converter Widget is “enabled” and the “LOCK” indicator is a “1”, then the Presence Detect bit in the Pin Sense register will be set to ‘1’. The S/PDIF IN Converter Widget (NID=07h) and the S/PDIF Receiver pin widget (NID=0Fh) must be in the D0 state to support presence detect using this method described.

With an incoming valid S/PDIF signal applied to the SPDIF_IN pin, the “LOCK” status will be valid approximately 200 S/PDIF frames following the receiver being enabled.

6. HD AUDIO CODEC SUPPORTED VERBS AND RESPONSES

6.1 Software Programming Model

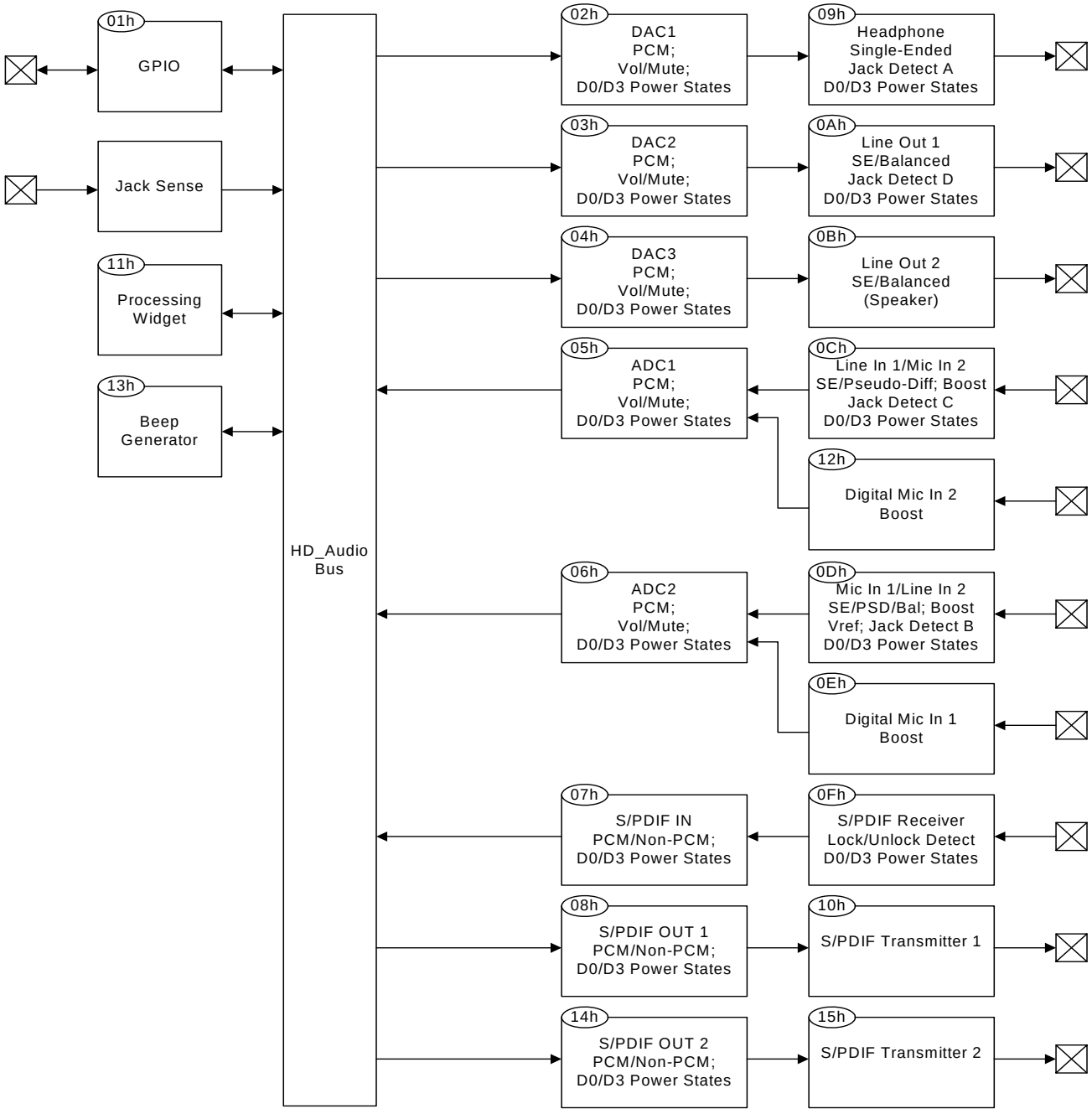


Figure 10. Software Programming Model

6.1.1 Node ID Summary

Node ID	Description	Reference Section
00h	Root Node	Section 6.2 on page 36
01h	Audio Function Group	Section 6.3 on page 37
02h	DAC1 Output Converter Widget	Section 6.4 on page 45
03h	DAC2 Output Converter Widget	Section 6.4 on page 45
04h	DAC3 Output Converter Widget	Section 6.4 on page 45
05h	ADC1 Input Converter Widget	Section 6.5 on page 53
06h	ADC2 Input Converter Widget	Section 6.5 on page 53
07h	S/PDIF Receiver Input Converter Widget	Section 6.6 on page 63
08h	S/PDIF Transmitter 1 Output Converter Widget	Section 6.7 on page 70
09h	Headphone Pin Widget	Section 6.8 on page 78
0Ah	Line Out 1 Pin Widget	Section 6.9 on page 85
0Bh	Line Out 2 Pin Widget	Section 6.10 on page 92
0Ch	Line In 1/Mic In 2 Pin Widget	Section 6.11 on page 97
0Dh	Mic In 1/Line In 2 Pin Widget	Section 6.11 on page 97
0Eh	Digital Mic 1 In Pin Widget	Section 6.12 on page 108
0Fh	S/PDIF Receiver Input Pin Widget	Section 6.13 on page 114
10h	S/PDIF Transmitter 1 Output Pin Widget	Section 6.14 on page 120
11h	Processing Widget	Section 6.15 on page 126
12h	Digital Mic 2 In Pin Widget	Section 6.12 on page 108
13h	Beep Generator Widget	Section 6.16 on page 136
14h	S/PDIF Transmitter 2 Output Converter Widget	Section 6.7 on page 70
15h	S/PDIF Transmitter 2 Output Pin Widget	Section 6.14 on page 120

Table 2. Device Node ID Summary

6.1.2 Pin Configuration Register Defaults

The Configuration Default Register is required for each Pin Widget. It is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values, see Table 3, indicating the typical system use of this particular pin/jack. After this initial loading, the state, including any software writes into the register, will be preserved across reset events. Its state need not be preserved across power level changes.

	Port	Location	Device	Type	Color	Misc	Assoc.	Sequence
Headphone Node ID = 09h (see p 83)	Jack	External/ Front	Headphone	1/8” Jack	Green	No PDC Override	F	0
Line Out 1 Node ID = 0Ah (see p 91)	Jack	External/ Rear	Line Out	1/8” Jack	Green	No PDC Override	F	0
Line Out 2 Node ID = 0Bh (see p 96)	Fixed	Internal	Speakers	Other Analog	Unknown	No PDC Override	F	0
Line In 1/Mic In 2 Node ID = 0Ch (see p 104)	Jack	External/ Rear	Line In	1/8” Jack	Blue	No PDC Override	5	1
Mic In 1/Line In 2 Node ID = 0Dh (see p 105)	Jack	External/ Rear	Mic In	1/8” Jack	Pink	No PDC Override	3	1
Digital Mic In 1 Node ID = 0Eh (see p 110)	Fixed	Other/ Mobile Lid Inside	Digital In	Other Digital	Unknown	No PDC Override	3	E
S/PDIF In Node ID = 0Fh (see p 119)	Jack	External/ Front	S/PDIF In	RCA Jack	White	No PDC Override	F	0
S/PDIF Out 1 Node ID = 10h (see p 124)	Jack	External/ Rear	S/PDIF Out	RCA Jack	Orange	No PDC Override	F	0
Digital Mic In 2 Node ID = 12h (see p 111)	Fixed	Other/ Mobile Lid Inside	Digital In	Other Digital	Unknown	No PDC Override	5	E
S/PDIF Out 2 Node ID = 15h (see p 125)	Jack	External/ Rear	S/PDIF Out	Optical Jack	Black	No PDC Override	F	0

Table 3. Pin Configuration Register Defaults

6.2 Root Node (Node ID = 00h)

6.2.1 Vendor and Device ID

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 00h	Verb ID = F00h	Parameter ID = 00h

Response Format:

Bits	Type	Default	Description
31:16	Read Only	1013h	**Vendor ID (VID):** Cirrus Logic PCI Vendor ID
15:0	Read Only	4207h	**Device ID (DID):** CS4207 Device ID

6.2.2 Revision ID

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 00h	Verb ID = F00h	Parameter ID = 02h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	1h	**Major Revision (MAJREV)** of the HDA Spec
19:16	Read Only	0h	**Minor Revision (MINREV)** of the HDA Spec
15:8	Read Only	03h	**Revision ID (REVID):** This indicates the letter rev used for all-layer changes. 01h - rev. Ax 02h - rev. Bx 03h - rev. Cx
7:0	Read Only	02h	**Stepping ID (SID):** This indicates the number rev used for metal layer changes. 00h - rev. A0 or rev. B0 or rev. C0 01h - rev. A1 or rev. C1 02h - rev. C2

6.2.3 Subordinate Node Count

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 00h	Verb ID = F00h	Parameter ID = 04h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:16	Read Only	01h	**Starting Node Number (SNN):** 1
15:8	Read Only	00h	Reserved
7:0	Read Only	01h	**Total Number of Nodes (TNN):** 1

6.3 Audio Function Group (Node ID = 01h)

6.3.1 Subordinate Node Count

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F00h	Parameter ID = 04h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:16	Read Only	02h	**Starting Node Number (SNN):** 2
15:8	Read Only	00h	Reserved
7:0	Read Only	14h	**Total Number of Nodes (TNN):** 20

6.3.2 Function Group Type

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F00h	Parameter ID = 05h

Response Format:

Bits	Type	Default	Description
31:9	Read Only	0	Reserved
8	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
7:0	Read Only	01h	**Node Type (NT):** Audio Function Group

6.3.3 Audio Function Group Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F00h	Parameter ID = 08h

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	1b	**Beep Gen:** Beep Generator is present.
15:12	Read Only	0h	Reserved
11:8	Read Only	9h	**Input Delay:** represents the number of samples between when the sample is received as an analog signal at the pin and when the digital representation is transmitted on the High Definition Audio Link. This may be a “typical” value.
7:4	Read Only	0h	Reserved
3:0	Read Only	Eh	**Output Delay:** represents the number of samples between when the sample is received from the Link and when it appears as an analog signal at the pin. This may be a “typical” value.

6.3.4 Supported PCM Size, Rates

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F00h	Parameter ID = 0Ah

Response Format:

Bits	Type	Default	Description
31:21	Read Only	00000000000b	Reserved
20	Read Only	1b	**32-Bit (32B):** 32-bit audio format is supported.
19	Read Only	1b	**24-Bit (24B):** 24-bit audio format is supported.
18	Read Only	1b	**20-Bit (20B):** 20-bit audio format is supported.
17	Read Only	1b	**16-Bit (16B):** 16-bit audio format is supported.
16	Read Only	0b	**8-Bit (8B):** 8-bit audio format is not supported.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**Rate-12 (R12):** 384 kHz (48*8) rate is not supported.
10	Read Only	1b	**Rate-11 (R11):** 192.0 kHz (48*4) rate is supported.
9	Read Only	1b	**Rate-10 (R10):** 176.4 kHz (44.1*4) rate is supported.
8	Read Only	1b	**Rate-9 (R9):** 96.0 kHz (48*2) rate is supported.
7	Read Only	1b	**Rate-8 (R8):** 88.2 kHz (44.1*2) rate is supported.
6	Read Only	1b	**Rate-7 (R7):** 48.0 kHz rate is supported.
5	Read Only	1b	**Rate-6 (R6):** 44.1 kHz rate is supported.
4	Read Only	1b	**Rate-5 (R5):** 32.0 kHz (48*2/3) rate is supported.
3	Read Only	0b	**Rate-4 (R4):** 22.05 kHz (44.1/2) rate is not supported.
2	Read Only	0b	**Rate-3 (R3):** 16.0 kHz (48/3) rate is not supported
1	Read Only	0b	**Rate-2 (R2):** 11.025 kHz (44.1/4) rate is not supported.
0	Read Only	0b	**Rate-1 (R1):** 8.0 kHz (48/6) rate is not supported.

6.3.5 Supported Stream Formats

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F00h	Parameter ID = 0Bh

Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	0b	**AC-3 (AC3):** AC-3™ data is not supported.
1	Read Only	0b	**Float32 (FLT32):** Float32 formatted data is not supported on this widget.
0	Read Only	1b	**Pulse Code Modulation (PCM):** PCM formatted data is supported on this widget.

6.3.6 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Function Group supports extended power states.
30	Read Only	1b	**CLKSTOP:** Function group supports D3 operation even if there is no BCLK present on the link.
29	Read Only	0b	**S3D3coldSup:** Software should place the codec in D3hot state when the platform is entering S3 state.
28:5	Read Only	000000h	Reserved
4	Read Only	0b	**D3coldSup:** D3cold operation is not supported.
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

CLKSTOP is defined only at the Function Group only (not at the widget level) and indicates that the Function Group and all widgets under it support D3 operation even when there is no BITCLK present on the Link. The maximum exit time back to fully functional is 10 milliseconds from the time that the clock begins operation and a codec address cycle has been completed. The CLKSTOP capability extends the required functionality for D3 support while the link is operational to include:

- Reporting of presence detect state changes, if enabled and supported by the pin widget, even if the Link Clock is not running (controller low power state) or is currently in a Link Reset condition.
- Presence state changes occurring during Link Reset will be deferred until after the reset sequence has completed. Presence state change Unsolicited Responses, if enabled, will not be lost because the Link Clock stops or if Link Resets are generated before the Unsolicited Response for the state change has been returned to the host.

- Reporting of ClkStopOk when stopping of the clock would be permitted. The CLKSTOP is a static capability with ClkStopOk a dynamic reporting. The setting the capability CLKSTOP to one (1) and not allowing the clock to stop by not reporting ClkStopOk is not permissible. Unless there is a condition or dependency that the host software cannot be made aware of, that would prohibit stopping the clock, the ClkStopOk shall be reported as set (1). It is expected that host software will poll the ClkStopOk before stopping the clock if the CLKSTOP is reported at one (1).

6.3.7 GPIO Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F00h	Parameter ID = 11h

Response Format:

Bits	Type	Default	Description
31	Read Only	0b	**GPIOWake:** Does not support wake functionality.
30	Read Only	0b	**GPIOUnsol:** Does not support UR functionality.
29:24	Read Only	0h	Reserved
23:16	Read Only	0h	**NumGPIs:** No dedicated GPI pins.
15:8	Read Only	0h	**NumGPOs:** No dedicated GPO pins.
7:0	Read Only	4h	**NumGPIOs:** AFG supports 4 GPIO pins.

6.3.8 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to '1'b when, during any type of reset or low power state transition, the settings that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as '0'b. This bit is always a '1'b following a POR condition. For more information, see "Power State Settings Reset (PS-SettingsReset)" on p 28.
9	Read Only	1b	**Power State Clock Stop OK (PS-ClkStopOK):** This bit is set to a '1'b when the codec is capable of continuing proper operation even when the HD Audio Bus BITCLK has been stopped. This bit is valid for the Audio Function Group node and not the device widgets.
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return '0'b when read. The power state requested by software will always be possible following a reasonable time required to execute the power state transition. There are no dependencies unknown to software between nodes that would inhibit transitioning to the requested power state.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = '0000'b; D0 - Fully on. PSS = '0001'b; D1 - Not Supported PSS = '0010'b; D2 - Not Supported PSS = '0011'b; D3 - Allows for lowest possible power consumption under software control. See "D3 Lower Power State Support" on page 26 for more information. PSS = '0100'b; D4 - Not Supported

PS-Set is a Power State field which defines the current power setting of the referenced node. Since this node is an Audio Function Group node, the actual power state is this setting. Setting this field to the D3

state for the Audio Function Group node will force all other nodes with power state control to the D3 state. If the Power State field for this node is set to D0, then the individual power state for each converter will be uniquely controlled via the corresponding node Power State field.

PS-Act is a Power State field which indicates the actual power state of the referenced node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition).

PS-ClkStopOk is reported as a '1'b when the codec is capable of continuing proper operation in the absence of the HD Audio Bus BITCLK. This bit is reported only at the Audio Function Group level and is reserved at the widget level. After accepting a low power state transition request (D3 state) to the Audio Function Group Node, the codec will begin ramping down all the audio converters. During this time, the PS-ClkStopOK bit will be set to '0'b to signify that the bus BITCLK can not be stopped. Once all the converters have been ramped down, the codec will update the PS-Act bits to reflect the actual transition to the D3 state and will then set the PS-ClkStopOk bit to a '1'b to report the ability of the codec to operate correctly while in the low power state with the BITCLK stopped. While in the low power D3 state, and with the bus BITCLK stopped, the pin widgets of the codec which were enabled to support unsolicited responses will continue to operate.

6.3.9 GPIO Data

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F15h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = 715h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read Only	0h	**GPIO[7:4] Data:** Not Supported.
3:0	Read/Write	0h	**GPIO[3:0] Data:** For GPIO programmed as inputs, this value is read only and is the sensed value on the corresponding pin. For GPIO programmed as outputs, the value written is driven onto the corresponding pin. Note that if the corresponding bit in the GPIO Enable Mask control is not set, pins configured as outputs will not drive the associated bit value (as the pin must be in a Hi-Z state), but the value returned on a read will still reflect the value that would be driven if the pin were to be enabled in the GPIO Enable Mask control.

6.3.10 GPIO Enable Mask

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F16h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = 716h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read Only	0h	**GPIO[7:4] Enable Mask:** Not Supported.
3:0	Read/Write	0h	**GPIO[3:0] Enable Mask:** If the bit associated with a pin is 0, the pin is disabled, and must be in a Hi-Z state. If the bit is a 1, the GPIO pin is enabled and the pin's behavior will be determined by the GPIO Direction control.

6.3.11 GPIO Direction

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F17h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = 717h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read Only	0h	**GPIO[7:4] Direction:** Not Supported.
3:0	Read/Write	0h	**GPIO[3:0] Direction:** If a bit is a 0, the associated GPIO signal is configured as an input. If the bit is set to a 1, the associated GPIO signal is configured as an output.

6.3.12 GPIO Sticky Mask

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F1Ah	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = 71Ah	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read Only	0h	**GPIO[7:4] Sticky Mask:** Not Supported.
3:0	Read/Write	0h	**GPIO[3:0] Sticky Mask:** Defines GPIO Input Type (0 = Non-Sticky, 1 = Sticky) when a GPIO pin is configured as an input. GPIO inputs configured as Sticky are cleared by writing a 0 to the corresponding bit of the GPIO Data Control The default value for these bits (0h) is all pins Non-Sticky. Non implemented GPIO pins always return 0's. Sticky is defined as Positive-Edge sensitive, Non-Sticky as Level sensitive.

6.3.13 Implementation Identification

This field provides the Board Implementation ID and Assembly ID of the functional group to software. It is a Read/Write-Once register; BIOS writes to this field to configure the Board Implementation ID and Assembly ID during the boot process.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = F20h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = 720h	Payload = xxh (IID bits [7:0])
CAd = X	Node ID = 01h	Verb ID = 721h	Payload = xxh (IID bits [15:8])
CAd = X	Node ID = 01h	Verb ID = 722h	Payload = xxh (IID bits [23:16])
CAd = X	Node ID = 01h	Verb ID = 723h	Payload = xxh (IID bits [31:24])

Response Format:

Bits	Type	Default	Description
31:16	Read/Write Once	1013h	**Board Manufacturer Identification (BMID):** Contains the PCI Vendor ID of the board manufacturer. Preset to Cirrus Logic's PCI Vendor ID.
15:8	Read/Write Once	42h	**Board SKU (BSKU):** Assigned by the board manufacturer to identify the specific board design. Preset to 42h for Cirrus Logic codecs.
7:0	Read/Write Once	07h	**Assembly ID (AssyID):** Uniquely identifies the specific board assembly. Preset to 07h for the CS4207.

6.3.14 Function Reset

Function Reset is an "Execute" verb. There is no physical register associated with the Function Reset. See "Function Group Reset" section on page 25 for more details.

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 01h	Verb ID = 7FFh	Payload = 00h

6.4 DAC1, DAC2, DAC3 Output Converter Widgets (Node ID = 02h, 03h, 04h)

6.4.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	0h	**Type (TYP):** Audio Output Converter Widget
19:16	Read Only	Dh	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	0b	**Connection List (CL):** A connection list is not present on this widget.
7	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	1b	**Format Override (FO):** This bit is a ‘1’ to indicate that the widget contains format information, and the “Supported Formats” and “Supported PCM Bits, Rates” should be queried for the widget’s format capabilities.
3	Read Only	1b	**Amplifier Parameter Override (APO):** This widget contains its own amplifier parameters.
2	Read Only	1b	**Output Amplifier Present (OAP):** Output amplifier is present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.4.2 Supported PCM Size, Rates

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = F00h	Parameter ID = 0Ah

Response Format:

Bits	Type	Default	Description
31:21	Read Only	00000000000b	Reserved
20	Read Only	1b	**32-Bit (32B):** 32-bit audio format is supported.
19	Read Only	1b	**24-Bit (24B):** 24-bit audio format is supported.
18	Read Only	1b	**20-Bit (20B):** 20-bit audio format is supported.
17	Read Only	1b	**16-Bit (16B):** 16-bit audio format is supported.
16	Read Only	0b	**8-Bit (8B):** 8-bit audio format is not supported.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**Rate-12 (R12):** 384 kHz (48*8) rate is not supported.
10	Read Only	1b	**Rate-11 (R11):** 192.0 kHz (48*4) rate is supported.
9	Read Only	1b	**Rate-10 (R10):** 176.4 kHz (44.1*4) rate is supported.
8	Read Only	1b	**Rate-9 (R9):** 96.0 kHz (48*2) rate is supported.
7	Read Only	1b	**Rate-8 (R8):** 88.2 kHz (44.1*2) rate is supported.
6	Read Only	1b	**Rate-7 (R7):** 48.0 kHz rate is supported.
5	Read Only	1b	**Rate-6 (R6):** 44.1 kHz rate is supported.
4	Read Only	1b	**Rate-5 (R5):** 32.0 kHz (48*2/3) rate is supported.
3	Read Only	0b	**Rate-4 (R4):** 22.05 kHz (44.1/2) rate is not supported.
2	Read Only	0b	**Rate-3 (R3):** 16.0 kHz (48/3) rate is not supported
1	Read Only	0b	**Rate-2 (R2):** 11.025 kHz (44.1/4) rate is not supported.
0	Read Only	0b	**Rate-1 (R1):** 8.0 kHz (48/6) rate is not supported.

6.4.3 Supported Stream Formats

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = F00h	Parameter ID = 0Bh

Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	0b	**AC-3 (AC3):** AC-3 data is not supported.
1	Read Only	0b	**Float32 (FLT32):** Float32 formatted data is not supported on this widget.
0	Read Only	1b	**Pulse Code Modulation (PCM):** PCM formatted data is supported on this widget.

6.4.4 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.4.5 Output Amplifier Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = F00h	Parameter ID = 12h

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**Mute Capable (MC):** This widget supports mute.
30:23	Read Only	00000000b	Reserved
22:16	Read Only	0000001b	**Step Size (SS):** Indicates that the size of each amplifier's step gain is 0.5 dB.
15	Read Only	0b	Reserved
14:8	Read Only	1111111b	**Number of Steps (NOS):** Indicates there are 128 gain steps; Attenuation range is from +6 dB to -57.5 dB in 0.5 dB steps.
7	Read Only	0b	Reserved
6:0	Read Only	1110011b	**Offset (OFST):** Indicates that if "1110011b" is programmed into the Amplified Gain Control, it would result in a gain of 0 dB.

6.4.6 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to ‘1’b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as ‘0’b. This bit is always a ‘1’b following a POR condition. For more information, see Section 4.6
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return ‘0’b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = ’0000’b; D0 - Fully on. PSS = ‘0001’b; D1 - Not Supported PSS = ‘0010’b; D2 - Not Supported PSS = ‘0011’b; D3 - Allows for lowest possible power consumption under software control. See Section 4.4 for more information. PSS = ‘0100’b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.4.7 Converter Stream, Channel

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = F06h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = 706h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read/Write	0h	**Stream Number (SN):** This field is written by software to indicate the stream number used by the Output Converter. “0h” is stream 0, “1h” is stream 1, etc. By convention, stream 0 is reserved and unused so that converter whose stream number has been reset to “0h” does not unintentionally decode data not intended for them.
3:0	Read/Write	0h	**Lowest Channel Number (LCN):** This field is written by software to indicate the lowest channel used by the Output Converter. The stereo converter will use this LCN value plus 1 for its left and right channel.

6.4.8 Converter Format

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = Ah	Payload = 0000h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = 2h	Payload = xxxxh

Response Format:

Bits [15:0] must be programmed with the same value programmed into the Stream Descriptor, so that the data format being transmitted on the link matches what is expected by the consumer of the data.

If the TYPE is set to Non-PCM, the controller pushes data over the link and is not concerned with formatting. The base rate, data type, and number of Words (MULT) to send each valid frame are specified to control the rate at which the non-PCM data is sent.

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15	Read/Write	0b	**Stream Type (TYPE):** If TYPE is non-zero, the other bits in the format structure have other meanings. 0: PCM 1: Non-PCM
14	Read/Write	0b	**Sample Base Rate (BASE):** 0 = 48 kHz 1 = 44.1 kHz
13:11	Read/Write	000b	**Sample Base Rate Multiple (MULT):** 000 = 48 kHz/44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) 100-111 = *Reserved*
10:8	Read/Write	000b	**Sample Base Rate Divisor (DIV):** 000 = Divide by 1 (48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	Read Only	0b	Reserved
6:4	Read/Write	000b	**Bits per Sample (BITS):** Bits in each sample: 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 101-111 = *Reserved*
3:0	Read/Write	0000b	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000 = 1 0001 = 2 … 1111 = 16

6.4.9 Amplifier Gain/Mute

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = Bh	Payload = xxxxh

Bits [19:16] = 'Bh', where bits [15:0] are defined below:

Bits [15:0]	Value	Description
15	1b	**Get Output/Input (GOI):** This bit controls whether the request is for the input amplifier or the output amplifier. When '1', the output amplifier is being requested. When '0', the input amplifier is being requested.
14	0b	'0'b
13	xb	**Get Left/Right (GLR):** This bit controls whether the request is for the left channel amplifier or the right channel amplifier. When '1', the left channel amplifier is being requested. When '0', the right channel amplifier is being requested.
12:4	000000000b	Reserved
3:0	0000b	**Index (IDX):** This field specifies the input index of the amplifier setting to return if the widget has multiple input amplifiers. It is only applicable if "Get Output/Input" is '0' which indicates input amplifier is being requested. This field has no meaning and ignored since the widget does not have multiple input amplifiers. It should be always '0's.

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	1b	**Amplifier Mute (AM):** This bit returns the Mute setting for the amplifier requested. A 1 indicates the amplifier is in the Mute condition. If the amplifier requested does not exist, a '0' will be returned. Default equals Muted.
6:0	Read Only	1110011b	**Amplifier Gain (AG):** This field returns the Gain setting for the amplifier requested. If the amplifier requested does not exist, all '0's will be returned Default equals 0 dB.

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DAC1 Node ID=02h DAC2 Node ID=03h DAC3 Node ID=04h	Verb ID = 3h	Payload = xxxxh

Bits [19:16] = ‘3h’, where bits [15:0] are defined below:

Bits	Type	Default	Description
15	Write Only	xb	**Set Output Amplifier (SOA):** Determines if the value programmed refers to the output amplifier. Set to a 1 for the value to be accepted.
14	Write Only	0b	**Set Input Amplifier (SIA):** Determines if the value programmed refers to the input amplifier. This bit should always be ‘0’ since an input amplifier is not present on this widget.
13	Write Only	xb	**Set Left Amplifier (SLA):** Selects the left channel (channel 0). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
12	Write Only	xb	**Set Right Amplifier (SRA):** Selects the right channel (channel 1). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
11:8	Write Only	0000b	**Index (IDX):** This field is used when programming the input amplifiers on Selector Widgets and Sum Widgets. This field is ignored.
7	Write Only	xb	**Mute (MUTE):** When ‘1’, the Mute is active. When ‘0’, the Mute is inactive.
6:0	Write Only	xxxxxxxb	**Gain (GAIN):** Specifies the amplifier gain in dB.

6.5 ADC1, ADC2 Input Converter Widgets (Node ID = 05h, 06h)

6.5.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	1h	**Type (TYP):** Audio Input Converter Widget
19:16	Read Only	8h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	1b	**Connection List (CL):** A connection list is present on this widget.
7	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	1b	**Format Override (FO):** This bit is a ‘1’ to indicate that the widget contains format information, and the “Supported Formats” and “Supported PCM Bits, Rates” should be queried for the widget’s format capabilities.
3	Read Only	1b	**Amplifier Parameter Override (APO):** This widget contains its own amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Is ‘0’ as it is irrelevant to this Audio Input Converter widget.
1	Read Only	1b	**Input Amplifier Present (IAP):** Input amplifier is present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.5.2 Supported PCM Size, Rates

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F00h	Parameter ID = 0Ah

Response Format:

Bits	Type	Default	Description
31:21	Read Only	00000000000b	Reserved
20	Read Only	1b	**32-Bit (32B):** 32-bit audio format is supported.
19	Read Only	1b	**24-Bit (24B):** 24-bit audio format is supported.
18	Read Only	1b	**20-Bit (20B):** 20-bit audio format is supported.
17	Read Only	1b	**16-Bit (16B):** 16-bit audio format is supported.
16	Read Only	0b	**8-Bit (8B):** 8-bit audio format is not supported.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**Rate-12 (R12):** 384 kHz (48*8) rate is not supported.
10	Read Only	0b	**Rate-11 (R11):** 192.0 kHz (48*4) rate is not supported.
9	Read Only	0b	**Rate-10 (R10):** 176.4 kHz (44.1*4) rate is not supported.
8	Read Only	1b	**Rate-9 (R9):** 96.0 kHz (48*2) rate is supported.
7	Read Only	1b	**Rate-8 (R8):** 88.2 kHz (44.1*2) rate is supported.
6	Read Only	1b	**Rate-7 (R7):** 48.0 kHz rate is supported.
5	Read Only	1b	**Rate-6 (R6):** 44.1 kHz rate is supported.
4	Read Only	1b	**Rate-5 (R5):** 32.0 kHz (48*2/3) rate is supported.
3	Read Only	0b	**Rate-4 (R4):** 22.05 kHz (44.1/2) rate is not supported.
2	Read Only	1b	**Rate-3 (R3):** 16.0 kHz (48/3) rate is supported
1	Read Only	0b	**Rate-2 (R2):** 11.025 kHz (44.1/4) rate is not supported.
0	Read Only	1b	**Rate-1 (R1):** 8.0 kHz (48/6) rate is supported.

6.5.3 Supported Stream Formats

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F00h	Parameter ID = 0Bh

Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	0b	**AC-3 (AC3):** AC-3 data is not supported.
1	Read Only	0b	**Float32 (FLT32):** Float32 formatted data is not supported on this widget.
0	Read Only	1b	**Pulse Code Modulation (PCM):** PCM formatted data is supported on this widget.

6.5.4 Input Amplifier Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F00h	Parameter ID = 0Dh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**Mute Capable (MC):** Supports muting.
30:23	Read Only	00000000b	Reserved
22:16	Read Only	0000011b	**Step Size (SS):** Indicates that the size of each amplifier's step gain is 1.0 dB.
15	Read Only	0b	Reserved
14:8	Read Only	0111111b	**Number of Steps (NOS):** There are 64 gain steps; Gain range is from +12 dB to -51 dB in 1.0 dB steps. If analog input pin widget is selected as input source, then the range of +12 dB to -12 dB is from analog PGA and the range of -13 dB to -51 dB is digital volume control. If the digital mic input pin widget is selected as the input source, then the entire gain range from +12 dB to -51 dB is digital volume control.
7	Read Only	0b	Reserved
6:0	Read Only	0110011b	**Offset (OFST):** Indicates that if "0110011b" is programmed into the Amplified Gain Control, it would result in a gain of 0 dB.

6.5.5 Connection List Length

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F00h	Parameter ID = 0Eh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Long Form (LF):** Connection list is short form.
6:0	Read Only	0000010b	**Connection List Length (CLL):** Two selectable inputs are possible for this widget.

6.5.6 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.5.7 ADC1 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 05h	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	12h	**Connection List Entry (N+1):** Returns 12h (Digital Mic In 2) for N=00h-03h. Returns 00h for N>03h.
7:0	Read Only	0Ch	**Connection List Entry (N):** Returns 0Ch (Line In 1) for N=00h-03h. Returns 00h for N>03h.

6.5.8 ADC1 Connection Select Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 05h	Verb ID = F01h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 05h	Verb ID = 701h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:0	Read/Write	00h	**Connection Index Value:** For a Get command, this field specifies the current connection index. The field is written by software to indicate the connection index value to be set. 00h: Line In 1 (NID=0Ch) 01h: Digital Mic In 2 (NID=12h)

6.5.9 ADC2 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 06h	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	0Eh	**Connection List Entry (N+1):** Returns 0Eh (Digital Mic In 1) for N=00h-03h. Returns 00h for N>03h
7:0	Read Only	0Dh	**Connection List Entry (N):** Returns 0Dh (Mic In 1) for N=00h-03h. Returns 00h for N>03h.

6.5.10 ADC2 Connection Select Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 06h	Verb ID = F01h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 06h	Verb ID = 701h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:0	Read/Write	00h	**Connection Index Value:** For a Get command, this field specifies the current connection index. The field is written by software to indicate the connection index value to be set. 00h: Mic In 1 (NID=0Dh) 01h: Digital Mic In 1 (NID=0Eh)

6.5.11 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to '1'b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as '0'b. This bit is always a '1'b following a POR condition. For more information, see "Power State Settings Reset (PS-SettingsReset)" on p 28
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return '0'b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = '0000'b; D0 - Fully on. PSS = '0001'b; D1 - Not Supported PSS = '0010'b; D2 - Not Supported PSS = '0011'b; D3 - Allows for lowest possible power consumption under software control. See "D3 Lower Power State Support" on page 26 for more information. PSS = '0100'b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.5.12 Converter Stream, Channel

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = F06h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = 706h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read/Write	0h	**Stream Number (SN):** This field is written by software to indicate the stream number used by the Input Converter. “0h” is stream 0, “1h” is stream 1, etc. By convention, stream 0 is reserved and unused so that converter whose stream number has been reset to “0h” does not unintentionally decode data not intended for them.
3:0	Read/Write	0h	**Lowest Channel Number (LCN):** This field is written by software to indicate the lowest channel used by the Input Converter. The stereo converter will use this LCN value plus 1 for its left and right channel.

6.5.13 Converter Format

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = Ah	Payload = 0000h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = 2h	Payload = xxxxh

Response Format:

Bits [15:0] must be programmed by software with the same value programmed into the Stream Descriptor, so that the data format being transmitted on the link matches what is expected by the consumer of the data.

If the TYPE is set to Non-PCM, the controller pushes data over the link and is not concerned with formatting. The base rate, data type, and number of Words (MULT) to send each valid frame are specified to control the rate at which the non-PCM data is sent.

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15	Read/Write	0b	**Stream Type (TYPE):** If TYPE is non-zero, the other bits in the format structure have other meanings. 0: PCM 1: Non-PCM
14	Read/Write	0b	**Sample Base Rate (BASE):** 0 = 48 kHz 1 = 44.1 kHz
13:11	Read/Write	000b	**Sample Base Rate Multiple (MULT):** 000 = 48 kHz/44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) 100-111 = *Reserved*
10:8	Read/Write	000b	**Sample Base Rate Divisor (DIV):** 000 = Divide by 1 (48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	Read Only	0b	Reserved
6:4	Read/Write	000b	**Bits per Sample (BITS):** Number of bits in each sample: 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 101-111 = *Reserved*
3:0	Read/Write	0000b	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000 = 1 0001 = 2 … 1111 = 16

6.5.14 Amplifier Gain/Mute

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = Bh	Payload = xxxxh

Bits [19:16] = 'Bh', where bits [15:0] are defined below:

Bits [15:0]	Value	Description
15	0b	**Get Output/Input (GOI):** Controls whether the request is for the input amplifier or the output amplifier. When '0', the input amplifier is being requested. When '1', the output amplifier is being requested.
14	0b	'0'b
13	xb	**Get Left/Right (GLR):** This bit controls whether the request is for the left channel amplifier or the right channel amplifier. When '1', the left channel amplifier is being requested. When '0', the right channel amplifier is being requested.
12:4	000000000b	Reserved
3:0	0000b	**Index (IDX):** This field specifies the input index of the amplifier setting to return if the widget has multiple input amplifiers. It is only applicable if "Get Output/Input" is '0' which indicates input amplifier is being requested. This field has no meaning and ignored since the widget does not have multiple input amplifiers. It should be always '0's.

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	1b	**Amplifier Mute (AM):** This bit returns the Mute setting for the amplifier requested. A 1 indicates the amplifier is in the Mute condition. If the amplifier requested does not exist, a '0' will be returned. Default equals Muted.
6:0	Read Only	0110011b	**Amplifier Gain (AG):** This field returns the Gain setting for the amplifier requested. If the amplifier requested does not exist, all '0's will be returned Default equals 0 dB.

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	ADC1 Node ID=05h ADC2 Node ID=06h	Verb ID = 3h	Payload = xxxxh

Bits [19:16] = '3h', where bits [15:0] are defined below:

Bits	Type	Default	Description
15	Write Only	0b	**Set Output Amplifier (SOA):** Bit is always '0' since an output amplifier is not present.
14	Write Only	xb	**Set Input Amplifier (SIA):** Determines if the value programmed refers to the input amplifier. Set to a 1 for the value to be accepted.

Bits	Type	Default	Description
13	Write Only	xb	**Set Left Amplifier (SLA):** Selects the left channel (channel 0). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
12	Write Only	xb	**Set Right Amplifier (SRA):** Selects the right channel (channel 1). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
11:8	Write Only	0000b	**Index (IDX):** This field is used when programming the input amplifiers on Selector Widgets and Sum Widgets. This field is ignored.
7	Write Only	xb	**Mute (MUTE):** When '1', the Mute is active. When '0', the Mute is inactive.
6:0	Write Only	xxxxxxxb	**Gain (GAIN):** Specifies the amplifier gain in dB.

6.6 S/PDIF Receiver Input Converter Widget (Node ID = 07h)

6.6.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	1h	**Type (TYP):** Audio Input Converter Widget
19:16	Read Only	8h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	1b	**Digital (DIG):** Widget is a digital widget.
8	Read Only	1b	**Connection List (CL):** A connection list is present on this widget.
7	Read Only	1b	**Unsolicited Capable (UC):** Unsolicited Response is supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	1b	**Format Override (FO):** This bit is a ‘1’ to indicate that the widget contains format information, and the “Supported Formats” and “Supported PCM Bits, Rates” should be queried for the widget’s format capabilities.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.6.2 Supported PCM Size, Rates

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F00h	Parameter ID = 0Ah

Response Format:

Bits	Type	Default	Description
31:21	Read Only	00000000000b	Reserved
20	Read Only	1b	**32-Bit (32B):** 32-bit audio format is supported.
19	Read Only	1b	**24-Bit (24B):** 24-bit audio format is supported.
18	Read Only	1b	**20-Bit (20B):** 20-bit audio format is supported.
17	Read Only	1b	**16-Bit (16B):** 16-bit audio format is supported.
16	Read Only	0b	**8-Bit (8B):** 8-bit audio format is not supported.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**Rate-12 (R12):** 384 kHz (48*8) rate is not supported.
10	Read Only	1b	**Rate-11 (R11):** 192.0 kHz (48*4) rate is supported.
9	Read Only	0b	**Rate-10 (R10):** 176.4 kHz (44.1*4) rate is not supported.
8	Read Only	1b	**Rate-9 (R9):** 96.0 kHz (48*2) rate is supported.
7	Read Only	0b	**Rate-8 (R8):** 88.2 kHz (44.1*2) rate is not supported.
6	Read Only	1b	**Rate-7 (R7):** 48.0 kHz rate is supported.
5	Read Only	1b	**Rate-6 (R6):** 44.1 kHz rate is supported.
4	Read Only	1b	**Rate-5 (R5):** 32.0 kHz (48*2/3) rate is supported.
3	Read Only	0b	**Rate-4 (R4):** 22.05 kHz (44.1/2) rate is not supported.
2	Read Only	0b	**Rate-3 (R3):** 16.0 kHz (48/3) rate is not supported
1	Read Only	0b	**Rate-2 (R2):** 11.025 kHz (44.1/4) rate is not supported.
0	Read Only	0b	**Rate-1 (R1):** 8.0 kHz (48/6) rate is not supported.

6.6.3 Supported Stream Formats

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F00h	Parameter ID = 0Bh

Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	1b	**AC-3 (AC3):** AC-3 data is supported.
1	Read Only	0b	**Float32 (FLT32):** Float32 formatted data is not supported on this widget.
0	Read Only	1b	**Pulse Code Modulation (PCM):** PCM formatted data is supported on this widget.

6.6.4 Connection List Length

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F00h	Parameter ID = 0Eh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Long Form (LF):** Connection list is short form.
6:0	Read Only	0000001b	**Connection List Length (CLL):** One hard-wired input is possible for this widget.

6.6.5 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.6.6 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	00h	**Connection List Entry (N+1):** Returns 00h for N=00h-03h or N>03h.
7:0	Read Only	0Fh	**Connection List Entry (N):** Returns 0Fh (S/PDIF RX) for N=00h-03h. Returns 00h for N>03h.

6.6.7 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to '1'b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as '0'b. This bit is always a '1'b following a POR condition. For more information, see "Power State Settings Reset (PS-SettingsReset)" on p 28
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return '0'b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = '0000'b; D0 - Fully on. PSS = '0001'b; D1 - Not Supported PSS = '0010'b; D2 - Not Supported PSS = '0011'b; D3 - Allows for lowest possible power consumption under software control. See "D3 Lower Power State Support" on page 26 for more information. PSS = '0100'b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.6.8 Converter Stream, Channel

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F06h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = 706h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read/Write	0h	**Stream Number (SN):** Indicates the stream number used by the Input Converter. “0h” is stream 0, “1h” is stream 1, etc. By convention, stream 0 is reserved and unused so that converter whose stream number has been reset to “0h” does not unintentionally decode data not intended for them.
3:0	Read/Write	0h	**Lowest Channel Number (LCN):** Indicates the lowest channel used by the Input Converter. The stereo converter will use this LCN value plus 1 for its left and right channel.

6.6.9 Converter Format

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 07h	Verb ID = Ah	Payload = 0000h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 07h	Verb ID = 2h	Payload = xxxxh

Response Format:

Bits [15:0] must be programmed by software with the same value programmed into the Stream Descriptor, so that the data format being transmitted on the link matches what is expected by the consumer of the data.

If the TYPE is set to Non-PCM, the controller pushes data over the link and is not concerned with formatting. The base rate, data type, and number of Words (MULT) to send each valid frame are specified to control the rate at which the non-PCM data is sent.

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15	Read/Write	0b	**Stream Type (TYPE):** If TYPE is non-zero, the other bits in the format structure have other meanings. 0: PCM 1: Non-PCM

Bits	Type	Default	Description
14	Read/Write	0b	**Sample Base Rate (BASE):** 0 = 48 kHz 1 = 44.1 kHz
13:11	Read/Write	000b	**Sample Base Rate Multiple (MULT):** 000 = 48 kHz/44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) 100-111 = *Reserved*
10:8	Read/Write	000b	**Sample Base Rate Divisor (DIV):** 000 = Divide by 1 (48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	Read Only	0b	Reserved
6:4	Read/Write	000b	**Bits per Sample (BITS):** Number of bits in each sample: 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 101-111 = *Reserved*
3:0	Read/Write	0000b	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000 = 1 0001 = 2 … 1111 = 16

6.6.10 Digital Converter Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = F0Dh/**	Payload = 00h

** Note: Address F0Eh is not supported.

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 07h	Verb ID = 70Dh	Payload = xxh (SIC bits [7:0])
CAd = X	Node ID = 07h	Verb ID = 70Eh	Payload = xxh (SIC bits [15:8])

Response Format:

The S/PDIF IEC Control (SIC) bits are supported in one of two ways. In the first case referred to as “Codec Formatted SPDIF,” on an input PCM stream of less than 32 bits, the codec strips off the SIC bits before transferring the samples to the system and puts them in the Digital Converter Control for later software access.

In the second case, referred to as “Software Formatted (or Raw) SPDIF,” on a 32-bit input stream, the entire stream is transferred into the system without the codec stripping any bits. However, the codec must properly interpret the Sync Preamble bits of the stream and then send the appropriately coded preamble. The IEC 60958 specification, Section 4.3, “Preambles,” defines the preambles and the coding to be used. Software will specify the “B,” “M,” or “W” (also known as “X,” “Y,” or “Z”) preambles by encoding the last four bits of the preamble into the Sync Preamble section (bits 0-3) of the frame. The codec must examine the bits specified and encode the proper preamble based on the previous state. The previous state is to be maintained by the codec hardware.

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15	Read Only	0b	Reserved
14:8	Read Only	0000000b	**CC[6:0]** (Category Code): Programmed according to IEC standards, or as appropriate.
7	Read Only	0b	**L** (Generation Level): Programmed according to IEC standards, or as appropriate.
6	Read Only	0b	**PRO** (Professional): 1 indicates Professional use of channel status; 0 indicates Consumer.
5	Read Only	0b	**/AUDIO** (Non-Audio): 1 indicates data is non-PCM format; 0 indicates data is PCM.
4	Read Only	1b	**COPY** (Copyright): 1 indicates copyright is asserted; 0 indicates copyright is not asserted.
3	Read Only	1b	**PRE** (Pre-emphasis): 1 indicates filter pre-emphasis is 50/15 us; 0 pre-emphasis is none.
2	Read Only	0b	**VCFG** (Validity Config.): This bit is only defined for Output Converters and is Reserved, with a Read Only value of 0 for Input Converters.
1	Read Only	0b	**V** (Validity): This bit reflects the “Validity flag,” transmitted in each subframe.
0	Read/Write	0b	**DigEn** (Digital Enable): Enables or disables digital transmission. A 1 indicates that the digital data can pass through the node. A 0 indicates that the digital data is blocked from passing through the node, regardless of the state.

6.7 S/PDIF Transmitter 1, S/PDIF Transmitter 2 Output Converter Widgets (Node ID = 08h, 14h)

6.7.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	0h	**Type (TYP):** Audio Output Converter Widget
19:16	Read Only	4h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	1b	**Digital (DIG):** Widget is a digital widget.
8	Read Only	0b	**Connection List (CL):** A connection list is not present on this widget.
7	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	1b	**Format Override (FO):** This bit is a ‘1’ to indicate that the widget contains format information, and the “Supported Formats” and “Supported PCM Bits, Rates” should be queried for the widget’s format capabilities.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.7.2 Supported PCM Size, Rates

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = F00h	Parameter ID = 0Ah

Response Format:

Bits	Type	Default	Description
31:21	Read Only	00000000000b	Reserved
20	Read Only	1b	**32-Bit (32B):** 32-bit audio format is supported.
19	Read Only	1b	**24-Bit (24B):** 24-bit audio format is supported.
18	Read Only	1b	**20-Bit (20B):** 20-bit audio format is supported.
17	Read Only	1b	**16-Bit (16B):** 16-bit audio format is supported.
16	Read Only	0b	**8-Bit (8B):** 8-bit audio format is not supported.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**Rate-12 (R12):** 384 kHz (48*8) rate is not supported.
10	Read Only	1b	**Rate-11 (R11):** 192.0 kHz (48*4) rate is supported.
9	Read Only	1b	**Rate-10 (R10):** 176.4 kHz (44.1*4) rate is supported.
8	Read Only	1b	**Rate-9 (R9):** 96.0 kHz (48*2) rate is supported.
7	Read Only	1b	**Rate-8 (R8):** 88.2 kHz (44.1*2) rate is supported.
6	Read Only	1b	**Rate-7 (R7):** 48.0 kHz rate is supported.
5	Read Only	1b	**Rate-6 (R6):** 44.1 kHz rate is supported.
4	Read Only	1b	**Rate-5 (R5):** 32.0 kHz (48*2/3) rate is supported.
3	Read Only	0b	**Rate-4 (R4):** 22.05 kHz (44.1/2) rate is not supported.
2	Read Only	0b	**Rate-3 (R3):** 16.0 kHz (48/3) rate is not supported
1	Read Only	0b	**Rate-2 (R2):** 11.025 kHz (44.1/4) rate is not supported.
0	Read Only	0b	**Rate-1 (R1):** 8.0 kHz (48/6) rate is not supported.

6.7.3 Supported Stream Formats

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = F00h	Parameter ID = 0Bh

Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	1b	**AC-3 (AC3):** AC-3 data is supported.
1	Read Only	0b	**Float32 (FLT32):** Float32 formatted data is not supported on this widget.
0	Read Only	1b	**Pulse Code Modulation (PCM):** PCM formatted data is supported on this widget.

6.7.4 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.7.5 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to ‘1’b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as ‘0’b. This bit is always a ‘1’b following a POR condition. For more information, see “Power State Settings Reset (PS-SettingsReset)” on p 28
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return ‘0’b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = ’0000’b; D0 - Fully on. PSS = ‘0001’b; D1 - Not Supported PSS = ‘0010’b; D2 - Not Supported PSS = ‘0011’b; D3 - Allows for lowest possible power consumption under software control. See “D3 Lower Power State Support” on page 26 for more information. PSS = ‘0100’b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.7.6 Converter Stream, Channel

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = F06h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = 706h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:4	Read/Write	0h	**Stream Number (SN):** Indicates the stream number used by the Output Converter. “0h” is stream 0, “1h” is stream 1, etc. By convention, stream 0 is reserved and unused so that converter whose stream number has been reset to “0h” does not unintentionally decode data not intended for them.
3:0	Read/Write	0h	**Lowest Channel Number (LCN):** Indicates the lowest channel used by the Output Converter. The stereo converter will use this LCN value plus 1 for its left and right channel.

6.7.7 Converter Format

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = Ah	Payload = 0000h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = 2h	Payload = xxxxh

Response Format:

Bits [15:0] must be programmed by software with the same value programmed into the Stream Descriptor, so that the data format being transmitted on the link matches what is expected by the consumer of the data.

If the TYPE is set to Non-PCM, the controller pushes data over the link and is not concerned with formatting. The base rate, data type, and number of Words (MULT) to send each valid frame are specified to control the rate at which the non-PCM data is sent.

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15	Read/Write	0b	**Stream Type (TYPE):** If TYPE is non-zero, the other bits in the format structure have other meanings. 0: PCM 1: Non-PCM
14	Read/Write	0b	**Sample Base Rate (BASE):** 0 = 48 kHz 1 = 44.1 kHz
13:11	Read/Write	000b	**Sample Base Rate Multiple (MULT):** 000 = 48 kHz/44.1 kHz or less 001 = x2 (96 kHz, 88.2 kHz, 32 kHz) 010 = x3 (144 kHz) 011 = x4 (192 kHz, 176.4 kHz) 100-111 = *Reserved*
10:8	Read/Write	000b	**Sample Base Rate Divisor (DIV):** 000 = Divide by 1 (48 kHz, 44.1 kHz) 001 = Divide by 2 (24 kHz, 22.05 kHz) 010 = Divide by 3 (16 kHz, 32 kHz) 011 = Divide by 4 (11.025 kHz) 100 = Divide by 5 (9.6 kHz) 101 = Divide by 6 (8 kHz) 110 = Divide by 7 111 = Divide by 8 (6 kHz)
7	Read Only	0b	Reserved
6:4	Read/Write	000b	**Bits per Sample (BITS):** Number of bits in each sample: 000 = 8 bits. The data will be packed in memory in 8-bit containers on 16-bit boundaries. 001 = 16 bits. The data will be packed in memory in 16-bit containers on 16-bit boundaries. 010 = 20 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 011 = 24 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 100 = 32 bits. The data will be packed in memory in 32-bit containers on 32-bit boundaries. 101-111 = *Reserved*
3:0	Read/Write	0000b	**Number of Channels (CHAN):** Number of channels in each frame of the stream: 0000 = 1 0001 = 2 … 1111 = 16

6.7.8 Digital Converter Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = F0Dh/**	Payload = 00h

** Note: Address F0Eh is not supported.

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = 70Dh	Payload = xxh (SIC bits [7:0])
CAd = X	S/P Tx 1 Node ID=08h S/P Tx 2 Node ID=14h	Verb ID = 70Eh	Payload = xxh (SIC bits [15:8])

Response Format:

The S/PDIF IEC Control (SIC) bits are supported in one of two ways. In the first case referred to as “Codec Formatted SPDIF,” if a PCM bit stream of less than 32 bits is specified in the Converter Format control, then the S/PDIF Control bits, including the “V,” “PRE,” “/AUDIO,” and other such bits are embedded in the stream by the codec using the values (SIC bits) from the Digital Converter Control.

In the second case referred to as “Software Formatted (or Raw) SPDIF,” if a 32-bit stream is specified in the Converter Format control, the S/PDIF IEC Control (SIC) bits are assumed to be embedded in the stream by software, and the raw 32-bit stream is transferred on the link with no modification by the codec. However, the codec must properly interpret the Sync Preamble bits of the stream and then send the appropriately coded preamble. The IEC60958 specification, Section 4.3, “Preambles,” defines the preambles and the coding to be used. Software will specify the “B,” “M,” or “W” (also known as “X,” “Y,” or “Z”) preambles by encoding the last four bits of the preamble into the Sync Preamble section (bits 0-3) of the frame. The codec must examine the bits specified and encode the proper preamble based on the previous state. The previous state is to be maintained by the codec hardware.

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15	Read Only	0b	Reserved
14:8	Read/Write	0000000b	**CC[6:0]** (Category Code): Programmed according to IEC standards, or as appropriate.
7	Read/Write	0b	**L** (Generation Level): Programmed according to IEC standards, or as appropriate.
6	Read/Write	0b	**PRO** (Professional): 1 indicates Professional use of channel status; 0 indicates Consumer.
5	Read/Write	0b	**/AUDIO** (Non-Audio): 1 indicates data is non-PCM format; 0 indicates data is PCM.
4	Read/Write	0b	**COPY** (Copyright): 1 indicates copyright is asserted; 0 indicates copyright is not asserted.
3	Read/Write	0b	**PRE** (Pre-emphasis): 1 indicates filter pre-emphasis is 50/15 µs; 0 pre-emphasis is none.

Bits	Type	Default	Description
2	Read/Write	0b	**VCFG** (Validity Config.): Determines S/PDIF transmitter behavior when data is not being transmitted. When asserted, this bit forces the de-assertion of the S/PDIF "Validity" flag, which is bit 28 transmitted in each S/PDIF subframe. This bit is only defined for Output Converters and is defined as Reserved, with a Read Only value of 0 for Input Converters. ♦ If "V" = 0 and "VCFG"=0, then for each S/PDIF subframe (Left and Right) bit[28] "Validity" flag reflects whether or not an internal codec error has occurred (specifically whether the S/PDIF interface received and transmitted a valid sample from the High Definition Audio Link). If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be 0 for that subframe. Otherwise, the "Validity" flag for that subframe should be transmitted as "1." ♦ If "V" = 0 and "VCFG" = 1, then for each S/PDIF subframe (Left and Right), bit[28] "Validity" flag reflects whether or not an internal codec transmission error has occurred. Specifically, an internal codec error should result in the "Validity" flag being set to 1. In the case where the S/PDIF transmitter is not receiving a sample or does not receive a valid sample from the High Definition Audio Controller (Left or Right), the S/PDIF transmitter should set the S/PDIF "Validity" flag to 0 and pad each of the S/PDIF "Audio Sample Word" in question with 0's for the subframe in question. If a valid sample (Left or Right) was received and successfully transmitted, the "Validity" flag should be 0 for that subframe. ♦ If "V" = 1 and "VCFG" = 0, then each S/PDIF subframe (Left and Right) should have bit[28] "Validity" flag = 1. This tags all S/PDIF subframes as invalid. ♦ "V" = 1 and "VCFG" = 1 state is reserved for future use. ♦ Default state, coming out of reset, for "V" and "VCFG" should be 0 and 0 respectively.
1	Read/Write	0b	**V** (Validity): This bit affects the "Validity flag," bit[28] transmitted in each subframe, and enables the S/PDIF transmitter to maintain connection during error or mute conditions. The behavior of the S/PDIF transmitter with respect to this bit depends on the value of the "VCFG" bit.
0	Read/Write	0b	**DigEn** (Digital Enable): Enables or disables digital transmission. A 1 indicates that the digital data can pass through the node. A 0 indicates that the digital data is blocked from passing through the node, regardless of the state.

6.8 Headphone Pin Widget (Node ID = 09h)

6.8.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	4h	**Type (TYP):** Pin Complex Widget
19:16	Read Only	1h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	1b	**Connection List (CL):** A connection list is present on this widget.
7	Read Only	1b	**Unsolicited Capable (UC):** Unsolicited Response is supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.8.2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.

Bits	Type	Default	Description
15:8	Read Only	00h	**VREF Control (VREFC):** VREF generation is not supported by this widget.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	0b	**Balanced I/O Pins (BIOP):** This widget does not have balanced I/O pins.
5	Read Only	0b	**Input Capable (INC):** Is not input capable.
4	Read Only	1b	**Output Capable (OUTC):** This bit is '1' to indicate that the widget is output capable.
3	Read Only	1b	**Headphone Drive Capable (HDC):** Widget is capable of driving headphones directly.
2	Read Only	1b	**Presence Detect Capable (PDC):** A '1' indicates the widget is capable of performing presence detect.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.
0	Read Only	0b	**Impedance Sense Capable (ISC):** This bit is '0' to indicate that the widget does not support impedance sense on the attached peripheral.

6.8.3 Connection List Length

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F00h	Parameter ID = 0Eh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Long Form (LF):** Connection list is short form.
6:0	Read Only	0000001b	**Connection List Length (CLL):** One hard-wired input for this widget.

6.8.4 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.8.5 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	00h	**Connection List Entry (N+1):** Returns 00h for N=00h-03h or N>03h.
7:0	Read Only	02h	**Connection List Entry (N):** Returns 02h (DAC1) for N=00h-03h. Returns 00h for N>03h.

6.8.6 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to ‘1’b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as ‘0’b. This bit is always a ‘1’b following a POR condition. For more information, see “Power State Settings Reset (PS-SettingsReset)” on p 28
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return ‘0’b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.

Bits	Type	Default	Description
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = ’0000’b; D0 - Fully on. PSS = ‘0001’b; D1 - Not Supported PSS = ‘0010’b; D2 - Not Supported PSS = ‘0011’b; D3 - Allows for lowest possible power consumption under software control. See “D3 Lower Power State Support” on page 26 for more information. PSS = ‘0100’b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.8.7 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read/Write	0b	**H-Phone Enable (HPE)**: This bit has no effect on the output path. Per HD Audio spec, a '1' enables a low impedance amplifier associated with the output. When '0', this bit disables a low impedance amplifier associated with the output.
6	Read/Write	0b	**Output Enable (OUTE)**: This bit has no effect on the output path. Per HD Audio spec, a '1' enables the output path of the Pin Widget. When '0', the output path of the Pin Widget is shut off.
5	Read Only	0b	**Input Enable (INE)**: Set to '0' since there is no input path associated with the pin widget.
4:3	Read Only	00b	Reserved
2:0	Read Only	000b	**VREF Enable (VREFE)**: This field selects one of the possible states for the VREF signal(s). The Pin Widget does not support VREF generation as indicated in the Pin Capabilities. As such, this field will always be "000b" to select Hi-Z state.

6.8.8 Unsolicited Response Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F08h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = 708h	Payload = xxh

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Function Group Reset:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read/Write	0b	**Enable:** Controls the actual generation of Unsolicited Responses. 1 is enable; 0 is disable.
6	Read Only	0b	Reserved
5:0	Read/Write	000000b	**Tag:** Is a 6 bit value assigned and used by software to determine what codec node generated the unsolicited response. The value programmed into the Tag field is returned in the top 6 bits (31:26) of every Unsolicited Response generated by this node.

Unsolicited Response Format:

Bits [31:26]	Bits [25:0]
Tag	Response

6.8.9 Pin Sense

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F09h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = 709h	Payload = xxh

Get Response Format:

Bits	Type	Default	Description
31	Read Only	0b	**Presence Detect (PDET)**: A '1' indicates that something is plugged into the jack associated with the Pin Widget. A '0' indicates that nothing is plugged in.
30:0	Read Only	0	**Impedance Sense (IMPS)**: Not valid since the widget is not capable of impedance sensing.

Pin Sense Execute Format:

Bits	Type	Default	Description
7:1	Write Only	0000000b	Reserved
0	Write Only	0b	**Right Channel (RCHAN):** A write to this bit is ignored since the widget is not capable of impedance sensing.

6.8.10 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 09h	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 09h	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 09h	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 09h	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a CODEC Reset:

Bits	Type	Default	Description
31:30	Read/Write	00b	**Port Connectivity (PCON):** The port complex is connected to a jack.
29:24	Read/Write	000010b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to External | Front.
23:20	Read/Write	2h	**Default Device (DD):** Indicates the intended use of the connection is for Headphone.
19:16	Read/Write	1h	**Connection Type (CTYP):** Indicates the type of physical connection is 1/8” jack.
15:12	Read/Write	4h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color selected is Green.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	Fh	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all ‘0’s is reserved. A value of all ‘1’s in this field indicates that the Association has the lowest priority.
3:0	Read/Write	0h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.9 Line Out 1 Pin Widget (Node ID = 0Ah)

6.9.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	4h	**Type (TYP):** Pin Complex Widget
19:16	Read Only	1h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	1b	**Connection List (CL):** A connection list is present on this widget.
7	Read Only	1b	**Unsolicited Capable (UC):** Unsolicited Response is supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.9.2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.
15:8	Read Only	00h	**VREF Control (VREFC):** VREF generation is not supported by this widget.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	1b	**Balanced I/O Pins (BIOP):** This widget has balanced I/O pins.
5	Read Only	0b	**Input Capable (INC):** The widget is not input capable.
4	Read Only	1b	**Output Capable (OUTC):** This bit is '1' to indicate that the widget is output capable.
3	Read Only	0b	**Headphone Drive Capable (HDC):** Widget is not capable of driving headphones directly.
2	Read Only	1b	**Presence Detect Capable (PDC):** This bit is '1' to indicate that the widget is capable of performing presence detect.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.
0	Read Only	0b	**Impedance Sense Capable (ISC):** This bit is '0' to indicate that the widget does not support impedance sense on the attached peripheral.

6.9.3 Connection List Length

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F00h	Parameter ID = 0Eh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Long Form (LF):** Connection list is short form.
6:0	Read Only	0000001b	**Connection List Length (CLL):** One hard-wired input for this widget.

6.9.4 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.9.5 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	00h	**Connection List Entry (N+1):** Returns 00h for N=00h-03h or N>03h.
7:0	Read Only	03h	**Connection List Entry (N):** Returns 03h (DAC2) for N=00h-03h. Returns 00h for N>03h.

6.9.6 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to '1'b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as '0'b. This bit is always a '1'b following a POR condition. For more information, see "Power State Settings Reset (PS-SettingsReset)" on p 28
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return '0'b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = '0000'b; D0 - Fully on. PSS = '0001'b; D1 - Not Supported PSS = '0010'b; D2 - Not Supported PSS = '0011'b; D3 - Allows for lowest possible power consumption under software control. See "D3 Lower Power State Support" on page 26 for more information. PSS = '0100'b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.9.7 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**H-Phone Enable (HPE)**: Set to '0' since there is no low impedance amplifier associated with this pin widget.
6	Read/Write	0b	**Output Enable (OUTE)**: This bit has no effect on the output path. Per HD Audio spec, a '1' enables the output path of the Pin Widget. When '0', the output path of the Pin Widget is shut off.
5	Read Only	0b	**Input Enable (INE)**: Set to '0' since there is no input path associated with the pin widget.
4:3	Read Only	00b	Reserved
2:0	Read Only	000b	**VREF Enable (VREFE)**: The Pin Widget does not support VREF generation as indicated in the Pin Capabilities. As such, this field should always be "000b" to select the Hi-Z state.

6.9.8 Unsolicited Response Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F08h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = 708h	Payload = xxh

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Function Group Reset:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read/Write	0b	**Enable:** Controls the actual generation of Unsolicited Responses. 1 is enable; 0 is disable.
6	Read Only	0b	Reserved
5:0	Read/Write	000000b	**Tag:** Is a 6 bit value assigned and used by software to determine what codec node generated the unsolicited response. The value programmed into the Tag field is returned in the top 6 bits (31:26) of every Unsolicited Response generated by this node.

Unsolicited Response Format:

Bits [31:26]	Bits [25:0]
Tag	Response

6.9.9 Pin Sense

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F09h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = 709h	Payload = xxh

Get Response Format:

Bits	Type	Default	Description
31	Read Only	0b	**Presence Detect (PDET)**: A '1' indicates that there is "something" plugged into the jack associated with the Pin Widget. A '0' indicates that nothing is plugged in.
30:0	Read Only	0	**Impedance Sense (IMPS)**: Not valid since the widget is not capable of impedance sensing.

Pin Sense Execute Format:

Bits	Type	Default	Description
7:1	Write Only	0000000b	Reserved
0	Write Only	0b	**Right Channel (RCHAN):** A write to this bit is ignored since the widget is not capable of impedance sensing.

6.9.10 EAPD/BTL Enable

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F0Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = 70Ch	Payload = xxh

Get Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	0b	**L-R Swap**: Not valid since the widget is not capable of left/right swapping.
1	Read Only	0b	**EAPD**: EAPD is not supported by this pin widget.
0	Read/Write	0b	**BTL:** controls the output configuration of a Pin Widget which has indicated support for balanced I/O (bit 6, Pin Capabilities Parameter). When this bit is 0, the output drivers are configured in normal, single-ended mode; when this bit is 1, they are configured in balanced mode.

6.9.11 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ah	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 0Ah	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 0Ah	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 0Ah	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	00b	**Port Connectivity (PCON):** The port complex is connected to a jack.
29:24	Read/Write	000001b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to External | Rear.
23:20	Read/Write	0h	**Default Device (DD):** Indicates the intended use of the connection is for Line Out.
19:16	Read/Write	1h	**Connection Type (CTYP):** Indicates the type of physical connection is 1/8” jack.
15:12	Read/Write	4h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color selected is Green.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	Fh	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all ‘0’s is reserved. A value of all ‘1’s in this field indicates that the Association has the lowest priority.
3:0	Read/Write	0h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.10 Line Out 2 Pin Widget (Node ID = 0Bh)

6.10.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	4h	**Type (TYP):** Pin Complex Widget
19:16	Read Only	1h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	0b	**Power Control (PC):** Power State control is not supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	1b	**Connection List (CL):** A connection list is present on this widget.
7	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.10.2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.
15:8	Read Only	00h	**VREF Control (VREFC):** VREF generation is not supported by this widget.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	1b	**Balanced I/O Pins (BIOP):** This widget has balanced I/O pins.
5	Read Only	0b	**Input Capable (INC):** The widget is not input capable.
4	Read Only	1b	**Output Capable (OUTC):** This bit is '1' to indicate that the widget is output capable.
3	Read Only	0b	**Headphone Drive Capable (HDC):** Widget is not capable of driving headphones directly.
2	Read Only	0b	**Presence Detect Capable (PDC):** This bit is '0' to indicate that the widget is not capable of performing presence detect to determine whether there is anything plugged in.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.
0	Read Only	0b	**Impedance Sense Capable (ISC):** This bit is '0' to indicate that the widget does not support impedance sense on the attached peripheral.

6.10.3 Connection List Length

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = F00h	Parameter ID = 0Eh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Long Form (LF):** Connection list is short form.
6:0	Read Only	0000001b	**Connection List Length (CLL):** One hard-wired input for this widget.

6.10.4 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	00h	**Connection List Entry (N+1):** Returns 00h for N=00h-03h or N>03h.
7:0	Read Only	04h	**Connection List Entry (N):** Returns 04h (DAC3) for N=00h-03h. Returns 00h for N>03h.

6.10.5 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**H-Phone Enable (HPE)**: Set to ‘0’ since there is no low impedance amplifier associated with this pin widget.
6	Read/Write	0b	**Output Enable (OUTE)**: This bit has no effect on the output path. Per HD Audio spec, a ‘1’ enables the output path of the Pin Widget. When ‘0’, the output path of the Pin Widget is shut off.
5	Read Only	0b	**Input Enable (INE)**: Set to ‘0’ since there is no input path associated with the pin widget.
4:3	Read Only	00b	Reserved
2:0	Read Only	000b	**VREF Enable (VREFE)**: The Pin Widget does not support VREF generation as indicated in the Pin Capabilities. As such, this field should always be “000b” to select the Hi-Z state.

6.10.6 EAPD/BTL Enable

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = F0Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = 70Ch	Payload = xxh

Get Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	0b	**L-R Swap**: Not valid since the widget is not capable of left/right swapping.
1	Read Only	0b	**EAPD**: EAPD is not supported by this pin widget.
0	Read/Write	0b	**BTL:** controls the output configuration of a Pin Widget which has indicated support for balanced I/O (bit 6, Pin Capabilities Parameter). When this bit is 0, the output drivers are configured in normal, single-ended mode; when this bit is 1, they are configured in balanced mode.

6.10.7 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Bh	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 0Bh	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 0Bh	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 0Bh	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	10b	**Port Connectivity (PCON):** The port complex is connected to a fixed function device.
29:24	Read/Write	010000b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to Internal | N/A.
23:20	Read/Write	1h	**Default Device (DD):** Indicates the intended use of the connection is for Speaker.
19:16	Read/Write	7h	**Connection Type (CTYP):** Indicates the type of physical connection is Other Analog.
15:12	Read/Write	0h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color for an internal connection is Unknown.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	Fh	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all ‘0’s is reserved. A value of all ‘1’s in this field indicates that the Association has the lowest priority.
3:0	Read/Write	0h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.11 Line In 1/Mic In 2, Mic In 1/Line In 2 Pin Widgets (Node ID = 0Ch, 0Dh)

6.11.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	4h	**Type (TYP):** Pin Complex Widget
19:16	Read Only	1h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	0b	**Connection List (CL):** A connection list is not present on this widget.
7	Read Only	1b	**Unsolicited Capable (UC):** Unsolicited Response is supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	1b	**Amplifier Parameter Override (APO):** This widget contains its own amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	1b	**Input Amplifier Present (IAP):** Input amplifier is present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.11.2 Line In 1/Mic In 2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ch	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.

Bits	Type	Default	Description
15:8	Read Only	00h	**VREF Control (VREFC):** VREF generation is not supported by this widget.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	0b	**Balanced I/O Pins (BIOP):** This widget does not have balanced I/O pins.
5	Read Only	1b	**Input Capable (INC):** Widget is input capable.
4	Read Only	0b	**Output Capable (OUTC):** Widget is not output capable.
3	Read Only	0b	**Headphone Drive Capable (HDC):** Widget is not capable of driving headphones directly.
2	Read Only	1b	**Presence Detect Capable (PDC):** This bit is '1' to indicate that the widget is capable of performing presence detect to determine whether there is anything plugged in.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.
0	Read Only	0b	**Impedance Sense Capable (ISC):** This bit is '0' to indicate that the widget does not support impedance sense on the attached peripheral.

6.11.3 Mic In 1/Line In 2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Dh	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.
15:8	Read Only	17h	**VREF Control (VREFC):** VREF generation is supported by this widget. Ground/80%/50%/Hi-Z are supported. 100% is not supported.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	1b	**Balanced I/O Pins (BIOP):** This widget has balanced I/O pins.
5	Read Only	1b	**Input Capable (INC):** Widget is input capable.
4	Read Only	0b	**Output Capable (OUTC):** Widget is not output capable.
3	Read Only	0b	**Headphone Drive Capable (HDC):** Widget is not capable of driving headphones directly.
2	Read Only	1b	**Presence Detect Capable (PDC):** This bit is '1' to indicate that the widget is capable of performing presence detect to determine whether there is anything plugged in.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.

Bits	Type	Default	Description
0	Read Only	0b	**Impedance Sense Capable (ISC):** This bit is '0' to indicate that the widget does not support impedance sense on the attached peripheral.

6.11.4 Input Amplifier Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = F00h	Parameter ID = 0Dh

Response Format:

Bits	Type	Default	Description
31	Read Only	0b	**Mute Capable (MC):** Does not support mute.
30:23	Read Only	00000000b	Reserved
22:16	Read Only	0100111b	**Step Size (SS):** Indicates that the size of each amplifier's step gain is 10 dB.
15	Read Only	0b	Reserved
14:8	Read Only	0000011b	**Number of Steps (NOS):** There are 4 gain steps; 0 dB, +10 dB, +20 dB, and +30 dB.
7	Read Only	0b	Reserved
6:0	Read Only	0000000b	**Offset (OFST):** Indicates that if "0000000b" is programmed into the Amplified Gain Control, it would result in a gain of 0 dB.

6.11.5 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.11.6 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to ‘1’b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as ‘0’b. This bit is always a ‘1’b following a POR condition. For more information, see “Power State Settings Reset (PS-SettingsReset)” on p 28
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return ‘0’b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = ’0000’b; D0 - Fully on. PSS = ‘0001’b; D1 - Not Supported PSS = ‘0010’b; D2 - Not Supported PSS = ‘0011’b; D3 - Allows for lowest possible power consumption under software control. See “D3 Lower Power State Support” on page 26 for more information. PSS = ‘0100’b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.11.7 Line In 1/Mic In 2 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ch	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ch	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**H-Phone Enable (HPE)**: Not supported on this widget.
6	Read Only	0b	**Output Enable (OUTE)**: Not supported on this widget.
5	Read/Write	0b	**Input Enable (INE)**: This bit has no effect on the input path. Per HD Audio Spec, when '1', this bit enables the input path of the Pin Widget. When '0', the input path of the Pin Widget is shut off.
4:3	Read Only	00b	Reserved
2:0	Read Only	000b	**VREF Enable (VREFE)**: Not supported on this widget.

6.11.8 Mic In 1/Line In 2 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Dh	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Dh	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**H-Phone Enable (HPE)**: Not supported on this widget.
6	Read/Write	0b	**Output Enable (OUTE)**: Not supported on this widget. Used by WHQL test to set VREFE = Hi-Z mode.
5	Read/Write	0b	**Input Enable (INE)**: This bit has no effect on the input path. Per HD Audio Spec., when '1', this bit enables the input path of the Pin Widget. When set to '0', the input path of the Pin Widget will continue to operate.
4:3	Read Only	00b	Reserved

Bits	Type	Default	Description
2:0	Read/Write	000b	**VREF Enable (VREFE)**: This field selects one of the possible states for the VREF signal(s). The pin associated with this function is MICBIAS. If the value written to this control does not correspond to a supported value (‘000’b, ‘001’b, ‘010’b or ‘100’b), the VREFE bits must retain the previous value. ‘000’b = Hi-Z ‘001’b = 0.5*VA ‘010’b = GND ‘100’b = 0.8*VA

6.11.9 Unsolicited Response Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = F08h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = 708h	Payload = xxh

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read/Write	0b	**Enable:** Controls the actual generation of Unsolicited Responses. 1 is enable; 0 is disable.
6	Read Only	0b	Reserved
5:0	Read/Write	000000b	**Tag:** Is a 6 bit value assigned and used by software to determine what codec node generated the unsolicited response. The value programmed into the Tag field is returned in the top 6 bits (31:26) of every Unsolicited Response generated by this node.

Unsolicited Response Format:

Bits [31:26]	Bits [25:0]
Tag	Response

6.11.10 Pin Sense

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = F09h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = 709h	Payload = xxh

Get Response Format:

Bits	Type	Default	Description
31	Read Only	0b	**Presence Detect (PDET)**: A '1' indicates that there is "something" plugged into the jack associated with the Pin Widget. A '0' indicates that nothing is plugged in.
30:0	Read Only	0	**Impedance Sense (IMPS)**: Not valid since the widget is not capable of impedance sensing.

Pin Sense Execute Format:

Bits	Type	Default	Description
7:1	Write Only	0000000b	Reserved
0	Write Only	0b	**Right Channel (RCHAN):** A write to this bit is ignored since the widget is not capable of impedance sensing.

6.11.11 Mic In 1/Line In 2 EAPD/BTL Enable

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Dh	Verb ID = F0Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Dh	Verb ID = 70Ch	Payload = xxh

Get Response Format:

Bits	Type	Default	Description
31:3	Read Only	0	Reserved
2	Read Only	0b	**L-R Swap**: Not valid since the widget is not capable of left/right swapping.
1	Read Only	0b	**EAPD**: Not supported on this widget.
0	Read/Write	0b	**BTL:** controls the input configuration of a Pin Widget which has indicated support for balanced I/O (bit 6, Pin Capabilities Parameter). When this bit is 0, the inputs are configured in single-ended or pseudo-differential mode; when this bit is 1, they are configured in balanced (fully differential) mode. *Note: This bit is OR'ed with the **ADC2 Gain** bit in the* ADC Configuration (CIR = 0002h) *Register of the* Vendor Processing Widget (Node ID = 11h).

6.11.12 Line In 1/Mic In 2 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ch	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Ch	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 0Ch	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 0Ch	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 0Ch	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	00b	**Port Connectivity (PCON):** The port complex is connected to a jack.
29:24	Read/Write	000001b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to External | Rear.
23:20	Read/Write	8h	**Default Device (DD):** Indicates the intended use of the connection is for Line In.
19:16	Read/Write	1h	**Connection Type (CTYP):** Indicates the type of physical connection is 1/8" jack.
15:12	Read/Write	3h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color selected is Blue.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	5h	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all '0's is reserved. A value of all '1's in this field indicates that the Association has the lowest priority.
3:0	Read/Write	1h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.11.13 Mic In 1/Line In 2 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Dh	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Dh	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 0Dh	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 0Dh	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 0Dh	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	00b	**Port Connectivity (PCON):** The port complex is connected to a jack.
29:24	Read/Write	000001b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to External | Rear.
23:20	Read/Write	Ah	**Default Device (DD):** Indicates the intended use of the connection is for Mic In.
19:16	Read/Write	1h	**Connection Type (CTYP):** Indicates the type of physical connection is 1/8" jack.
15:12	Read/Write	9h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color selected is Pink.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	3h	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all '0's is reserved. A value of all '1's in this field indicates that the Association has the lowest priority.
3:0	Read/Write	1h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.11.14 Amplifier Gain/Mute

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = Bh	Payload = xxxxh

Bits [19:16] = 'Bh', where bits [15:0] are defined below:

Bits [15:0]	Value	Description
15	0b	**Get Output/Input (GOI):** This bit controls whether the request is for the input amplifier or the output amplifier. When '1', the output amplifier is being requested. When '0', the input amplifier is being requested.
14	0b	'0'b
13	xb	**Get Left/Right (GLR):** This bit controls whether the request is for the left channel amplifier or the right channel amplifier. When '1', the left channel amplifier is being requested. When '0', the right channel amplifier is being requested.
12:4	000000000b	Reserved
3:0	0000b	**Index (IDX):** This field specifies the input index of the amplifier setting to return if the widget has multiple input amplifiers. This field has no meaning and ignored since the widget does not have multiple input amplifiers. It should be always '0's.

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Amplifier Mute (AM):** Mute is not supported by this widget.
6:0	Read Only	0000000b	**Amplifier Gain (AG):** This field returns the Gain setting for the amplifier requested. If the amplifier requested does not exist, all '0's will be returned. Default equals 0 dB.

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Line In 1 Node ID=0Ch Mic In 1 Node ID=0Dh	Verb ID = 3h	Payload = xxxxh

Bits [19:16] = '3h', where bits [15:0] are defined below:

Bits	Type	Default	Description
15	Write Only	0b	**Set Output Amplifier (SOA):** This bit determines whether the value programmed refers to the output amplifier. This bit should always be '0' since an output amplifier is not present on this widget.
14	Write Only	xb	**Set Input Amplifier (SIA):** This bit determines whether the value programmed refers to the input amplifier. Set to a 1 for the value to be accepted.
13	Write Only	xb	**Set Left Amplifier (SLA):** Selects the left channel (channel 0). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
12	Write Only	xb	**Set Right Amplifier (SRA):** Selects the right channel (channel 1). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
11:8	Write Only	0000b	**Index (IDX):** This field is used when programming the input amplifiers on Selector Widgets and Sum Widgets. This field is ignored.
7	Write Only	0b	**Mute (MUTE):** When '0', the Mute is inactive. This field is ignored.
6:0	Write Only	xxxxxxxb	**Gain (GAIN):** Specifies the amplifier gain in dB. xxxxx00b = 0 dB xxxxx01b = +10 dB xxxxx10b = +20 dB xxxxx11b = +30 dB Bits(6:2) are not used and are ignored.

6.12 Digital Mic In 1, Digital Mic In 2 Pin Widgets (Node ID = 0Eh, 12h)

6.12.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DigMic 1 Node ID=0Eh DigMic 2 Node ID=12h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	4h	**Type (TYP):** Pin Complex Widget
19:16	Read Only	1h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	0b	**Power Control (PC):** Power State control is not supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	0b	**Connection List (CL):** A connection list is not present on this widget.
7	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	1b	**Amplifier Parameter Override (APO):** This widget contains its own amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	1b	**Input Amplifier Present (IAP):** Input amplifier is present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.12.2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DigMic 1 Node ID=0Eh DigMic 2 Node ID=12h	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.
15:8	Read Only	00h	**VREF Control (VREFC):** VREF not supported.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	0b	**Balanced I/O Pins (BIOP):** This widget does not have balanced I/O pins.
5	Read Only	1b	**Input Capable (INC):** Input capable.
4	Read Only	0b	**Output Capable (OUTC):** Not output capable.
3	Read Only	0b	**Headphone Drive Capable (HDC):** Widget is not capable of driving headphones directly.
2	Read Only	0b	**Presence Detect Capable (PDC):** This bit is '0' to indicate that the widget is not capable of performing presence detect.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.
0	Read Only	0b	**Impedance Sense Capable (ISC):** This bit is '0' to indicate that the widget does not support impedance sense on the attached peripheral.

6.12.3 Input Amplifier Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DigMic 1 Node ID=0Eh DigMic 2 Node ID=12h	Verb ID = F00h	Parameter ID = 0Dh

Response Format:

Bits	Type	Default	Description
31	Read Only	0b	**Mute Capable (MC):** Does not support mute.
30:23	Read Only	00000000b	Reserved
22:16	Read Only	0100111b	**Step Size (SS):** Indicates that the size of each amplifier's step gain is 10 dB.
15	Read Only	0b	Reserved
14:8	Read Only	0000010b	**Number of Steps (NOS):** There are 3 gain steps; 0 dB, +10 dB and +20 dB.
7	Read Only	0b	Reserved
6:0	Read Only	0000000b	**Offset (OFST):** Indicates that if "0000000b" is programmed into the Amplified Gain Control, it would result in a gain of 0 dB.

6.12.4 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DigMic 1 Node ID=0Eh DigMic 2 Node ID=12h	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	DigMic 1 Node ID=0Eh DigMic 2 Node ID=12h	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**H-Phone Enable (HPE)**: Not supported.
6	Read Only	0b	**Output Enable (OUTE)**: Not supported.
5	Read/Write	0b	**Input Enable (INE)**: This bit, when set to '1', enables the data path for the corresponding DMIC. When set to '0', the data path is disabled and the corresponding ADC output is muted.
4:3	Read Only	00b	Reserved
2:0	Read Only	000b	**VREF Enable (VREFE)**: VREF is not supported on this widget. Will always read back '000'

6.12.5 Digital Mic In 1 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Eh	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Eh	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 0Eh	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 0Eh	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 0Eh	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	10b	**Port Connectivity (PCON):** The port complex is connected to a fixed function device.
29:24	Read/Write	110111b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to Other | Mobile Lid-Inside.
23:20	Read/Write	Dh	**Default Device (DD):** Indicates the intended use of the connection is for Digital In.
19:16	Read/Write	6h	**Connection Type (CTYP):** Indicates the type of physical connection is Other Digital.
15:12	Read/Write	0h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color for an internal connection is Unknown.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	3h	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all '0's is reserved. A value of all '1's in this field indicates that the Association has the lowest priority.
3:0	Read/Write	Eh	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.12.6 Digital Mic In 2 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 12h	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 12h	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 12h	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 12h	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 12h	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	10b	**Port Connectivity (PCON):** The port complex is connected to a fixed function device.
29:24	Read/Write	110111b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to Other | Mobile Lid-Inside.
23:20	Read/Write	Dh	**Default Device (DD):** Indicates the intended use of the connection is for Digital In.
19:16	Read/Write	6h	**Connection Type (CTYP):** Indicates the type of physical connection is Other Digital.
15:12	Read/Write	0h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color for an internal connection is Unknown.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	5h	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all '0's is reserved. A value of all '1's in this field indicates that the Association has the lowest priority.
3:0	Read/Write	Eh	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.12.7 Amplifier Gain/Mute

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DigMic 1 Node ID=0Eh DigMic 2 Node ID=12h	Verb ID = Bh	Payload = xxxxh

Bits [19:16] = 'Bh', where bits [15:0] are defined below:

Bits [15:0]	Value	Description
15	0b	**Get Output/Input (GOI):** This bit controls whether the request is for the input amplifier or the output amplifier. When '1', the output amplifier is being requested. When '0', the input amplifier is being requested.
14	0b	'0'b
13	xb	**Get Left/Right (GLR):** This bit controls whether the request is for the left channel amplifier or the right channel amplifier. When '1', the left channel amplifier is being requested. When '0', the right channel amplifier is being requested.
12:4	000000000b	Reserved
3:0	0000b	**Index (IDX):** This field specifies the input index of the amplifier setting to return if the widget has multiple input amplifiers. This field has no meaning and ignored since the widget does not have multiple input amplifiers. It should be always '0's.

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Amplifier Mute (AM):** Mute is not supported by this widget.
6:0	Read Only	0000000b	**Amplifier Gain (AG):** This field returns the Gain setting for the amplifier requested. If the amplifier requested does not exist, all '0's will be returned. Default equals 0 dB.

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	DigMic 1 Node ID=0Eh DigMic 2 Node ID=12h	Verb ID = 3h	Payload = xxxxh

Bits [19:16] = '3h', where bits [15:0] are defined below:

Bits	Type	Default	Description
15	Write Only	0b	**Set Output Amplifier (SOA):** This bit determines whether the value programmed refers to the output amplifier. This bit should always be '0' since an output amplifier is not present.
14	Write Only	xb	**Set Input Amplifier (SIA):** This bit determines whether the value programmed refers to the input amplifier. Set to 1 for the value to be accepted.
13	Write Only	xb	**Set Left Amplifier (SLA):** Selects the left channel (channel 0). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
12	Write Only	xb	**Set Right Amplifier (SRA):** Selects the right channel (channel 1). A 1 indicates that the relevant amplifier should accept the value being set. If both bits are set, both amplifiers are set.
11:8	Write Only	0000b	**Index (IDX):** This field is used when programming the input amplifiers on Selector Widgets and Sum Widgets. This field is ignored.
7	Write Only	0b	**Mute (MUTE):** When '0', the Mute is inactive. This field is ignored.
6:0	Write Only	xxxxxxxb	**Gain (GAIN):** Specifies the amplifier gain in dB. xxxxx00b = 0 dB xxxxx01b = +10 dB xxxxx10b = +20 dB xxxxx11b = not used Bits(6:2) are not used and are ignored.

6.13 S/PDIF Receiver Input Pin Widget (Node ID = 0Fh)

6.13.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	4h	**Type (TYP):** Pin Complex Widget
19:16	Read Only	1h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	1b	**Power Control (PC):** Power State control is supported on this widget.
9	Read Only	1b	**Digital (DIG):** Widget is a digital widget.
8	Read Only	0b	**Connection List (CL):** A connection list is not present on this widget.
7	Read Only	1b	**Unsolicited Capable (UC):** Unsolicited Response is supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.13.2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.
15:8	Read Only	00h	**VREF Control (VREFC):** VREF not supported.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	0b	**Balanced I/O Pins (BIOP):** This widget does not have balanced I/O pins.
5	Read Only	1b	**Input Capable (INC):** Widget is input capable.
4	Read Only	0b	**Output Capable (OUTC):** Is not output capable.
3	Read Only	0b	**Headphone Drive Capable (HDC):** Widget is not capable of driving headphones directly.
2	Read Only	1b	**Presence Detect Capable (PDC):** This bit is '1' to indicate that the widget is capable of performing presence detect.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.
0	Read Only	0b	**Impedance Sense Capable (ISC):** A '0' indicates that the widget does not support impedance sense on the attached peripheral.

6.13.3 Supported Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F00h	Parameter ID = 0Fh

Response Format:

Bits	Type	Default	Description
31	Read Only	1b	**EPSS:** Converter widget supports extended power states.
30:4	Read Only	0000000h	Reserved
3	Read Only	1b	**D3Sup:** D3hot operation is supported.
2	Read Only	0b	**D2Sup:** D2 operation is not supported.
1	Read Only	0b	**D1Sup:** D1 operation is not supported.
0	Read Only	1b	**D0Sup:** D0 operation is supported.

6.13.4 Power States

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F05h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = 705h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:11	Read Only	00000h	Reserved
10	Read Only	1b	**Power State Settings Reset (PS-SettingsReset):** This bit is set to '1'b when, during any type of reset or low power state transition, the settings within this widget that were changed from the defaults, either by software or hardware, have been reset back to their default state. When these settings have not been reset, this is reported as '0'b. This bit is always a '1'b following a POR condition. For more information, see "Power State Settings Reset (PS-SettingsReset)" on p 28
9	Read Only	0b	Reserved
8	Read Only	0b	**Power State Error (PS-Error):** This bit is not supported and will always return '0'b when read.
7:4	Read Only	0011b	**Power State Actual (PS-Act):** This field indicates the actual power state of the referenced node. The default state is D3.
3:0	Read/Write	0011b	**Power State Set (PS-Set):** Writes to these bits set the Audio Function Group to the Power State as described below: PSS = '0000'b; D0 - Fully on. PSS = '0001'b; D1 - Not Supported PSS = '0010'b; D2 - Not Supported PSS = '0011'b; D3 - Allows for lowest possible power consumption under software control. See "D3 Lower Power State Support" on page 26 for more information. PSS = '0100'b; D4 - Not Supported

PS-Set is a PowerState field which defines the current power setting of the referenced node. Since this node is of type other than an Audio Function Group node, the actual power state is a function of both this setting and the PowerState setting of the Audio Function Group node under which this node was enumerated (is controlled).

PS-Act is a PowerState field which indicates the actual power state of this node. Within the Audio Function Group node, this field will always be equal to the PS-Set field (modulo the time required to execute a power state transition). Within this type of node, this field will be the lower power consuming state of either a) the PS-Set field of the currently referenced node or b) the PS-Set field of the Audio Function Group node under which the currently referenced node was enumerated (is controlled).

6.13.5 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**H-Phone Enable (HPE)**: Not supported on this widget.
6	Read Only	0b	**Output Enable (OUTE)**: Not supported on this widget.
5	Read/Write	0b	**Input Enable (INE)**: This bit has no effect on the input path. Per HD Audio Spec., when '1', this bit enables the input path of the Pin Widget. When '0', the input path of the Pin Widget is shut off.
4:3	Read Only	00b	Reserved
2:0	Read Only	000b	**VREF Enable (VREFE)**: VREF is not supported on this widget. These bits are ignored and always report '000'.

6.13.6 Unsolicited Response Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F08h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = 708h	Payload = xxh

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Function Group Reset:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read/Write	0b	**Enable:** Determines if a change in receiver lock status will generate an Unsolicited Response (0 = No, 1 = Yes). If enabled, and the lock status changes from "LOCK" to "UNLOCK" or "UNLOCK" to "LOCK", an unsolicited response will be sent. The default value after cold or register reset for this register (0b) specifying no unsolicited response.
6	Read Only	0b	Reserved

Bits	Type	Default	Description
5:0	Read/Write	000000b	**Tag:** Is a 6-bit value assigned and used by software to determine what codec node generated the unsolicited response. The value programmed into the Tag field is returned in the top 6 bits (31:26) of every Unsolicited Response generated by this node.

Unsolicited Response Format:

Bits [31:26]	Bits [25:0]
Tag	Response

6.13.7 Pin Sense

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F09h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = 709h	Payload = xxh

Get Response Format:

Bits	Type	Default	Description
31	Read Only	0b	**Presence Detect (PDET)**: A ‘1’ indicates that there is “something” plugged into the jack associated with the Pin Widget. A ‘0’ indicates that nothing is plugged in.
30:0	Read Only	0	**Impedance Sense (IMPS)**: Not valid since the widget is not capable of impedance sensing.

Pin Sense Execute Format:

Bits	Type	Default	Description
7:1	Write Only	0000000b	Reserved
0	Write Only	0b	**Right Channel (RCHAN):** A write to this bit is ignored since the widget is not capable of impedance sensing.

6.13.8 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 0Fh	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 0Fh	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 0Fh	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 0Fh	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	00b	**Port Connectivity (PCON):** The port complex is connected to a jack.
29:24	Read/Write	000010b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to External | Front.
23:20	Read/Write	Ch	**Default Device (DD):** Indicates the intended use of the connection is for S/PDIF In.
19:16	Read/Write	4h	**Connection Type (CTYP):** Indicates the type of physical connection is RCA jack.
15:12	Read/Write	Eh	**Color (COL):** This field indicates the color of the physical jack for use by software. The color selected is White.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	Fh	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all ‘0’s is reserved. A value of all ‘1’s in this field indicates that the Association has the lowest priority.
3:0	Read/Write	0h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.14 S/PDIF Transmitter 1, S/PDIF Transmitter 2 Output Pin Widgets (Node ID = 10h, 15h)

6.14.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=10h S/P Tx 2 Node ID=15h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	4h	**Type (TYP):** Pin Complex Widget
19:16	Read Only	1h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	0b	**Power Control (PC):** Power State control is not supported on this widget.
9	Read Only	1b	**Digital (DIG):** Widget is a digital widget.
8	Read Only	1b	**Connection List (CL):** A connection list is present on this widget.
7	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Output amplifier is not present for this widget.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	1b	**Stereo (ST):** A 1 indicates a stereo widget.

6.14.2 Pin Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=10h S/P Tx 2 Node ID=15h	Verb ID = F00h	Parameter ID = 0Ch

Response Format:

Bits	Type	Default	Description
31:17	Read Only	0	Reserved
16	Read Only	0b	**EAPD Capable (EAPDC):** This widget does not support EAPD.
15:8	Read Only	00h	**VREF Control (VREFC):** VREF not supported.
7	Read Only	0b	**HDMI Capable (HDMIC):** This widget is not capable of supporting HDMI.
6	Read Only	0b	**Balanced I/O Pins (BIOP):** This widget does not have balanced I/O pins.
5	Read Only	0b	**Input Capable (INC):** Widget is not input capable.
4	Read Only	1b	**Output Capable (OUTC):** This bit is '1' to indicate that the widget is output capable.
3	Read Only	0b	**Headphone Drive Capable (HDC):** Widget is not capable of driving headphones directly.
2	Read Only	0b	**Presence Detect Capable (PDC):** This bit is '0' to indicate that the widget is not capable of performing presence detect to determine whether there is anything plugged in.
1	Read Only	0b	**Trigger Required (TR):** Trigger is not required for an impedance measurement.
0	Read Only	0b	**Impedance Sense Capable (ISC):** This bit is '0' to indicate that the widget does not support impedance sense on the attached peripheral.

6.14.3 Connection List Length

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=10h S/P Tx 2 Node ID=15h	Verb ID = F00h	Parameter ID = 0Eh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**Long Form (LF):** Connection list is short form.
6:0	Read Only	0000001b	**Connection List Length (CLL):** One hard-wired input for this widget.

6.14.4 S/PDIF Transmitter 1 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 10h	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	00h	**Connection List Entry (N+1):** Returns 00h for N=00h-03h or N>03h.
7:0	Read Only	08h	**Connection List Entry (N):** Returns 08h (S/PDIF Out 1) for N=00h-03h. Returns 00h for N>03h.

6.14.5 S/PDIF Transmitter 2 Connection List Entry

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 15h	Verb ID = F02h	Payload = N = xxh

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	**Connection List Entry (N+3):** Returns 00h for N=00h-03h or N>03h.
23:16	Read Only	00h	**Connection List Entry (N+2):** Returns 00h for N=00h-03h or N>03h.
15:8	Read Only	00h	**Connection List Entry (N+1):** Returns 00h for N=00h-03h or N>03h.
7:0	Read Only	14h	**Connection List Entry (N):** Returns 14h (S/PDIF Out 2) for N=00h-03h. Returns 00h for N>03h.

6.14.6 Pin Widget Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=10h S/P Tx 2 Node ID=15h	Verb ID = F07h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	S/P Tx 1 Node ID=10h S/P Tx 2 Node ID=15h	Verb ID = 707h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7	Read Only	0b	**H-Phone Enable (HPE)**: Not supported.
6	Read/Write	0b	**Output Enable (OUTE)**: This bit has no effect on the output path. Per HD Audio Spec., when '1', this bit enables the output path of the Pin Widget. When '0', the output path is shut off.
5	Read Only	0b	**Input Enable (INE)**: Set to '0' since there is no input path associated with the pin widget.
4:3	Read Only	00b	Reserved
2:0	Read Only	000b	**VREF Enable (VREFE)**: The Pin Widget does not support VREF generation as indicated in the Pin Capabilities. As such, this field should always be "000b" to select the Hi-Z state.

6.14.7 S/PDIF Transmitter 1 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 10h	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 10h	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 10h	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 10h	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 10h	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	00b	**Port Connectivity (PCON):** The port complex is connected to a jack.
29:24	Read/Write	000001b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to External | Rear.
23:20	Read/Write	4h	**Default Device (DD):** Indicates the intended use of the connection is for S/PDIF Out.
19:16	Read/Write	4h	**Connection Type (CTYP):** Indicates the type of physical connection is RCA jack.
15:12	Read/Write	6h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color selected is Orange.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	Fh	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all ‘0’s is reserved. A value of all ‘1’s in this field indicates that the Association has the lowest priority.
3:0	Read/Write	0h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.14.8 S/PDIF Transmitter 2 Configuration Default

The Configuration Default register is used by software as an aid in determining the configuration of jacks and devices attached to the codec. At the time the codec is first powered on, this register is internally loaded with default values indicating the typical system use of this particular pin/jack. After this initial loading, it is completely codec opaque, and its state, including any software writes into the register, must be preserved across reset events such as Link Reset or Codec Reset (the Function Reset Verb). Its state need not be preserved across power level changes.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 15h	Verb ID = F1Ch	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 15h	Verb ID = 71Ch	Payload = xxh (Config bits [7:0])
CAd = X	Node ID = 15h	Verb ID = 71Dh	Payload = xxh (Config bits [15:8])
CAd = X	Node ID = 15h	Verb ID = 71Eh	Payload = xxh (Config bits [23:16])
CAd = X	Node ID = 15h	Verb ID = 71Fh	Payload = xxh (Config bits [31:24])

Response Format:

Bits [31:0] are sticky and will not be reset by a Link Reset or a Codec Reset:

Bits	Type	Default	Description
31:30	Read/Write	00b	**Port Connectivity (PCON):** The port complex is connected to a jack.
29:24	Read/Write	000001b	**Location (LOC):** This field indicates the physical location of the jack or device to which the pin complex is connected. Set to External | Rear.
23:20	Read/Write	4h	**Default Device (DD):** Indicates the intended use of the connection is for S/PDIF Out.
19:16	Read/Write	5h	**Connection Type (CTYP):** Indicates the type of physical connection is Optical jack.
15:12	Read/Write	1h	**Color (COL):** This field indicates the color of the physical jack for use by software. The color selected is Black.
11:8	Read/Write	0h	**Miscellaneous (MISC):** No PDC override.
7:4	Read/Write	Fh	**Default Association (DA):** This field is used by software to group Pin Complex (and therefore jacks) together into functional blocks to support multichannel operation. All jacks with the same association number may be assumed to be grouped together. A value of all ‘0’s is reserved. A value of all ‘1’s in this field indicates that the Association has the lowest priority.
3:0	Read/Write	0h	**Sequence (SEQ):** This field indicates the order of the jacks in the association group.

6.15 Vendor Processing Widget (Node ID = 11h)

6.15.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 11h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	Fh	**Type (TYP):** Vendor Defined Widget
19:16	Read Only	0h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	0b	**Power Control (PC):** Power State control is not supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	0b	**Connection List (CL):** Connection list is not present.
7	Read Only	0b	**Unsolicited Capable (UC):** Not supported.
6	Read Only	1b	**Processing Widget (PW):** Widget does contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** Set to ‘0’ to indicate that the widget does not contain format information.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Not present.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	0b	**Stereo (ST):** A 0 indicates not supported.

6.15.2 Processing Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 11h	Verb ID = F00h	Parameter ID = 10h

Response Format:

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15:8	Read Only	16h	**NumCoeff:** Number of coefficients. There are a total of 22 registers.
7:1	Read Only	0000000b	Reserved
0	Read Only	0b	**Benign:** This processing widget is not linear and time invariant.

6.15.3 Processing State

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 11h	Verb ID = F03h	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 11h	Verb ID = 703h	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:0	Read/Write	00h	**HDA Defined Processing State:** Writes to these bits set the Widget to the processing state as described below: '00'h; Processing Off. '01'h; Processing On. '02'h; Processing Benign. Benign state is not supported. Will be treated as "Processing Off". '03'h - '7F'h; - Reserved

6.15.4 Coefficient Index

The **Coefficient Index** is a zero-based index into the processing coefficient list which will be either read or written using the Processing Coefficient control. When the coefficient has been read or written to, the Coefficient Index will automatically increment by one so that the next Set Processing Coefficient verb will load the coefficient into the next slot. The auto-increment feature can be disabled by setting the Disable Coefficient Index Auto-Increment bit in the DAC Configuration (CIR = 0003h) register. The auto-increment feature will "wrap around" at a Coefficient Index value of 04h, that is an index of 04h will be auto-incremented to an index of 00h. If Coefficient Index is set to be greater than the number of "slots" in the processing coefficient list, unpredictable behavior will result if an attempt is made to Get or Set the processing coefficient.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 11h	Verb ID = Dh	Payload = 0000h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 11h	Verb ID = 5h	Payload = xxxxh

Response Format:

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15:0	Read/Write	0000h	**Index n:** Coefficient Index value.

6.15.5 Processing Coefficient

Processing Coefficient loads the value *n* into the widget's coefficient array at the index determined by the Coefficient Index control. When the coefficient has been read or written to, the Coefficient Index will automatically increment by one so that the next Set Processing Coefficient verb will load the coefficient into the next slot.

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 11h	Verb ID = Ch	Payload = 0000h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:16]	Bits [15:0]
CAd = X	Node ID = 11h	Verb ID = 4h	Payload = xxxxh

Response Format:

Bits	Type	Default	Description
31:16	Read Only	0000h	Reserved
15:0	Read/Write	0000h	**Value n:** The value n of the 16 bit coefficient to set.

6.15.6 Coefficient Registers

Processing Coefficient loads the 16-bit value *n* into the widget's coefficient array at the index determined by the Coefficient Index control. When the coefficient has been loaded, the Coefficient Index will automatically increment by one so that the next Set Processing Coefficient verb will load the coefficient into the next slot.

Coefficient Index Register Summary:

Coefficient Index Register (CIR)	Description
0000h	S/PDIF RX/TX Interface Status
0001h	S/PDIF RX/TX Interface Control
0002h	ADC Configuration
0003h	DAC Configuration
0004h	Beep Configuration

6.15.6.1 S/PDIF RX/TX Interface Status (CIR = 0000h)

Bits	Type	Default	Description
15:10	Read Only	0	Reserved
9	Read Only	0b	**192 kHz Recovered Sample Rate** - Measured audio sample rate of incoming S/PDIF data. A '1'b indicates a 192 kHz sample rate.
8	Read Only	0b	**96 kHz Recovered Sample Rate** - Measured audio sample rate of incoming S/PDIF data. A '1'b indicates a 96 kHz sample rate.
7	Read Only	0b	**48 kHz Recovered Sample Rate** - Measured audio sample rate of incoming S/PDIF data. A '1'b indicates a 48 kHz sample rate.
6	Read Only	0b	**44.1 kHz Recovered Sample Rate** - Measured audio sample rate of incoming S/PDIF data.A '1'b indicates a 44.1 kHz sample rate.
5	Read Only	0b	**32 kHz Recovered Sample Rate** - Measured audio sample rate of incoming S/PDIF data. A '1'b indicates a 32 kHz sample rate.
4	Read Only	0b	**CCRC** - Channel Status Block Cyclic Redundancy Check bit. Updated on CS block boundaries, valid only in Pro mode. This bit will go high on occurrence of the error, and will stay high until the register is read. Reading the register resets this bit to 0, unless the error condition is still true. 0 - No error. 1 - Error.
3	Read Only	0b	**BIP** - Bi-phase error bit. Updated on sub-frame boundaries. This bit will go high on occurrence of the error, and will stay high until the register is read. Reading the register resets this bit to 0, unless the error condition is still true. 0 - No error. 1 - Bi-phase error. This indicates an error in the received bi-phase coding.
2	Read Only	0b	**PAR** - Parity bit. Updated on sub-frame boundaries. This bit will go high on occurrence of the error, and will stay high until the register is read. Reading the register resets this bit to 0, unless the error condition is still true. 0 - No error. 1 - Parity error.
1	Read Only	0b	**SPUL** - S/PDIF Receiver Unlock Indicator 1 - The receiver is unlocked or has transition-ed from lock to unlock since the last read. 0 - The receiver is locked and has not transitioned from lock to unlock since the last read.
0	Read Only	0b	**SPL** - S/PDIF Receiver Lock Indicator 1 - The receiver is locked or has transition-ed from unlock to lock since the last read. 0 - The receiver is unlocked and has not transition-ed from unlock to lock since the last read.

6.15.6.2 S/PDIF RX/TX Interface Control (CIR = 0001h)

Bits	Type	Default	Description
15	Read Only	0b	Reserved
14	Read/Write	0b	**TX 2 Enable:** Routes S/PDIF Transmitter 2 to the GPIO1/DMIC_SDA2/SPDIF_OUT2 pin. 0 - The pin functions as GPIO1 or DMIC_SDA2, according to **DMIC2 Enable**. 1 - The pin functions as SPDIF_OUT2, regardless of **DMIC2 Enable**.
13	Read/Write	0b	Reserved
12	Read/Write	0b	**TX 2 Raw Data Mode**: Enables AES3 Direct Mode. In this mode, a direct copy of the received NRZ data from the HD Audio bus is sent to S/PDIF transmitter 2. 0 - Normal S/PDIF TX 2 Data Mode. 1 - Enable Raw S/PDIF TX 2 Data Mode.
11	Read/Write	0b	**RX To TX 2 Loopthru**: This bit is used to enable an internal loop through from the S/PDIF RX to S/PDIF TX 2. The path is a straight digital mux from input to output. No re-clocking is performed. 0 - Do not loop S/PDIF RX to S/PDIF TX 2. 1 - Enable S/PDIF RX to S/PDIF TX 2 loopthru.
10	Read/Write	0b	**RX A/B Chnl Status Select:** Specifies the channel from which to extract the channel status bits. ‘0’b - Select channel A status. ‘1’b - Select channel B status.
9:8	Read/Write	00b	Reserved
7	Read/Write	0b	**TX 1 Raw Data Mode**: Enables AES3 Direct Mode. In this mode, a direct copy of the received NRZ data from the HD Audio bus is sent to S/PDIF transmitter 1. 0 - Normal S/PDIF TX 1 Data Mode. 1 - Enable Raw S/PDIF TX 1 Data Mode.
6	Read/Write	0b	**RX Raw Data Mode**: Enables AES3 Direct Mode. In this mode, a direct copy of the received NRZ data from the S/PDIF receiver including the C, U, and V bits are transmitted to the HD Audio bus. The time slot occupied by the Z bit is used to indicate the location of the block start. 0 - Normal S/PDIF RX Data Mode. 1 - Enable Raw S/PDIF RX Data Mode.
5	Read/Write	0b	**RX To TX 1 Loopthru**: This bit is used to enable an internal loop through from the S/PDIF RX to S/PDIF TX 1. The path is a straight digital mux from input to output. No re-clocking is performed. 0 - Do not loop S/PDIF RX to S/PDIF TX 1. 1 - Enable S/PDIF RX to S/PDIF TX 1 loopthru.

Bits	Type	Default	Description
4:3	Read/Write	01b	**HOLD[1:0]** – Determines how received AES3 audio sample is affected when an receive error occurs. The errors that affect hold behavior are parity, bi-phase and confidence. HOLD has no effect in Raw S/PDIF RX Data Mode. 00 - hold last audio sample. 01 - replace the current audio sample with all zeros (mute). 10 - do not change the received audio sample. 11 - reserved
2	Read/Write	0b	**TRUNC** – Determines if the audio word length is set according to the incoming channel status data as decoded by the AUX[3:0] bits. The resulting word length in bits is 24 minus AUX[3:0]. The TRUNC function is valid only on PCM audio data. 0 – Incoming data is not truncated. 1 – Incoming data is truncated according to the length specified in the channel status data. TRUNC has no effect on output data if detected as being non-audio.
1	Read/Write	0b	**SRC_MUTE** – When SRC_MUTE is set to '1', the SRC will soft-mute when it loses lock and soft unmute when it regains lock. 0 - Soft mute disabled 1 - Soft mute enabled
0	Read/Write	0b	Reserved

6.15.6.3 ADC Configuration (CIR = 0002h)

Bits	Type	Default	Description
15	Read/Write	0b	**URG (Unsolicited Response Gating):** This bit allows unsolicited responses to be gated. 0 - Normal propagation of unsolicited responses. 1 - Unsolicited responses are gated if AFG is in D3.
14	Read/Write	0b	**ADC2 Gain:** This bit adjusts the gain of the Mic In 1/Line In 2 path for the given input topology. 0 - 6 dB gain added (pseudo-differential and single-ended mode). 1 - no gain added (fully differential mode). *Note: This bit is OR'ed with the **BTL** bit in the* Mic In 1/Line In 2 EAPD/BTL Enable *Control.*
13	Read/Write	0b	**ADC1 Gain:** This bit adjusts the gain of the Line In 1/Mic In 2 path for the given input topology. 0 - 6 dB gain added (pseudo-differential and single-ended mode). 1 - no gain added (not supported - test only).

Bits	Type	Default	Description
12:11	Read/Write	00b	**ADC2 Channel Mode[1:0]:** Controls the channel mapping from the ADC2 output to the HDA bus. ‘00’b - ADC2 left channel is mapped to HDA left channel and ADC2 right channel is mapped HDA right channel (normal mode). ‘01’b - ADC2 left channel is mapped to both HDA left and right channels. ADC2 right channel is discarded (mono mode). ‘10’b - ADC2 right channel is mapped to both HDA left and right channels. ADC2 left channel is discarded (alternate mono mode). ‘11’b - ADC2 left channel is mapped to HDA right channel and ADC2 right channel is mapped to HDA left channel (channel swap mode).
10:9	Read/Write	00b	**ADC1 Channel Mode[1:0]:** Controls the channel mapping from the ADC1 output to the HDA bus. ‘00’b - ADC1 left channel is mapped to HDA left channel and ADC1 right channel is mapped HDA right channel (normal mode). ‘01’b - ADC1 left channel is mapped to both HDA left and right channels. ADC1 right channel is discarded (mono mode). ‘10’b - ADC1 right channel is mapped to both HDA left and right channels. ADC1 left channel is discarded (alternate mono mode). ‘11’b - ADC1 left channel is mapped to HDA right channel and ADC1 right channel is mapped to HDA left channel (channel swap mode).
8:6	Read/Write	000b	Reserved
5	Read/Write	0b	**ADC2 PGA Mode:** Sets the topology for the Mic In 1/Line In 2 PGA. 0 - Fully differential or pseudo-differential mode. 1 - Single-ended mode.
4	Read/Write	0b	**ADC1 PGA Mode:** Sets the topology for the Line In 1/Mic In 2 PGA. 0 - Pseudo-differential mode. 1 - Single-ended mode.
3:2	Read/Write	10b	**ADC2 SZCMode[1:0]:** Same function as ADC1. See below.

Bits	Type	Default	Description
1:0	Read/Write	10b	**ADC1 SZCMode[1:0]:** Sets the mode by which analog PGA and digital volume, and muting changes will be implemented. See "Input Amplifier Capabilities" section on page 55 regarding digital and analog volume ranges. '00'b - Immediate Change: When immediate change is selected, all level changes will take effect immediately in one step '01'b - Digital Immediate and Analog Zero Cross: Dictates that signal level changes, both muting and gain/attenuation, will occur immediately for digital volume changes, and on a signal zero crossing for analog volume changes to minimize audible artifacts. The requested level change will occur after a timeout period of 1024/Fs (approx. 21 ms @ Fs = 48 kHz) if the signal does not encounter a zero crossing. '10'b - Digital Soft Ramp and Analog Soft Ramp: Allows level changes, both muting and gain/attenuation, to be implemented by incrementally ramping at a rate of 1/8 dB per audio sample period for digital volume changes, and at a rate of 1 dB per 8 audio sample periods for analog volume changes. If the analog PGA is being used for +10 dB "boost" function, or the Digital Mic is being used, then the digital soft ramp gain range will be from +12 dB to -51 dB, and analog soft ramp will not be used. '11'b - Digital Soft Ramp and Analog Zero Cross: Allows level changes, both muting and gain/attenuation, to be implemented by incrementally ramping at a rate of 1/8 dB per audio sample period for digital volume changes. Analog volume changes are to be implemented on a signal zero crossing. The requested level change will occur after a timeout period of 1024/Fs (approx. 21 ms @ Fs = 48 kHz) if the signal does not encounter a zero crossing. If the analog PGA is being used for +10 dB "boost" function, or the Digital Mic is being used, then the digital soft ramp gain range will be from +12 dB to -51 dB and analog soft ramp will not be used. Both soft ramp and zero cross are independently monitored and implemented for each channel.

6.15.6.4 DAC Configuration (CIR = 0003h)

Bits	Type	Default	Description
15:13	Read/Write	000b	Reserved
12	Read/Write	1b	**Enable DACs High Pass Filter:** When set to '1'b, will enable a high pass filter to remove any DC component. '0'b - Disable HPF. '1'b - Enable HPF.
11	Read/Write	0b	**Power Down Internal References (PDREF):** When set to '1'b, will ramp the internal voltage references down. This should be used prior to removing operating voltages from the codec. '0'b - Normal Operation. '1'b - Power down internal references.
10	Read/Write	0b	**Disable Coefficient Index Auto-Increment:** Specifies if the Coefficient Index value will be automatically incremented following a read or write operation. Auto increment is supported by Vista OS. '0'b - auto increment coefficient index following a read or write. '1'b - do not auto increment coefficient index following a read or write.
9:7	Read/Write	000b	Reserved
6	Read/Write	1b	**Mute DAC Outputs on FIFO Error:** Specifies to force a Mute condition if an under-run or over-run condition occurs on the HD Audio FIFO memory. The transition to Mute will occur as per the settings of each of the DACx SZCMode bits. '0'b - Disable Mute DAC Outputs on FIFO Error. '1'b - Enable Mute DAC Outputs on FIFO Error.
5:4	Read/Write	10b	**DAC3 SZCMode[1:0]:** Same function as DAC1. See below.
3:2	Read/Write	10b	**DAC2 SZCMode[1:0]:** Same function as DAC1. See below.

Bits	Type	Default	Description
1:0	Read/Write	10b	**DAC1 SZCMode[1:0]:** Sets the soft ramp and zero crossing detection modes by which volume and muting changes will be implemented. ‘00’b - Immediate Change: When immediate change is selected, all level changes will take effect immediately in one step ‘01’b - Zero Cross: Dictates that signal level changes, both muting and gain/attenuation, will occur on a signal zero crossing to minimize audible artifacts. The requested level change will occur after a timeout period of 512/Fs (approximately 11 ms @ Fs = 48 kHz) if the signal does not encounter a zero crossing. ‘10’b - Soft Ramp: Allows level changes, both muting and gain/attenuation, to be implemented by incrementally ramping, in 1/8 dB steps, from the current level to the new level at a rate of 1/8 dB per audio sample period. ‘11’b - Soft Ramp on Zero Cross: Dictates that signal level changes, both muting and gain/attenuation, will occur in 1/8 dB steps and be implemented on a signal zero crossing. The 1/8 dB level change will occur after a timeout period of 512/Fs (approximately 11 ms @ Fs = 48 kHz) if the signal does not encounter a zero crossing. Both soft ramp and zero cross are independently monitored and implemented for each channel.

6.15.6.5 Beep Configuration (CIR = 0004h)

Bits	Type	Default	Description
15:5	Read Only	0	Reserved
4	Read/Write	0b	**DMIC2 Enable:** Specifies whether GPIO1 or Digital Mic Interface 2 is enabled. ‘0’b - GPIO1 enabled, Digital Mic 2 disabled. ‘1’b - Digital Mic 2 enabled, GPIO1 disabled.
3	Read/Write	0b	**DMIC1 Enable:** Specifies whether GPIO0 or Digital Mic Interface 1 is enabled. ‘0’b - GPIO0 enabled, Digital Mic 1 disabled. ‘1’b - Digital Mic 1 enabled, GPIO0 disabled.
2	Read/Write	1b	**DAC3 Beep Enable:** This bit allows the output from the beep generator to be passed to DAC3.
1	Read/Write	1b	**DAC2 Beep Enable:** This bit allows the output from the beep generator to be passed to DAC2.
0	Read/Write	1b	**DAC1 Beep Enable:** This bit allows the output from the beep generator to be passed to DAC1.

6.16 Beep Generator Widget (Node ID = 13h)

6.16.1 Audio Widget Capabilities

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 13h	Verb ID = F00h	Parameter ID = 09h

Response Format:

Bits	Type	Default	Description
31:24	Read Only	00h	Reserved
23:20	Read Only	7h	**Type (TYP):** Beep Generator Widget
19:16	Read Only	0h	**Delay (DLY):** Number of sample delays through the widget.
15:12	Read Only	0h	Reserved
11	Read Only	0b	**L-R Swap (LRS):** This widget is not capable of swapping the left and right channels.
10	Read Only	0b	**Power Control (PC):** Power State control is not supported on this widget.
9	Read Only	0b	**Digital (DIG):** Widget is not a digital widget.
8	Read Only	0b	**Connection List (CL):** A connection list is not present on this widget.
7	Read Only	0b	**Unsolicited Capable (UC):** Unsolicited Response is not supported on this widget.
6	Read Only	0b	**Processing Widget (PW):** This widget does not contain “Processing Controls” parameters.
5	Read Only	0b	**Stripe (STRP):** Striping is not supported.
4	Read Only	0b	**Format Override (FO):** This widget does not contain format information.
3	Read Only	0b	**Amplifier Parameter Override (APO):** This widget does not contain amplifier parameters.
2	Read Only	0b	**Output Amplifier Present (OAP):** Not present.
1	Read Only	0b	**Input Amplifier Present (IAP):** Input amplifier is not present for this widget.
0	Read Only	0b	**Stereo (ST):** Not supported.

6.16.2 Beep Generation Control

Get Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 13h	Verb ID = F0Ah	Payload = 00h

Set Parameter Command Format:

Bits [31:28]	Bits [27:20]	Bits [19:8]	Bits [7:0]
CAd = X	Node ID = 13h	Verb ID = 70Ah	Payload = xxh

Response Format:

Bits	Type	Default	Description
31:8	Read Only	000000h	Reserved
7:0	Read/Write	00h	**Divider:** When set to 0, beep generation is turned off. When set to any other value, beep generation is turned on and the frequency of the beep equals 12 kHz divided by this value.

7. APPLICATIONS

7.1 HD Audio Interface

7.1.1 Multi-Channel Streams

The CS4207 codec supports multi-channel streams (streams with sample blocks containing more than two samples), on both inbound and outbound frames. Each of the 5 output converter widgets (DAC1/2/3, S/PDIF TX 1/2) can be associated with an individual stream, or multiple widgets can be grouped to share the same stream. A mix of shared and individual streams is also supported. Furthermore, the order in which channels are assigned to each widget is not constrained by design. However, the following limitations exist and must be avoided:

- a stream cannot contain channels that are not associated with any widget (unused channels), unless those channels appear last within the stream packet, after all other channels
- the same channel cannot be associated with more than one widget

The same capabilities and limitations exist for the 3 input converter widgets (ADC1/2, S/PDIF RX). The following table gives some examples of valid and invalid stream formats:

Stream Format	DAC1	DAC2	DAC3	SPDO1	SPDO2	comment
{A,B} {C,D} {E,F} {G,H} {I,J}	A, B	C, D	E, F	G, H	I, J	indiv. streams, in-order assignment
{A, B, C, D, E, F, G, H, I, J}	A, B	C, D	E, F	G, H	I, J	shared stream, in-order assignment
{A, B, C, D} {E, F}	A, B	C, D	E, F	-	-	mixed shared and indiv. streams
{A, B} {C, D}	-	-	C, D	-	A, B	indiv. streams, out of order assignment
{A, B, C, D, E, F, G, H, I, J}	G, H	E, F	A, B	I, J	C, D	shared stream, out of order assignment
{A, B, C, D}	-	-	-	C, D	-	invalid: leading unused ch. (A, B)
{A, B, C, D, E, F, G, H, I, J}	A, B	E, F	G, H	I, J	-	invalid: intermittent unused ch. (C, D)
{A, B, C, D, E, F, G, H, I, J}	A, B	C, D	E, F	G, H	-	ok: trailing unused ch. (I, J)
{A, B, C, D}	A, B	C, D	-	A, B	-	invalid: ch. assigned to mult. widgets

Table 4. Stream Format Examples

The curly brackets { } delineate each stream packet. The letters within curly brackets designate each channel within that stream packet. For instance the sequence “{A, B, C, D} {E, F}” denotes two streams - one stream consisting of 4 channels A-D and one stream consisting of 2 channels E-F.

7.2 Analog Inputs

The analog inputs of the CS4207 can be configured as single-ended, pseudo-differential, or fully differential topologies. See Tables 5 and 6 for the register settings required to place the analog inputs into the appropriate topology. The ADC1 Gain, ADC2 Gain, ADC1 PGA Mode, and ADC2 PGA Mode bits are located in the ADC Configuration (CIR = 0002h) register of the Vendor Processing Widget (Node ID = 11h).

	ADC1 Gain	ADC1 PGA Mode	Figure
Single-Ended	0	1	11
Pseudo-Differential (default)	0	0	12

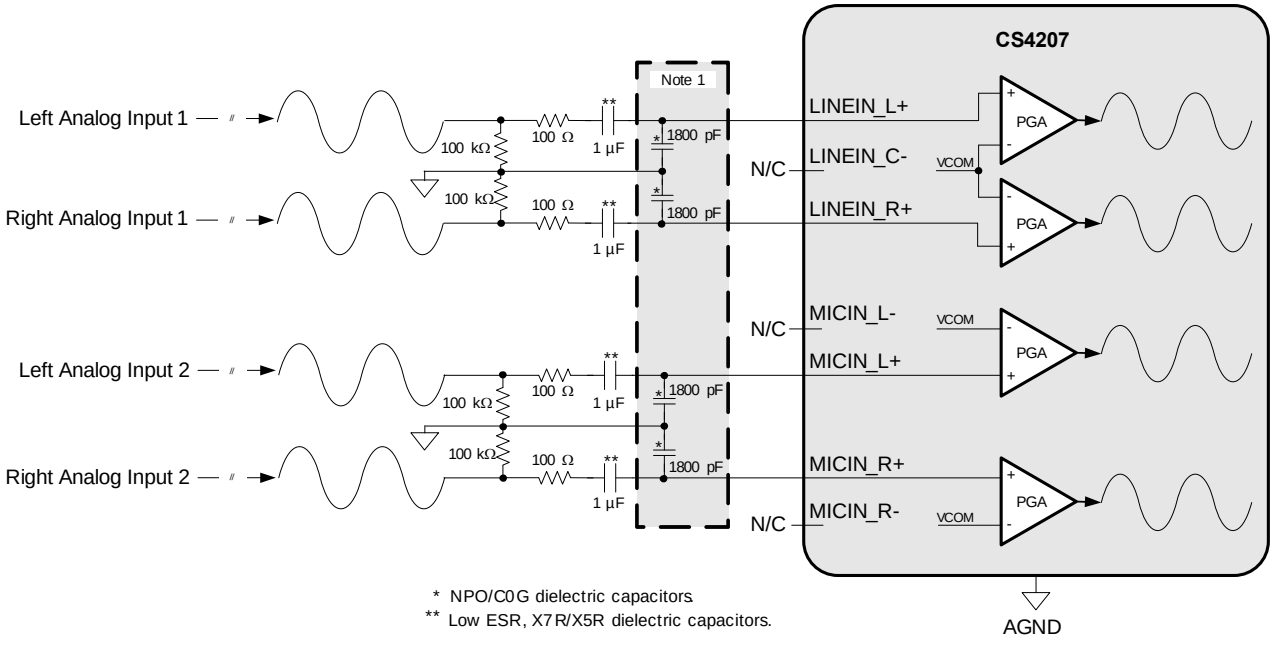
Table 5. Line In 1/Mic In 2 Input Topology Register Settings

	ADC2 Gain (Note:)	ADC2 PGA Mode	Figure
Single-Ended	0	1	11
Pseudo-Differential (default)	0	0	12
Fully Differential	1	0	13

Table 6. Mic In 1/Line In 2 Input Topology Register Settings

Note: Alternatively, the BTL bit in the Mic In 1/Line In 2 EAPD/BTL Enable control of the Mic In 1/Line In 2 Pin Widget (Node ID = 0Dh) may be set to '1'b to put ADC2 in fully differential mode.

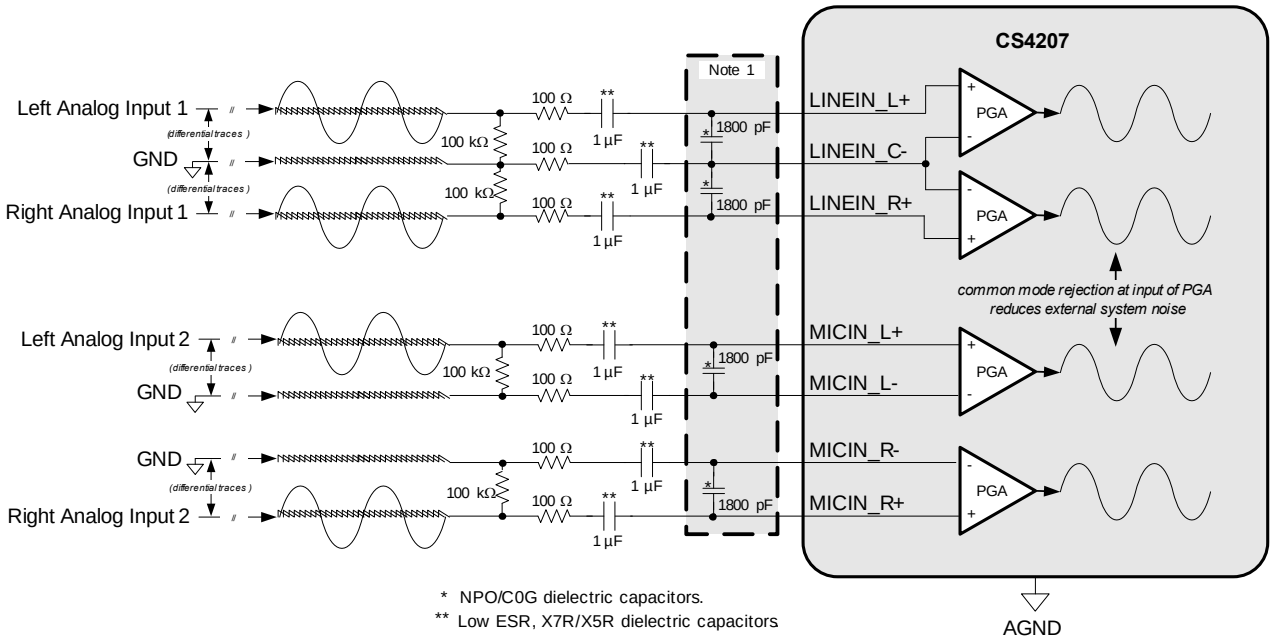
Both analog stereo input pairs may be used with single-ended line or microphone inputs. In this configuration the LINEIN_C-, MICIN_L-, and MICIN_R- pins are internally disconnected and should be left floating. See Figure 11 for the recommended single-ended input filter.



Note:
1. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators and should be placed as close as possible to the inputs

Figure 11. Single-Ended Input Filter

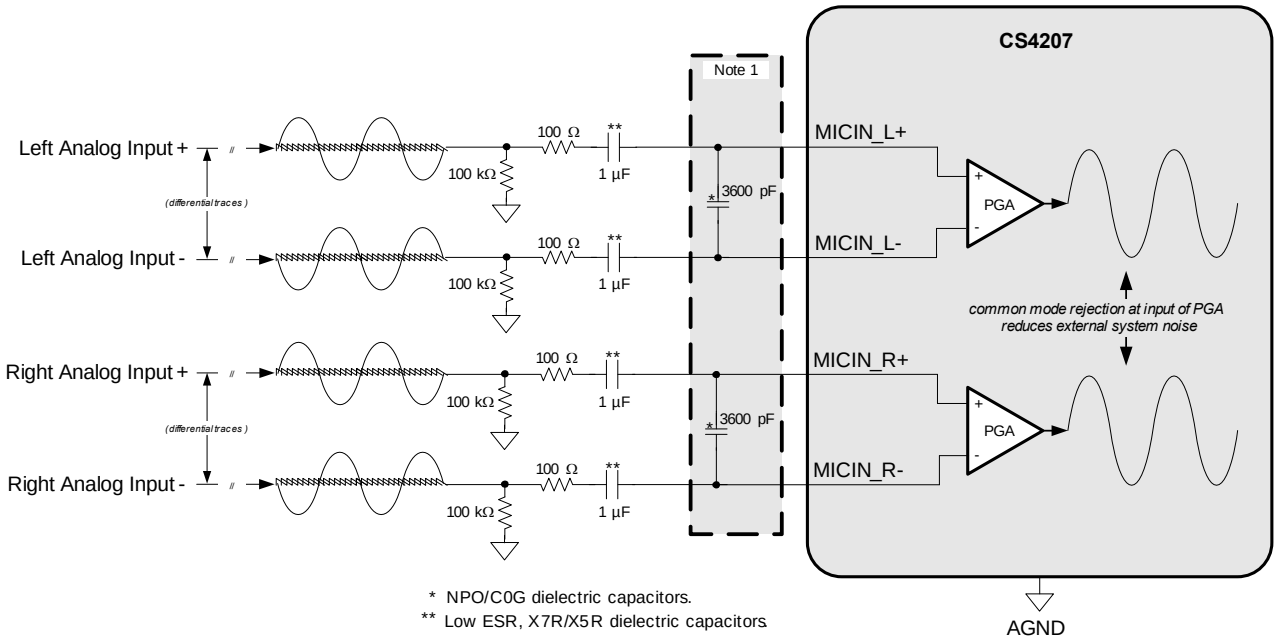
For an improvement from using the single-ended circuitry, both analog stereo input pairs may be configured in a pseudo-differential topology. This provides common-mode noise rejection for single-ended inputs by differentially routing LINEIN_C-, MICIN_L-, and/or MICIN_R- with the signal traces. See Figure 12 for the recommended pseudo-differential input filter.



Note:
1. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators and should be placed as close as possible to the inputs

Figure 12. Pseudo-Differential Input Filter

For the best ADC performance, fully differential inputs can be connected to the Mic In 1/Line In 2 input pair only. This topology provides the best common-mode noise rejection and also increases the dynamic range due to the larger full-scale input voltage. See Figure 13 for the recommended differential input filter.



Note:
1. These capacitors serve as a charge reservoir for the internal switched capacitor ADC modulators and should be placed as close as possible to the inputs

Figure 13. Differential Input Filter

For all of the input topologies, either input pair can be used with a microphone input by connecting the MICBIAS pin to the signals as shown in Figure 1. If electrolytic capacitors are used for AC coupling the microphone inputs, the positive terminal of the capacitor must be connected to the greater bias voltage. The analog input pins are internally biased at 0.5*VA and the voltage level of the MICBIAS pin can be configured by setting the VREFE bits in the Mic In 1/Line In 2 Pin Widget Control of the Mic In 1/Line In 2 Pin Widget (Node ID = 0Dh).

7.3 Analog Outputs

7.3.1 Output Filter

The Cirrus Application Note titled *Design Notes for a 2-Pole Filter with Differential Input*, available as AN48 at www.cirrus.com, discusses the second-order Butterworth filter and differential-to-single-ended converter that was implemented on the CDB4207 evaluation board. Figure 14 illustrates this implementation. If only single-ended outputs from the CS4207 are required, the passive output filter shown in Figure 15 can be used.

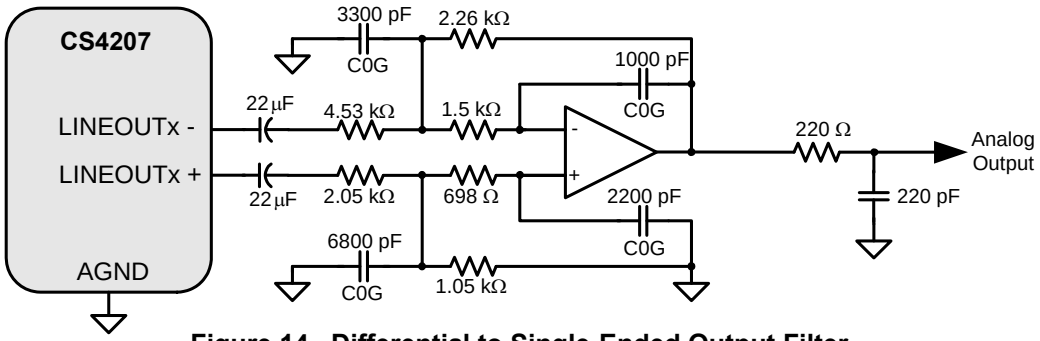


Figure 14. Differential to Single-Ended Output Filter

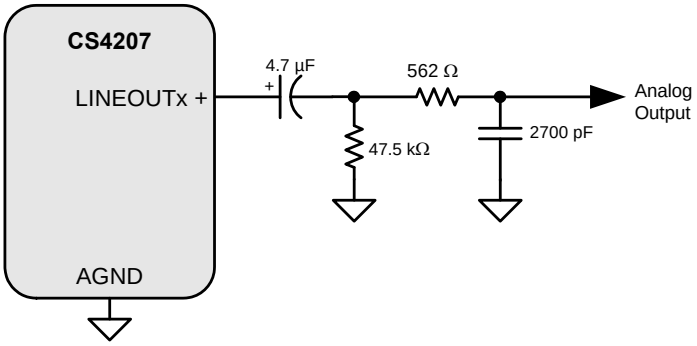


Figure 15. Passive Single-Ended Output Filter

7.3.2 Analog Supply Removal

In order to reduce audible artifacts, the analog reference is always powered up, even if the AFG has been transitioned into D3 state. For maximum power savings during D3, it may be desirable to completely remove the analog supplies on the system level. Doing so would cause an uncontrolled discharge of the internal reference and hence audible artifacts, and must therefore be preceded with a controlled reference ramp-down, which is initiated by setting the PDREF bit in the DAC Configuration (CIR = 0003h) register of the Vendor Processing Widget (Node ID = 11h).

7.4 Digital Mic Inputs

For each ADC, the data from the digital mic input pin widgets are multiplexed with the data from the analog line/mic input pin widgets, and only one pin widget can be selected at any given time. Furthermore, the data pins for the DMIC interface (DMIC_SDA1/2) are multiplexed with the GPIO0/1 pins and default to GPIO. In order to successfully setup the data path for a digital microphone, the following steps have to be followed:

1. clear the **TX 2 Enable** bit in the S/PDIF RX/TX Interface Control (CIR = 0001h) register of the Vendor Processing Widget (Node ID = 11h) (only required for DMIC2)

2. set the **DMIC1 Enable** and/or **DMIC2 Enable** bit in the Beep Configuration (CIR = 0004h) register of the Vendor Processing Widget (Node ID = 11h)
3. set the **INE** bit in the Pin Widget Control of the Digital Mic In 1 Pin Widget (Node ID = 0Eh) and/or the Digital Mic In 2 Pin Widget (Node ID = 12h)
4. for DMIC1 set the **Connection Index** in the ADC2 Connection Select Control of the ADC2 Input Converter Widget (Node ID = 06h) to a value of 01h
5. for DMIC2 set the **Connection Index** in the ADC1 Connection Select Control of the ADC1 Input Converter Widget (Node ID = 05h) to a value of 01h

The clock signal for the DMIC interface (DMIC_SCL) will be enabled if at least one of the DMIC data paths has been configured as described above.

7.5 S/PDIF Input and Outputs

7.5.1 S/PDIF Receiver SRC

The S/PDIF Receiver SRC is used to sample-rate convert incoming source-synchronous data to HDA bus-synchronous data. The SRC can only convert rates that are close to one another, therefore, software must monitor the Recovered Sample Rate in the S/PDIF RX/TX Interface Status (CIR = 0000h) register and program the Converter Format Control of the S/PDIF Receiver Input Converter Widget (Node ID = 07h) accordingly.

The S/PDIF Receiver SRC is on by default and will be turned off if at least one of the following conditions is true:

- TYPE (bit 15) in the Converter Format Control of the S/PDIF Receiver Input Converter Widget (Node ID = 07h) is set to ‘1’.
- RX Raw Data Mode (bit 6) in the S/PDIF RX/TX Interface Control (CIR = 0001h) register is set to ‘1’.

8. PCB LAYOUT CONSIDERATIONS

8.1 Power Supply, Grounding

As with any high-resolution converter, the CS4207 requires careful attention to power supply and grounding arrangements if its potential performance is to be realized. Figure 1 on page 11 and Figure 2 on page 12 show the recommended power arrangements, with VA connected to a clean supply. VD, which powers the digital circuitry, may be run from the system logic supply.

To achieve full analog performance, it is strongly recommended that the following rules be followed:

- place the cap between VBIAS and VA_REF as close to the codec as possible to minimize trace impedance
- keep the traces for VA and VA_REF separate as much as possible and only connect them at the supply

Extensive use of power and ground planes, ground plane fill in unused areas and surface mount decoupling capacitors are recommended. Decoupling capacitors should be as close to the pins of the CS4207 as possible. The low value ceramic capacitor should be closest to the pin and should be mounted on the same side of the board as the CS4207 to minimize inductance effects. All signals, especially clocks, should be kept away from the FILT+ and VCOM pins in order to avoid unwanted coupling into the modulators. The CDB4207 evaluation board demonstrates the optimum layout and power supply arrangements.

8.2 QFN Thermal Pad

The CS4207 is available in a compact QFN package. The underside of the QFN package reveals a large metal pad that serves as a thermal relief to provide for maximum heat dissipation. This pad must mate with an equally dimensioned copper pad on the PCB and must be electrically connected to ground. A series of vias should be used to connect this copper pad to one or more larger ground planes on other PCB layers. In split ground systems, it is recommended that this thermal pad be connected to AGND for best performance. The CDB4207 evaluation board demonstrates the optimum thermal pad and via configuration.

9. PARAMETER DEFINITIONS

Dynamic Range

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified bandwidth. Dynamic Range is a signal-to-noise ratio measurement over the specified band width made with a -60 dBFS signal. 60 dB is added to resulting measurement to refer the measurement to full-scale. This technique ensures that the distortion components are below the noise level and do not affect the measurement. This measurement technique has been accepted by the Audio Engineering Society, AES17-1991, and the Electronic Industries Association of Japan, EIAJ CP-307. Expressed in decibels.

Total Harmonic Distortion + Noise

The ratio of the rms value of the signal to the rms sum of all other spectral components over the specified band width (typically 10 Hz to 20 kHz), including distortion components. Expressed in decibels. Measured at -1 and -20 dBFS as suggested in AES17-1991 Annex A.

Frequency Response

A measure of the amplitude response variation from 10 Hz to 20 kHz relative to the amplitude response at 1 kHz. Units in decibels.

Interchannel Isolation

A measure of crosstalk between the left and right channel pairs. Measured for each channel at the converter's output with no signal to the input under test and a full-scale signal applied to the other channel. Units in decibels.

Interchannel Gain Mismatch

The gain difference between left and right channel pairs. Units in decibels.

Gain Error

The deviation from the nominal full-scale analog output for a full-scale digital input.

Gain Drift

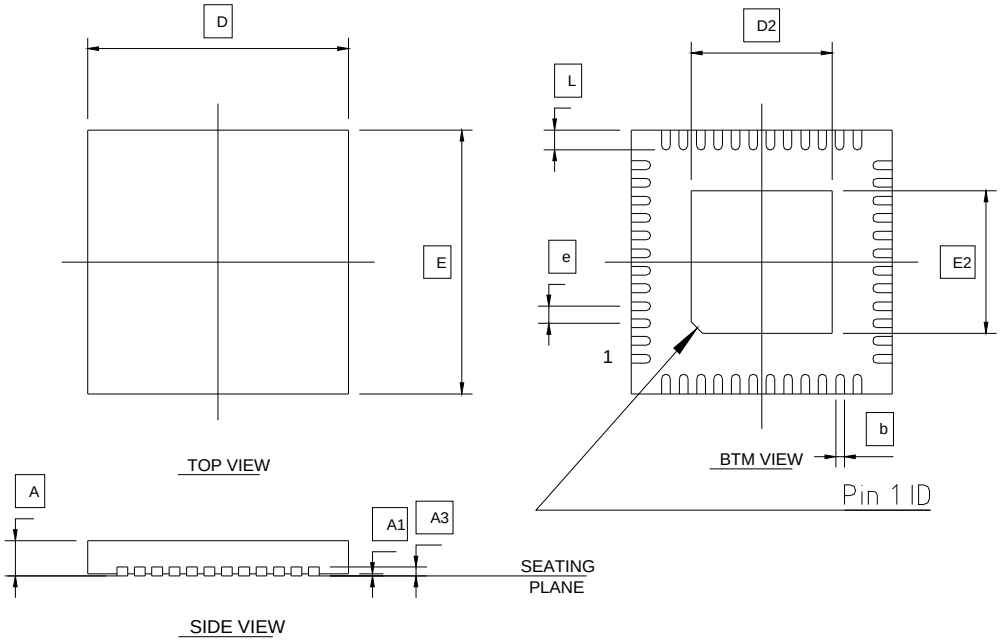
The change in gain value with temperature. Units in ppm/°C.

Offset Error

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal. Units in mV.

10.QFN PACKAGE DIMENSIONS

48L QFN (6 X 6 mm body) Package Drawing



Notes:
1) Controlling dimensions are in mm.
2) Dimensioning and tolerancing conform to ASME Y14.5m-1994
3) Dimension b applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip.
4) Reference JEDEC MO-229

DIM	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00		0.05
A3		0.20 BSC	
b	0.15	0.20	0.25
D		6.00 BSC	
D2	4.55	4.60	4.65
E		6.00 BSC	
E2	4.55	4.60	4.65
e		0.40 BSC	
L	0.30	0.40	0.50

THERMAL CHARACTERISTICS

Parameter		Symbol	Min	Typ	Max	Units
Junction to Ambient Thermal Impedance	4 Layer Board	θ_{JA}	-	24	-	°C/W
Junction to Case Thermal Impedance	4 Layer Board	θ_{JC}	-	10	-	°C/W

11.ORDERING INFORMATION

Product	Description	Package	Pb-Free	Grade	Temp Range	Container	Order #
CS4207	Low Power, 4-In/6-Out HD Audio Codec with Headphone Amp	48L-QFN	Yes	Commercial	-40°C to +85°C	Tray	CS4207-CNZ
						Tape & Reel	CS4207-CNZR
CS4207	Low Power, 4-In/6-Out HD Audio Codec with Headphone Amp	48L-QFN	Yes	Automotive	-40°C to +105°C	Tray	CS4207-DNZ
						Tape & Reel	CS4207-DNZR
CDB4207	CS4207 Evaluation Board		-	-	-	-	CDB4207

12.REFERENCES

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6. Cirrus Logic, *AN48: Design Notes for a 2-Pole Filter with Differential Input,* March 2003. http://www.cirrus.com/en/pubs/appNote/AN048Rev2.pdf

13.REVISION HISTORY

Revision	Changes
F1	• Production Release
F2	• Added "Digital Microphone Interface Characteristics" on page 22 • Updated "Implementation Identification" on page 44 as per HDA006-A • Updated ADC1 SZCMode in "ADC Configuration (CIR = 0002h)" on page 131 • Updated DAC1 SZCMode in "DAC Configuration (CIR = 0003h)" on page 134 • Added "Analog Inputs" on page 139 • Updated "QFN Package Dimensions" on page 146 (updated thermal characteristics)
F3	• Updated "Analog Input Characteristics (Commercial - CNZ)" on page 14 and "Analog Input Characteristics (Automotive - DNZ)" on page 15 (corrected MICIN/LINEIN input impedance) • Added "S/PDIF Input and Outputs" on page 143 • Updated "QFN Package Dimensions" on page 146 (corrected D2, E2, and L dimensions)
F4	• Changed CS4207-CNZ and CS4207-DNZ containers to "Tray" in Section 11.

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find one nearest you, go to www.cirrus.com.