intersil | Techwell™

LCD Video Processor with Built-in Decoder, Triple ADCs, LVDS & TTL Inputs, MCU, OSD, TCON and LVDS panel interface

TW8836

The TW8836 is a highly integrated LCD video processor that incorporates many of the features required to create a multi-purpose LCD display system into a single package. This includes a high quality 2D comb NTSC/PAL/SECAM video decoder, triple high speed RGB ADCs, an LVDS and TTL digital input interface, high quality scaler and de-interlacer, as well as a versitile OSD, high performance MCU, and LVDS or TTL output panel interface. The TW8836 can support input resolutions up to 1080p and can drive LCD panels at resolutions up 1366 x 768. The TW8836's video processing capability includes arbitrary H/V scaling, panoramic scaling, image mirroring, image adjustment and enhancement, black and white stretch, etc. The feature set and versatility of this device makes it an ideal solution for in-car LCD display applications, as well as portable display applications such as Pico Projectors.

Applications

- In-car display
- Pico Projector & Portable media player
- Portable DVD and DVR players

Analog Video Decoder

- NTSC (M, 4.43) and PAL (B, D, G, H, I, M, N, N combination), PAL (60), SECAM with automatic format detection
- Three 10-bit ADCs and analog clamping circuit.
- Fully programmable static gain or automatic gain control for the Y or CVBS channel
- Programmable white peak control for the Y or CVBS channel
- Software selectable analog inputs allows composite, S-video, analog YPbPr or RGB
- High quality adaptive 2D comb filter for both NTSC and PAL inputs
- PAL delay line for color phase error correction
- Image enhancement with 2D dynamic peaking / CTI.
- Digital sub-carrier PLL for accurate color decoding
- Programmable hue, brightness, saturation, contrast, sharpness
- Selectable differential or single-ended CVBS input
- Digital horizontal PLL and Advanced synchronization processing for VCR playback and weak signal performance
- High quality horizontal and vertical filtered down scaling with arbitrary scale down ratio
- Up to 2CH differential or 4CH single ended CVBS input

Analog RGB Inputs

- Triple high speed 10-bit ADCs with clamping and programmable gain amplifier
- SOG and H/V sync support for YPbPr or RGB input
- Built-in line locked PLL with sync separator
- Supports input resolution up to 1080p

Digital Inputs Support

- Supports both BT656 and 601 video formats
- Supports YCbCr/RGB 24-bit input (bi-directional) up to 1080p resolution
- Single channel LVDS input up to 720p resolution
- Supports RGB 565 + BT 656 at the same time

TFT Panel Support

- Built-in programmable timing controller
- Supports 3, 4, 6 or 8 bits per pixel up to 16.8 million colors with built-in dithering engine
- Supports digital panels (TTL) or single channel LVDS panels up to WXGA (1366 x 768) resolution, 85MHz
- Supports Serial (8-bit) RGB panel

Font Based On Screen Display

- Eight window font OSD with bordering / shadow
- 10KB programmable font RAM and 512 display RAM
- 1/2/3/4 bits/pixel
- Supports variable width (12/16), height (2~32)

SPI Flash Based On Screen Display

- 9 bitmap based OSD windows in 2 layers through SPI with alpha blending between layers
- Supports 4/6/8 bits/pixel
- Supports RLE decompression for two windows

Image Processing

- High quality scaler with both up/down and panorama / water-glass scaling support
- Built-in 2D de-interlacing function
- Programmable brightness, contrast, saturation, hue and sharpness
- Programmable color transient improvement control
- Supports programmable cropping of input video and graphics
- Independent RGB gain and offset controls
- DTV hue adjustment
- Programmable 8-bit Gamma correction for each color
- Black/White Stretch

Clock Generation

- Spread spectrum profile based on triangular modulation with center spread
- Programmable modulation frequency and spread width

Timing Controller (TCON)

- Supports programmable interface signals for control
- Column (source) driver/Row (gate) driver

MCU

- Industry standard 8052 based
- Code fetch from external SPI flash memory
- 256B code cache
- 2K XDATA memory
- Supports power save mode with 32K internal clock
- ISP (In System Programming) through I2C
- Supports 24-bit addressing

BT.656 Output

- Independent ITU-R 656 compatible YCbCr(4:2:2) output format
- Supports progressive ITU-R 656 output format for both interlaced and progressive inputs
- ITU-R 656 output generated from decoder, ARGB, DRGB and post scaling path

Touch Screen Controller

- Built-in 4-wire resistive touch screen
- 12–bit ADC
- 4 channel Auxiliary input

Miscellaneous

- Supports Fast Mode Plus I2C interface
- Up to 4 PWMs
- GPIOs
- 1.8/3.3V internal operation
- 1.8V I/O support
- Power-down mode
- Single 27MHz crystal
- 128-pin LQFP and 144 pin TFBGA package

Table of Contents

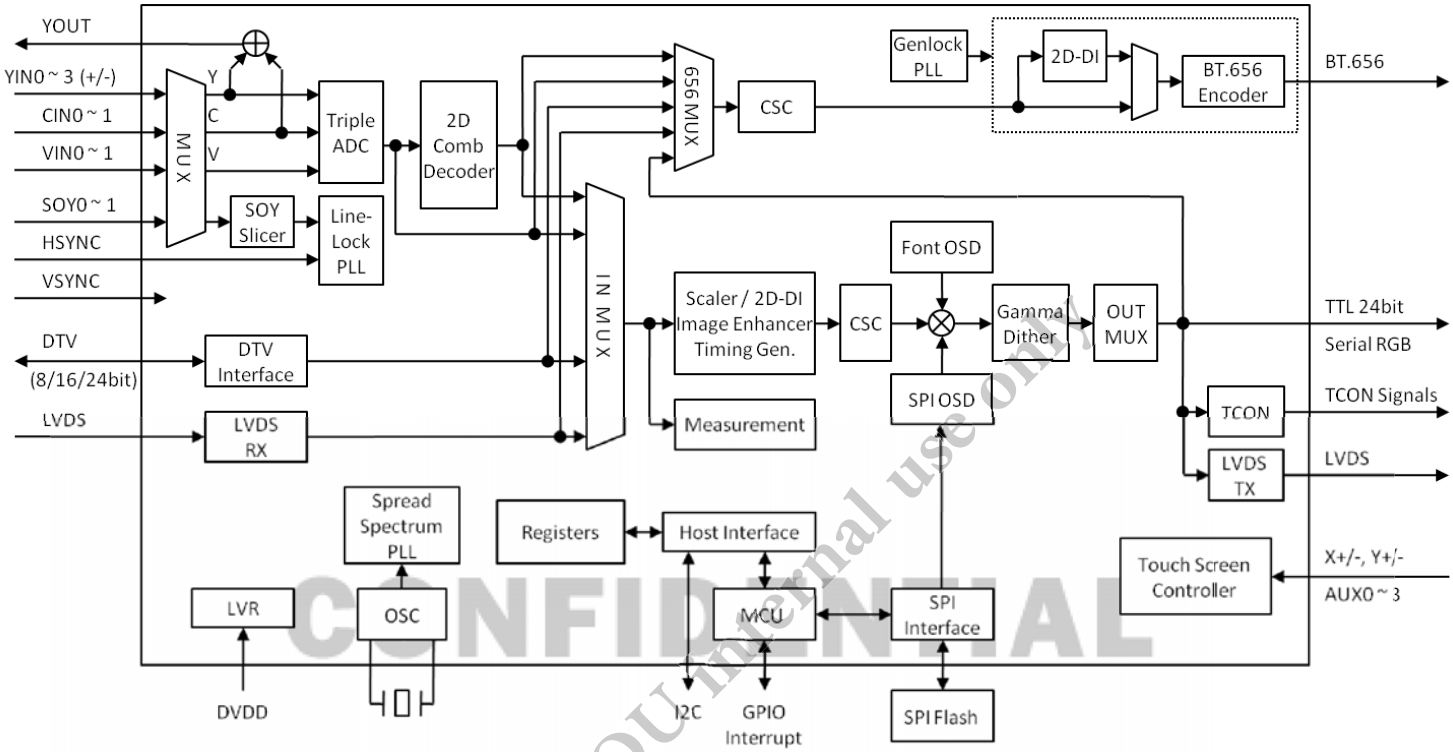
Ordering Information

PART NUMBER	PART MARKING	PACKAGE (PB-FREE)	PKG. DWG. #
TW8836-BA1-CR (Note **Error! Reference source not found.**)	TW8836 BA1-CR	144 Ball TFBGA (7mmx7mm)	V144.7X7A
TW8836-LA1-CR (Note **Error! Reference source not found.**)	TW8836 LA1-CR	128 Lead LQFP (14mmx14mm)	Q128.14x14
TW8836AT-LA1-GR (Note **Error! Reference source not found.**)	TW8836AT LA1-GR	128 Lead LQFP (14mmx14mm)	Q128.14x14

NOTES:

1. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. These Intersil Pb-free WLCSP and BGA packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e1 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free WLCSP and BGA packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

TW8836 Functional Block Diagram



Functional Description

Overview

Intersil|Techwell's TW8836 LCD Video processor is a highly integrated TFT panel controller. It integrates a high quality 2D comb NTSC/PAL/SECAM video decoder, scalers and de-interlacer, timing controller, flexible OSD (font based and SPI bit-map based OSD engine), and a high performance MCU. This unique level of mixed signal integration turns a TFT panel into a flexible display system. TW8836 incorporates easy-to-operate features in a single package for multi-purpose in-car LCD display, portable DVD and DVRs, media players, and pico projectors. It contains all the logic required to convert analog or digital video signals in various formats to the signal formats that are necessary to drive various kinds of TFT panels. It supports different panel resolutions depending on the scaler and panel clock settings, and has a built-in TCON for direct connecting with low cost TCON-less panel.

The integrated analog front-end contains ADCs with clamping circuits and Automatic Gain Control (AGC)

circuits as well as anti-aliasing filters to minimize the external component count. The built-in video decoder employs proprietary 2D Comb filter Y/C separation technologies to produce exceptionally high quality pictures.

The chip's internal logic synchronizes the panel frame rate to the incoming input frame rate. A high quality image-scaling engine is used to convert the different input resolution formats to the output panel resolution. An internal de-interlacing engine also allows interlaced video to be displayed.

In addition, TW8836 has an array of integrated value-added features and input/output flexibility that makes it an extremely versitile single chip solution. On Screen Display (OSD) is supported through an on-chip multi-window OSD engine for maximum flexibility. Integraged 12-bit ADCs for 4-wire resistive touch screen control, single channel LVDS (Open LDI) input and output, as well as an on-chip MCU are just a few of these features. The host control interface supports a standard 2-wire serial bus

Analog Front-end

The analog front-end converts analog video signals to the required digital format. Each channel contains an automatic clamping circuit, AGC circuit, anti-aliasing filter and high performance ADCs to minimize the number of external components needed. The clamping circuit restores the signal DC level so it can be properly digitized. The analog inputs source selections are software programmable. Different input sources have different signal conditioning logic to properly convert the signal into correct format for further processing.

Video Decoder

SYNC PROCESSOR

The decoder sync processor of the video input detects horizontal synchronization and vertical synchronization signals in the composite video or in the Y signal of an S-Video input. The processor contains a digital phase-locked-loop (PLL) and decision logic to achieve reliable sync detection in both stable signals as well as in unstable signals, such as those from VCR fast forward or rewind.

HORIZONTAL SYNC PROCESSING

Horizontal synchronization processing contains a sync separator, a phase-locked-loop (PLL), and the related decision logic.

The horizontal PLL locks onto the extracted horizontal sync in all conditions to provide a jitter free output image. From there, the PLL also provides orthogonal sampling raster for the down-stream processor. It has a very wide lock-in range for tracking any non-standard video signal.

VERTICAL SYNC PROCESSING

The vertical sync separator detects the vertical synchronization pattern in the input video signals. A detection window controls the sync determination to provide a more reliable synchronization and simulates the functionality of a PLL without the complexity of a PLL. The field status is determined at the vertical synchronization time based on the vertical and horizontal sync relationship.

COLOR DECODING

Y/C SEPARATION

The color-decoding block contains the luma / chroma separation engine for composite video signals and multi-standard color demodulation. For NTSC and PAL standard signals, the luma / chroma separation can be done either by comb filter or notch/band-pass filter combination. For SECAM standard signals, only notch/band-pass filter is available. The default selection for NTSC/PAL is comb filter. The characteristics of the band-pass filter can be found in the filter curve section.

In the case of comb filter, the decoder separates luma (Y) and chroma (C) of a NTSC/PAL composite video signal using a proprietary adaptive comb filter algorithm. It leads to good Y/C separation with minimal cross luma and cross color at both horizontal and vertical edges. Due to the nature of the line buffer used in the comb filter, there is always a two line processing delay in the output images regardless of what standard or filter option is chosen.

COLOR DEMODULATION

The color demodulation for NTSC and PAL standards are done by quadrature mixing of the chroma signal to the base band and extracting the chroma components with the low-pass filter. The low-pass filter characteristics can be selected for optimized transient color performance. For the PAL system, the PAL ID or the burst phase switching is identified to aid the PAL color demodulation.

The SECAM color demodulation process consists of bell filtering, FM demodulation, and de-emphasis filtering. The chroma carrier frequency is identified in the process and used to control the SECAM color demodulation.

The sub-carrier signal used in the color demodulator is generated by a direct digital synthesis PLL that locks onto the input sub-carrier reference (color burst). This arrangement allows any sub-standard NTSC or PAL signal to be demodulated easily.

AUTOMATIC CHROMA GAIN CONTROL

The Automatic Chroma Gain Control (ACC) compensates for reduced amplitudes caused by transmission loss in the video signal. In the NTSC/PAL standards, the color reference signal is the burst on the back porch. This color-burst amplitude is

calculated and compared to standard amplitude. The chroma (Cx) signals amplitude is then compensated accordingly. The range of ACC control is –6db to +24db.

LOW COLOR DETECTION AND REMOVAL

For low color amplitude signals, black and white video, or very noisy signals, the color will be “killed”. The color killer uses the burst amplitude measurement to switch-off the color when the measured burst amplitude falls below a programmed threshold. The threshold has programmed hysteresis to prevent oscillation of the color killer operation. This function can be disabled by programming a low threshold value.

AUTOMATIC STANDARD DETECTION

The video decoder has automatic standard discrimination circuitry. The circuit uses burst-phase, burst-frequency, and frame rate to identify NTSC, PAL or SECAM color signals. The standards that can be identified are NTSC (M), NTSC (4.43), PAL (B, D, G, H, I), PAL (M), PAL (N), PAL (60) and SECAM (M). Any of these standards can be included or excluded in the standard recognition process by software control. The identified standard is indicated by the Standard Selection (SDT) register. Automatic standard detection can be overridden by software controlled standard selection.

VIDEO FORMAT SUPPORT

The integrated video decoder supports all common video formats as shown in Table 1. This needs to be programmed appropriately for each of the composite video input formats.

TABLE 1. VIDEO INPUT FORMATS SUPPORTED

Format	Lines	Fields	Fsc	Country
NTSC-M	525	60	3.58 MHz	U.S., many others
NTSC-Japan (1)	525	60	3.58 MHz	Japan
PAL-B, G, N	625	50	4.43 MHz	Many
PAL-D	625	50	4.43 MHz	China
PAL-H	625	50	4.43 MHz	Belgium
PAL-I	625	50	4.43 MHz	Great Britain, others
PAL-M	525	60	3.58 MHz	Brazil
PAL-CN	625	50	3.58 MHz	Argentina
SECAM	625	50	4.406MHz 4.250MHz	France, Eastern Europe, Middle East, Russia
PAL-60	525	60	4.43 MHz	China
NTSC (4.43)	525	60	4.43 MHz	Transcoding

Notes: (1). NTSC-Japan has 0 IRE setup.

COMPONENT PROCESSING

LUMINANCE PROCESSING

The video decoder adjusts brightness by adding a programmable value (in register BRIGHTNESS) to the Y signal. It adjusts the picture contrast by changing the gain (in register CONTRAST) of the Y signal.

The decoder also provides a sharpness control function through a control register. The center frequency of the peaking filter is selectable, and a coring function is provided along with the sharpness control to reduce enhancement to the noise.

THE HUE AND SATURATION

When decoding NTSC signals, the decoder can adjust the hue of the chroma signal. The hue is defined as a phase shift of the subcarrier with respect to the burst. This phase shift can be programmed through a control register.

The color saturation can be adjusted by changing the gain of Cb and Cr signals for all NTSC, PAL and SECAM formats. The Cb and Cr gain can be adjusted independently for flexibility.

Touch Screen Controller

Built-in 12-bit ADC touch screen controller in TW8836 provides accurate position reading with simplified digital operation and can also be used to monitor up to four auxiliary inputs with touch interrupt.

Digital Input Support

In addition to analog inputs, TW8836 also has dual digital inputs for YCbCr/RGB data and a single channel LVDS port (Open LDI type). The DTV input supports up to 24 bit digital RGB with resolution up to 1080p and opperates independently from the LVDS input. The DTV port is bi-directional, and can be used as a digital output port to provide duplicate secondary panel output.

LVDS VIDEO INPUT INTERFACE

TW8836 LVDS video input interface takes 4 channel-data LVDS inputs and one LVDS clock input. The 4 channel serial input data are de-muxed intol parallel 28bits output (24bits of RGB and 4 bits of HSYNC, VSYNC, DataReady, and CNTL).

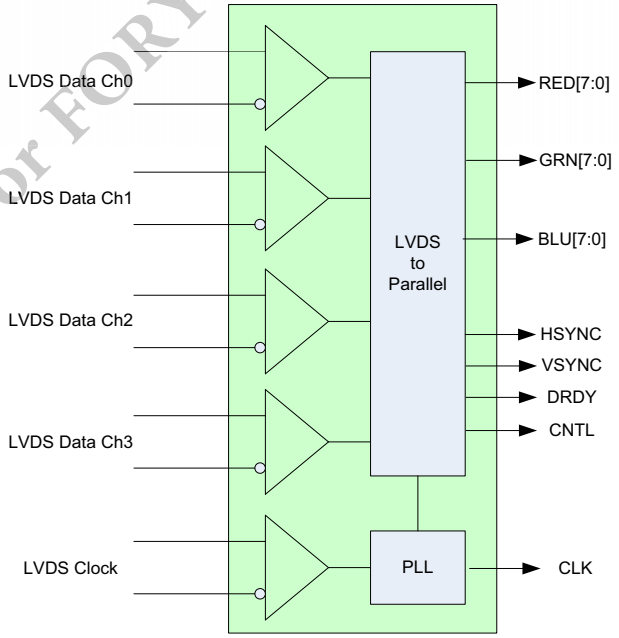


Figure 1 LVDS Rx Functional Block

The PLL recovers clock from VLDS input and generates synchronized capture clock for 24 video data. The following figure shows the LVDS Rx data / clock timing diagram for seral and parallel data.

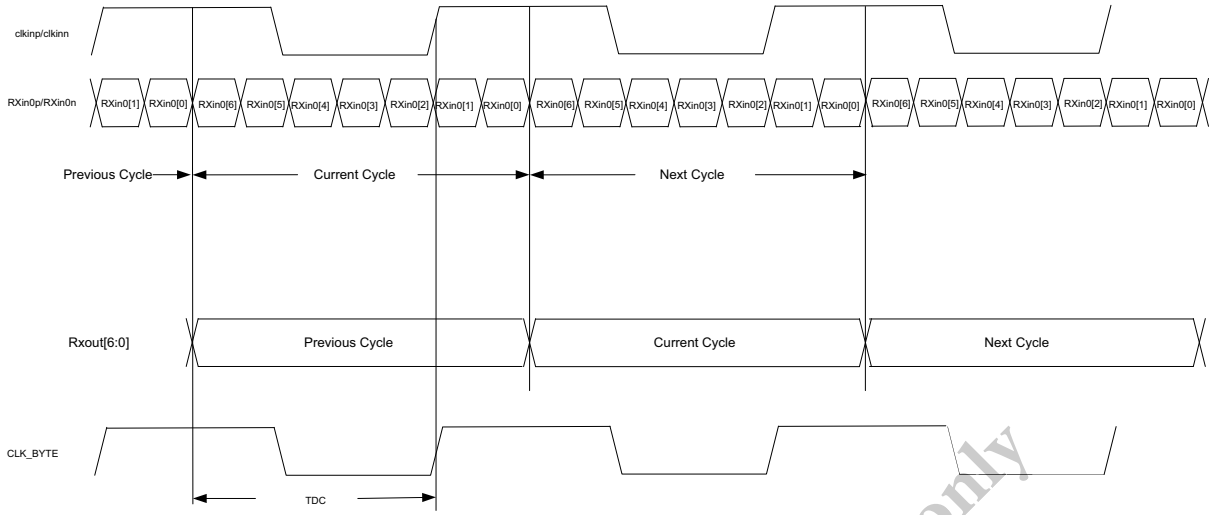


Figure 2 LVDS Rx Data/Clock Input/Output Timing diagram

In order for TW8836 LVDS Rx to operate properly, the input data switching timing needs to met. Figure 3 and Table 2 illustrates TW8836 LVDS Rx stroble data timing parameters.

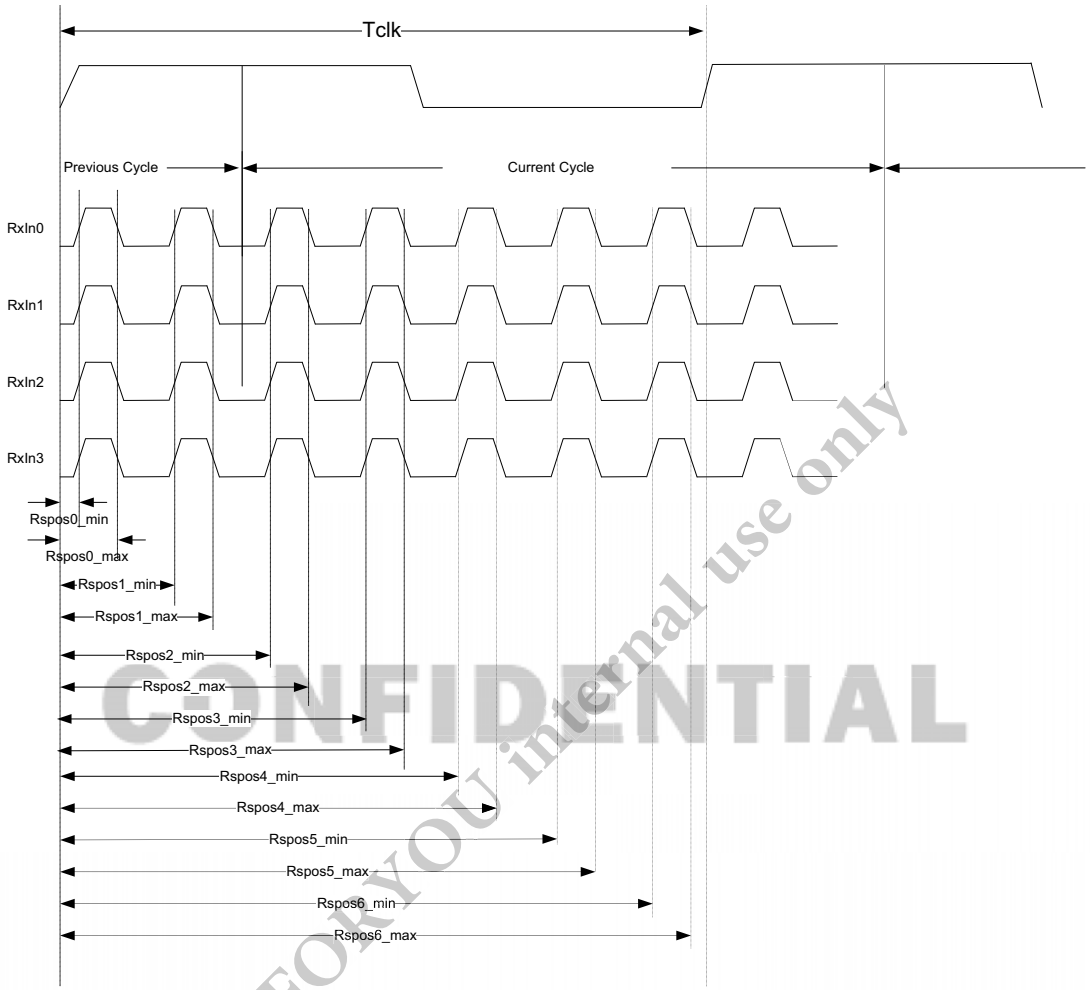


Figure 3 LVDS input strobe position

Symbol	Parameters	Min	Typ	Max	Units
RSPos0	Input Strobe position for Bit 0	0.49	0.84	1.19	ns
RSPos1	Input Strobe position for Bit 1	2.17	2.52	2.87	ns
RSPos2	Input Strobe position for Bit 2	3.85	4.21	4.55	ns
RSPos3	Input Strobe position for Bit 3	5.53	5.88	6.23	ns
RSPos4	Input Strobe position for Bit 4	7.21	7.56	7.91	ns
RSPos5	Input Strobe position for Bit 5	8.89	9.24	9.59	ns
RSPos6	Input Strobe position for Bit 6	10.57	10.92	11.27	ns

Table 2 LVDS Rx Switching timing (f=85MHz)

Input Image Control

The input cropping control provides a way for programming the active display window region for the selected input video or graphic. In normal operation, the first active line starts with the VSYNC signal. This and the vertical active length register setting are used to determine the active vertical window. The active pixel starts HSYNC. This and the horizontal active width register are used to determine the active horizontal window. The vertical window is programmed in line increments. The horizontal window is programmed in single pixel increments for single pixel input mode or two pixel increments for double pixel input mode. If the data qualifier is used, then only qualified pixels will be counted in the window size.

Image Scaling

The internal high quality image-scaling engine operates in several modes. The first is the bypass mode. No image scaling is done in this mode. The number of active output lines per frame and the number of active output pixels per line are identical to the input active lines and pixels, respectively. This mode is best used for displaying computer graphics at the panel's native resolution.

By default, the input active window is zoomed up to the full screen for display. This is used for non-interlaced data like PC graphics or progressive scan video. The vertical and horizontal magnification ratio can be adjusted independently. TW8836 has an option called frame-sync mode which does not use a frame buffer. In this mode, the zoom ratio and output clock rate should be coordinated appropriately to avoid internal buffer overrun.

The TW8836 has a built-in 2D de-interlacing engine to process interlaced video inputs. When used, every input field is zoomed to the full output frame resolution. The de-interlaced fields can also be properly adjusted to have fields aligned correctly to avoid any artifacts. The offset can be programmed to provide maximum flexibility.

The horizontal scaler can be programmed to perform non-linear scaling : panorama scaling for displaying 4:3 input on a 16:9 display and water-glass scaling for displaying 16:9 input on a 4:3 display.

Image Enhancement Processing

BLACK/WHITE STRETCH

This feature is to expand the dynamic range of the input image, which creates a more vivid image impression.

TFT Panel Support

TW8836 supports a variety of active matrix TFT panel types and resolutions up to 1366x768 including panels with a TTL or single channel LVDS interface.

DITHERING

TW8836 has a dithering circuit to reduce the output dynamic range to fit the panel type. This allows LCD panels with 3, 4, 6 or 8 bits per color per pixel to display up to 16.8 million colors and LCD panels with 3 bits per color per pixel can display up to 2.1 million colors. Both spatial and frame modulation dithering are available. When dithering with the least significant 4-bits of input data it uses spatial modulation with 4x4 blocks of pixels. When dithering with the least significant 1 to 3 bits of input data, it uses either spatial modulation with 2x2 pixel blocks, or frame modulation.

GAMMA TABLE

TW8836 has an integrated gamma table for each color output and is fully programmable through the host bus.

TCON

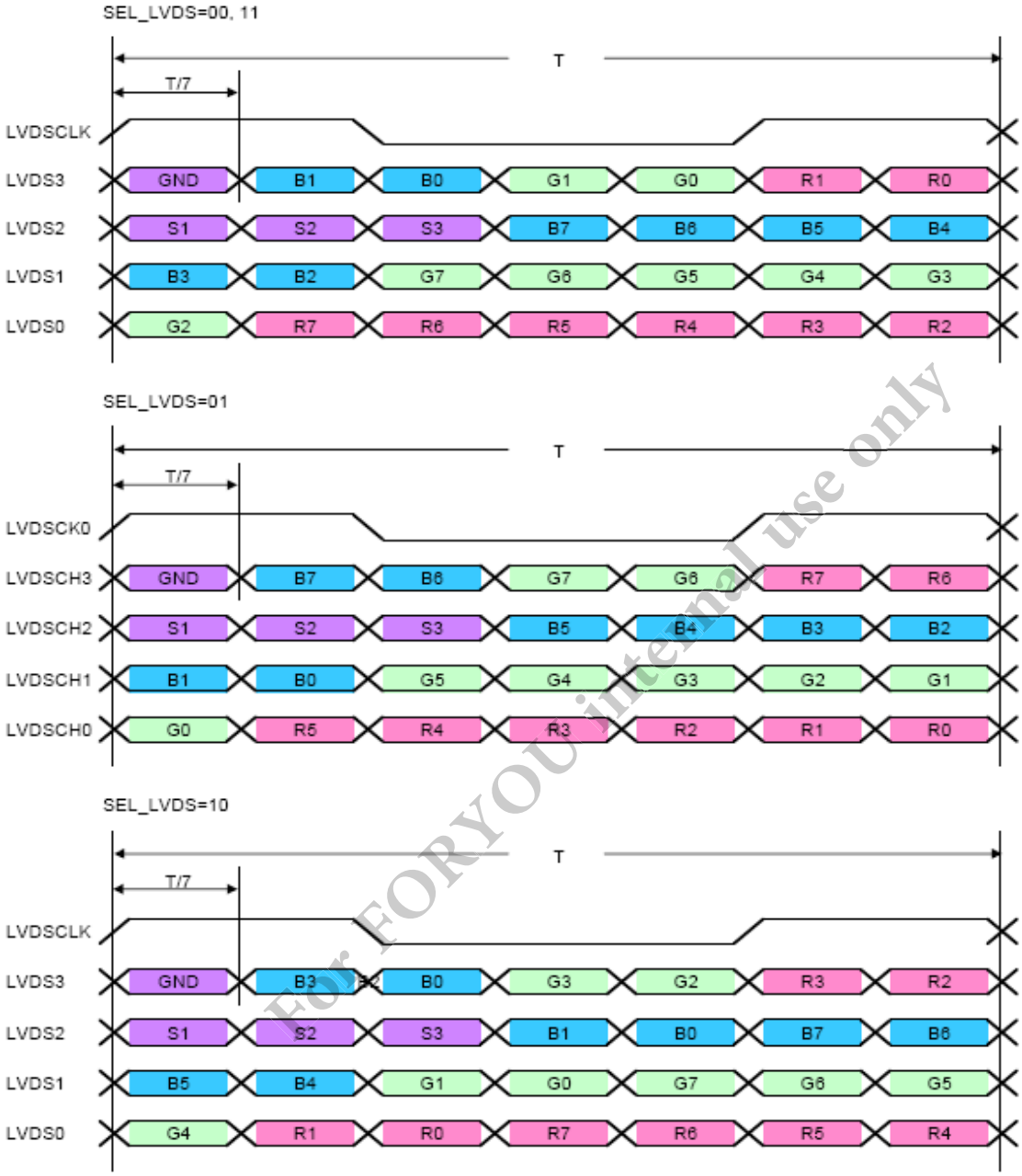
The integrated Timing controller supports flexible column/row driver control signals to interface with TCON-less panel directly.

LVDS OUT PUT FORMAT

TW8836 is able to control the output order for panel control signals VS, HS and DE by register settings.

LVDS COLOR MAPPING

TW8836 is able to control the output color order.



Font Based On Screen Display

The TW8836 has a built-in OSD controller with programmable RAM font. The OSD display is independent of the input active window settings and the scaling ratio.

The on-chip OSD controller is a character-based controller. The pre-defined character or graphic bit map is stored in the font RAM. It can store up to 379 single color fonts when the character is 12 pixels wide by 18 pixels high. The characters can be displayed on the screen in four user defined window locations of any size from 1 to 512 characters. The spaces between characters are also programmable. There is a limit of 512 characters that may be displayed on screen at one time in all windows combined. The attributes of each window can also be set to give it a shadow effect or 3-D effect. In addition, the characters can be expanded by a factor of 2, 3 or 4 in vertical or horizontal directions and have the blinking effect and border/shadow effect on a character by character basis.

ON CHIP OSD FUNCTIONS

Font SRAM: Max 379 (12x18) User Programmable Single Color Font (10240x8 SRAM)

- Character Register SRAM : 512 Location (9-bit Font Address + 10-bit Character Attribute, 512x19 SRAM)
- Characters

Character Color: 16 colors
Character Background Color: 16 colors
Character Blinking: Enable/Disable, 1 Hz Blinking frequency
Character Border/Shadow Effect: Enable/Disable

(Multi OSD Window Display Case : Chip has a limitation)
Character Space: Both H and V programmable by number of pixels
Quick Character Change in Window: Programmable Start Address and Buffer Size
Programmable OSD Color Palette Support
Re-designed OSD Font Supporting Standard Alpha-Numerical Character Set Windows
Number of Windows: 4 Independent Windows
Window Color: 16 colors
Window Zoom: 2, 3, 4 times zoom by dot number, H/V separate zooming control
Window Position: Programmable
H Direction: 1-pixel per step, V Direction: 1-Line per step
Window Size: Both H and V programmable by number of characters
Window Bordering/Shadowing Effect : 4 Independent Windows Enable/Disable Control
Window Alpha Blending Control : 4 Independent Windows Control
→ 16 Different Color for Alpha Blending support(4-bit control)
Window 3-D Effect : 4 Independent Windows Enable/Disable Control
Window Border Color : 16 Colors
Window Border Width: programmable

BASIC REGISTER SETTING FLOW EXAMPLE FOR BUILT-IN OSD CONTROLLER

Step_1: OSD_FONT_SIZE_CONFIGURATION

1. Select FONT Width to be 12 or 16 - 0x300 (bit4)
2. Set FONT Height - 0x350 (bit4-0)
3. Set Sub-Font Total Count - 0x351 (bit6-0)

Step_2: OSD_WINDOW_CONFIGURATION setting for **Window#1** (0x310~0x31F)
Note) **Window#2** (0x320~0x32F), **Window#3** (0x330~0x33F), **Window#4** (0x340~0x34F)

1. OSD Window Disable	0x310, bit7
2. OSD Window Zoom multiplier	0x310, bit1-0: V, bit3-2:H
3. OSD Window Background B Color	0x31E, bit6-4
4. OSD Window Background G Color	0x31E, bit6-4
5. OSD Window Background R Color	0x31E, bit6-4
6. OSD Window Background Color Extension	0x31E, bit7
7 OSD Window 3-D Effect Top/Bottom Mode Select	0x31B, bit6
8. OSD Window 3-D Effect Level Select	0x31B, bit5
9. OSD Window 3-D Effect Enable/Disable	0x31B, bit7
10. OSD Window H-Start Location (see details in next page)	0x313, bit7-0 0x312, bit6-4
11. OSD Window V-Start Location (see details in next page)	0x314, bit7-0 0x312, bit1-0
12. OSD Window Width	0x316, bit5-0
13. OSD Window Height	0x315, bit5-0
14. OSD Window Border_Line Width	0x318, bit4-0
15. OSD Window Border_Line B color	0x317, bit2-0
16. OSD Window Border_Line G color	0x317, bit2-0
17. OSD Window Border_Line R color	0x317, bit2-0
18. OSD Window Border_Line Enable	0x318, bit7
19. OSD Window Border Color Extension	0x317, bit3
20. OSD Window Shadow Width	0x31C, bit4-0
21. OSD Window Shadow B color	0x31B, bit2-0
22. OSD Window Shadow G color	0x31B, bit2-0
23. OSD Window Shadow R color	0x31B, bit2-0
24. OSD Window Shadow Enable	0x31C, bit7
25. OSD Window Shadow Color Extension	0x31B, bit3
26. OSD Window H-Space Width (Between Border_line and Characters)	0x319, bit6-0
27. OSD Window V-Space Width (Between Border_line and Characters)	0x31A, bit6-0
28. Character H-Space Width (Between Character and Character)	0x31D, bit7-4 0x31C, bit6
29. Character V-Space Width (Between Character and Character)	0x31D, bit3-0 0x31C, bit5
30. OSD Window Alpha Blending Color Select	0x352, bit4-0
31. OSD Window Alpha Blending Value Control	0x311, bit3-0
32. Window content start address	0x305, bit0 0x306, bit7-0
33. Repeat 1 – 32	

Step_3: OSD_COLOR_ATTRIBUTE / FONT setting (OSD RAM)

1. Enable OSD RAM Access
   - 0x304 (bit0 = 0)
2. Set Multi-Color Start Address
   - 0x305 (bit3-1), 0x30B (bit7-0), 0x353 (bit7-0), 0x354 (bit7-0)
3. OSD RAM Address
   - 0x305 (bit0), 0x306 (bit7-0)
   - The first address is Step_1_32 Window content start address.
4. OSD RAM Data Port High (Font Address)
   - 0x307 Data is written to above address automatically.
   - 0x304 (bit5=0) select lower 256 char. (bit5=1) select upper 256 char.
5. OSD RAM Data Port Bit18 (Border Effect), Bit17 (Blinking Effect), Bit16 (Upper|Lower 256 char.)
   - 0x304 Bit4, Bit7, and Bit5 Data are written to above address automatically.
6. OSD RAM Data Port Low (Color Attribute)
   - 0x308 Data is written to above address automatically.
7. Repeat 3), 4), 5), and 6)
   - The address should be increased by one each.

Step_4: COLOR LOOK-UP TABLE setting

1. Select Color Look-Up Table Write Address
   - 0x30C (bit[5:0])
   - BIT[5:0]: These 6 bits specify one of the 64 entries in the look-up table. Each entry is a 16-bit RGB color by its content.
   - There are 65536 colors available. For single color font, only sixteen of them are accessible by OSD controller at a given time.
2. Color Look-Up Table control bits setting
   - 0x30D (High Byte), 0x30E (Low Byte)
   - The data of the Look-Up Table is accessed through 0x30D and 0x30E.
3. Repeat 1) and 2) to program each entry of the Look-Up Table.

Step_5: FONT_RAM_DATA setting (FONT RAM)

1. Enable FONT RAM Access
   - 0x304 (bit0 = 1)
2. FONT RAM Address Setting - 8 bits(h00 – hFF)
   - 0x309
   - h00~hFF : Single Font RAM(256 Programmable Characters)
3. FONT RAM Data Port
   - - 0x30A Data is written to above address automatically.
4. Repeat (4) at 27 times for one FONT RAM Data
   - The internal address automatically increases by one each.
5. New FONT RAM Address Setting – 8 bits
6. Repeat 3), 4), 5)
   - The FONT RAM Address should be increased by one each.

Note) as for the FONT RAM configuration and font bit mapping, see the detailed description

Step_6: End of OSD setting and Enable OSD

1. OSD On/Off Enable Control 0: ON, 1: OFF
   - 0x30C (bit6 = 0)
2. OSD Window Enable
   - 0x310 (bit7 = 1) Window1 Enable

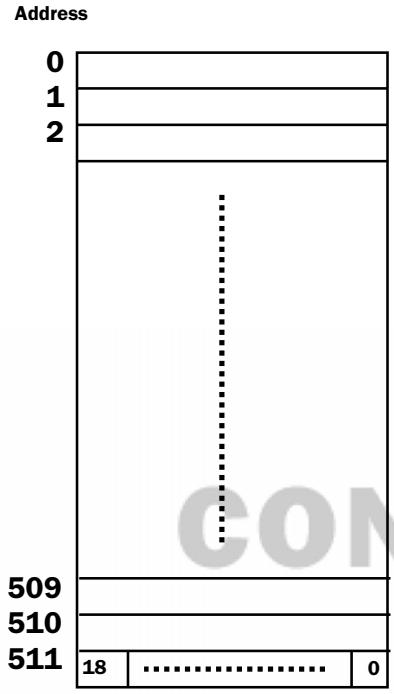
OSD WINDOW START LOCATION: BUILT-IN OSD CONTROLLER

Internal generated OSD DE Position delayed from H-SYNC: 0x303[7:0]

OSD window H_start location from start of internal OSD DE: 0x312[6:4], 0x313[7:0] increment by 1 pixel at a time

OSD window V_start location from start of VACT: 0x312[1:0], 0x314[7:0] increment by 1 line at a time

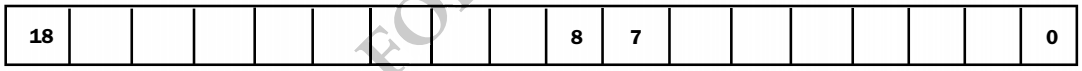
OSD_RAM CONFIGURATION



The characters can be displayed on the screen in four user defined window locations of any size from 1 to 512 characters. There is a limit of 512 characters that may be displayed on screen at one time in all windows combined.

Example

Window #1: Address 0 – 2 (3 character)
Window #2: Address 3 – 100 (98 character)
Window #3: Address 101– 254 (154 character)
Window #4: Address 255 - 511 (257 character)



FONT_ADDRESS (11-bits)

Bit 18: Border/Shadow
Bit 17: Blinking
Bit 16: Up256
Bit 15 - 8: FONT Address

FONT_ATTRIBUTE (8-bits)

Bit 7: Character's background color extension
Bit 6: Character's background R
Bit 5: Character's background G
Bit 4: Character's background B
Bit 3: Character's color extension
Bit 2: Character R
Bit 1: Character G
Bit 0: Character B

ALPHA BLENDING FOR OSD WINDOW

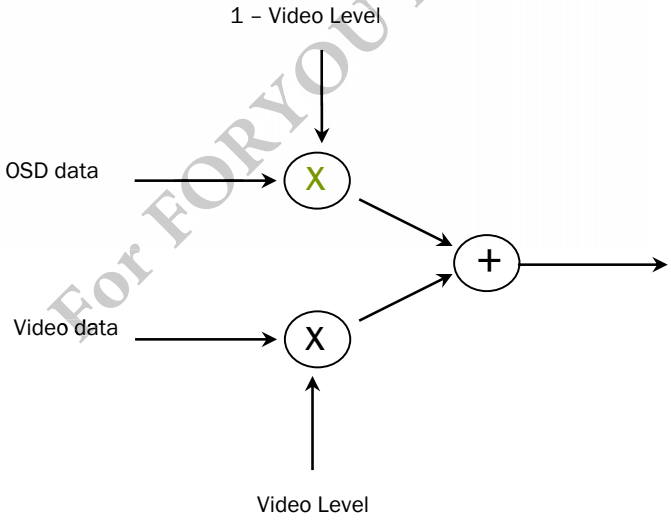
The TW8836 uses "Alpha Blending" in OSD 4 separation windows & 64 separation colors. The upper 32 separation colors are forced to 0. Alpha blending mixes (adds) the video signal and OSD signal at the following specified levels. In other words, alpha blending determines the transparency of the OSD window each color to in relation to video signal. When alpha blending is disabled, the only OSD data is displayed in OSD window.

The alpha blending level selection are 4-bit assigned, it can support 8 different level controls.

The alpha blending level bits are in register 0x311[3:0] for window#1, 0x321[3:0] for window#2, 0x331[3:0] for window#3, 0x341[3:0] for window#4 and alpha blending color selection bits are in register 0x352[4:0] for 32 separation colors.

alpha[3:0]	Video Level
0000	0.00 %
0001	12.5
0010	25.0
0011	37.5
0100	50.0
0101	62.5
0110	75.0
0111	87.5
1000	100

ALPHA BLENDING CONCEPT



SPI Flash On Screen Display

The TW8836 SPIOSD provides flexible mapping between its display on the LCD and its bit mapped image stored in the SPI memory. There are total nine windows provided. One of the windows is of “Complex” type, the rest are of “Simple” type. There are two layers of SPIOSD that can be alpha blended with each other and the active video.

In general, a buffer in the SPI memory is allocated for the image to be displayed. The “Simple” type refers to the windows that have the same buffer size and display size. Whereas the buffer size of a “Complex” window is usually larger than the display size. The SPIOSD Window #0 is designated as “Complex” window. The other eight windows (SPIOSD Window #1 ~ #8) are “Simple” windows.

The bit mapped image stored can be 4, 6 or 8 bits per pixel. During display, the pixel is fetched from the SPI memory and mapped to a 32-bit real color pixel by the LUT (Look Up Table). This 32-bit real color pixel consists of 24-bit RGB, 7-bit alpha blending attribute, and one bit blinking attribute. The real color pixel is then mixed with video before displaying on the LCD panel.

To reduce the storage size and the access time, RLC (Run Length Code) decode circuitry is provided. However, only one of the eight “Simple” windows can be assigned to receive RLC pixel data. The other windows must receive uncompressed pixel data.

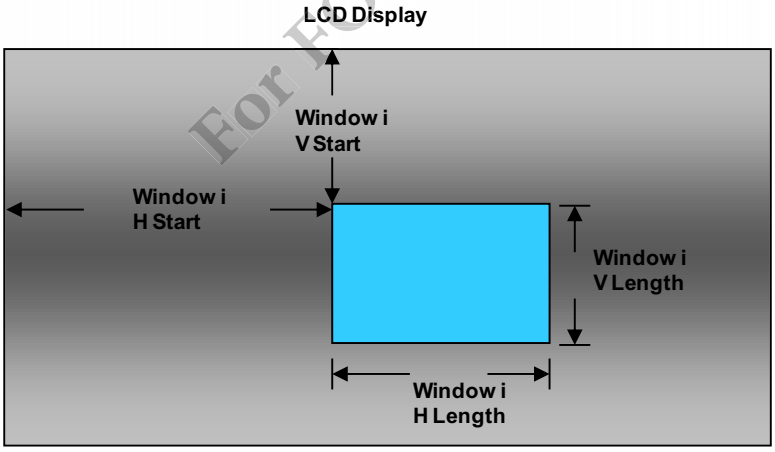
Each of the nine windows has its own set of register but shares a common 512 entry LUT. For each window, LUT Entry Offset register is provided for flexible mapping.

All nine windows can be active and overlapped at the same time without blending among themselves. Blending with video can be pixel based or window based.

Looping control for adjacent buffers is provided for the “Complex” window. Animation can be achieved by properly allocating multiple buffers in the adjacent area and the looping control.

SPIOSD Window Display Starting Location and Sizes

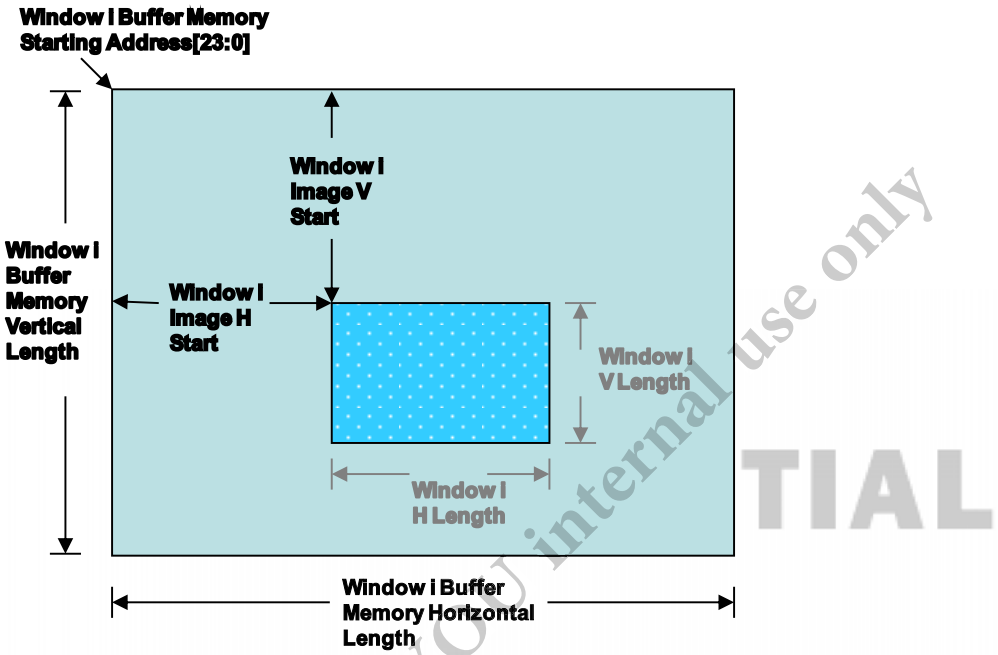
There are four registers used to specify the staring location and size on the LCD:
Window i Horizontal Start
Window i Vertical Start
Window i Horizontal Length
Window i Vertical Length



SPIOSD Window Buffer Memory

Two (or three for Complex window) registers define the buffer starting location and boundaries:
Window i Buffer Memory Starting Address
Window i Buffer Memory Horizontal Length
Window i Buffer Memory Vertical Length (Complex window only)

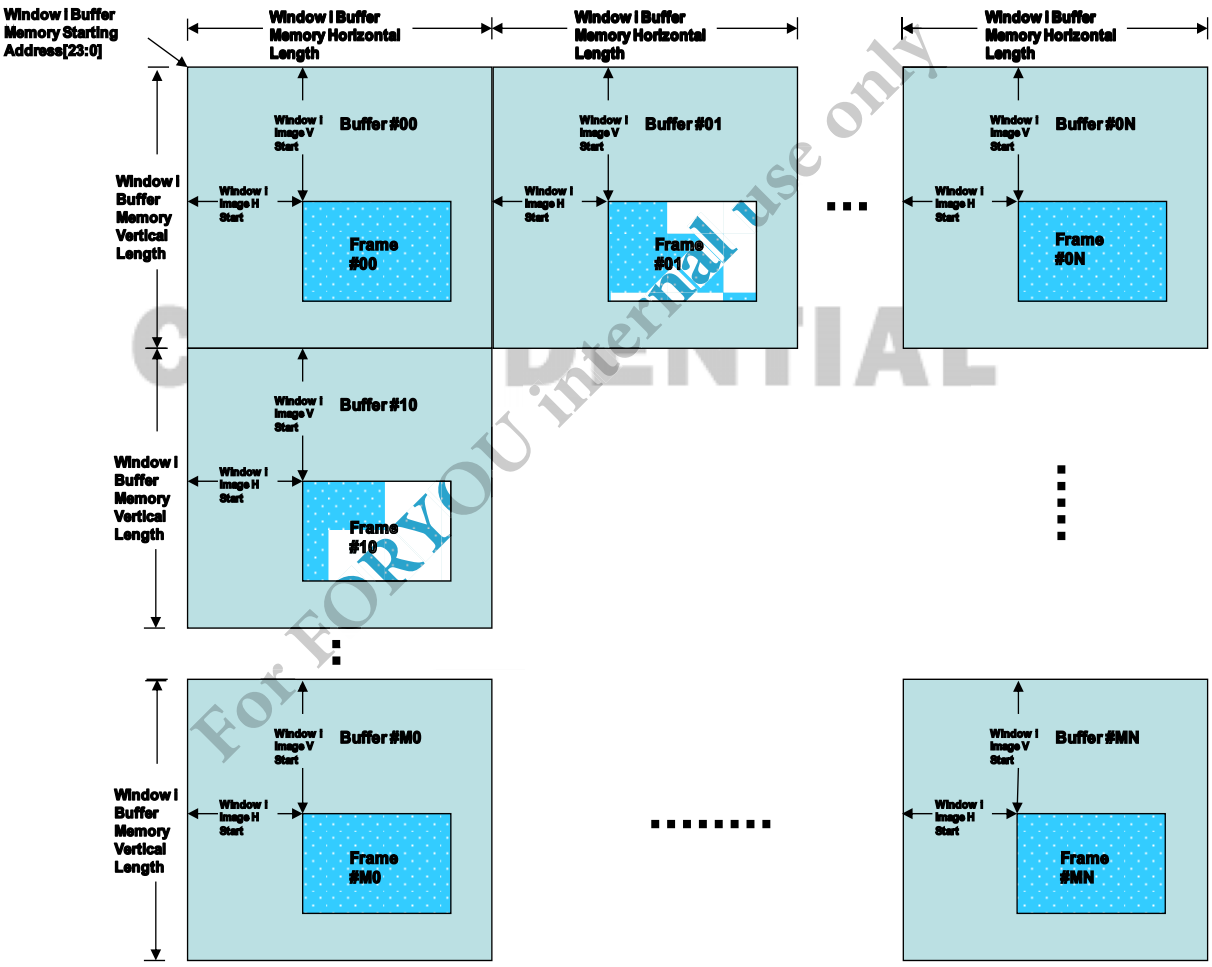
For Complex window two additional registers point to the starting location of the image stored:
Window i Image Vertical Start (Complex window only)
Window i Image Horizontal Start (Complex window only)



SPIOSD Window Loop Control

For Complex window, three registers are used for loop control:
Window i Looping Horizontal Frame Number (Complex window only)
Window i Looping Vertical Frame Number (Complex window only)
Window i Frame Duration (Complex window only)

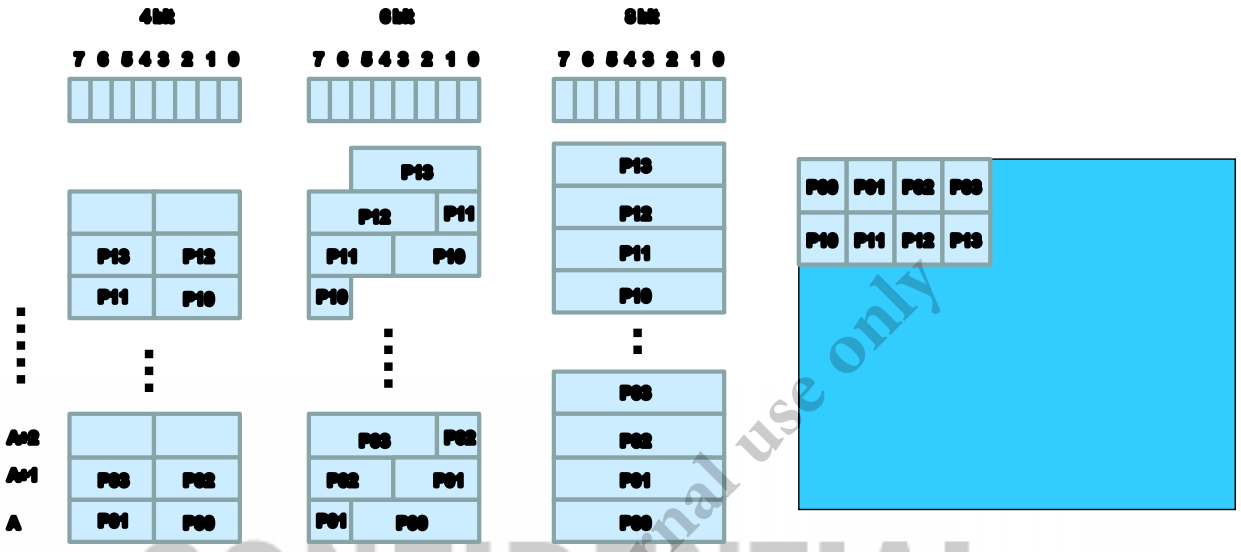
In the diagram below, the **Looping Horizontal Frame Number** register contains a value N, and the **Looping Vertical Frame Number** register contains a value M. The display starts from Frame #00 and then moves horizontally to the right and then vertically down. The display order is #00, #01, #02, ... #0N, #10, #11, #12, ... #1N, ... #M0, #M1, ... #MN. Each frame stays on for the time specified by **Frame Duration** register.



PIXEL ORDER

Pixel data (uncompressed) stored in SPI memory follows Little Endian order.

The following diagram shows the pixel on LCD display and its corresponding storage order in the SPI memory for pixel width 4, 6 and 8 bit wide.



RLC DATA FORMAT

RLC data format is shown below:

T: Type to follow, 0 for Data, 1 for CNT

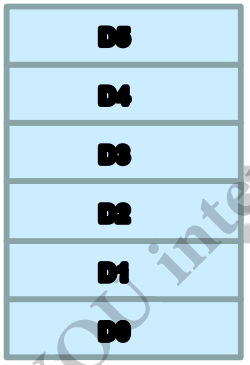
DATA: Uncompressed data

CNT: Repeat count

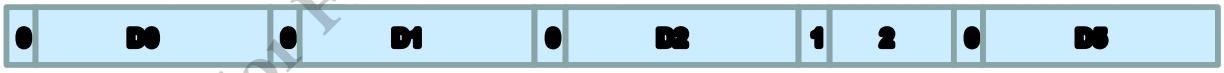
The width of DATA and CNT are set by RLC Control register. The valid DATA width is 4, 6, or 8. The width of CNT can be 2 up to 16.

The diagrams below show original data sequence of D0, D1, D2, D3, D4, and D5 before and after compression. In this example the DATA width is 8 and the CNT width is 4. Data D2, D3, and D4 are the same.

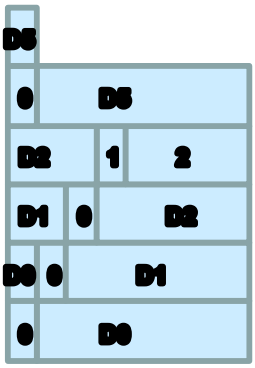
Original Data:



RLC Compression result:

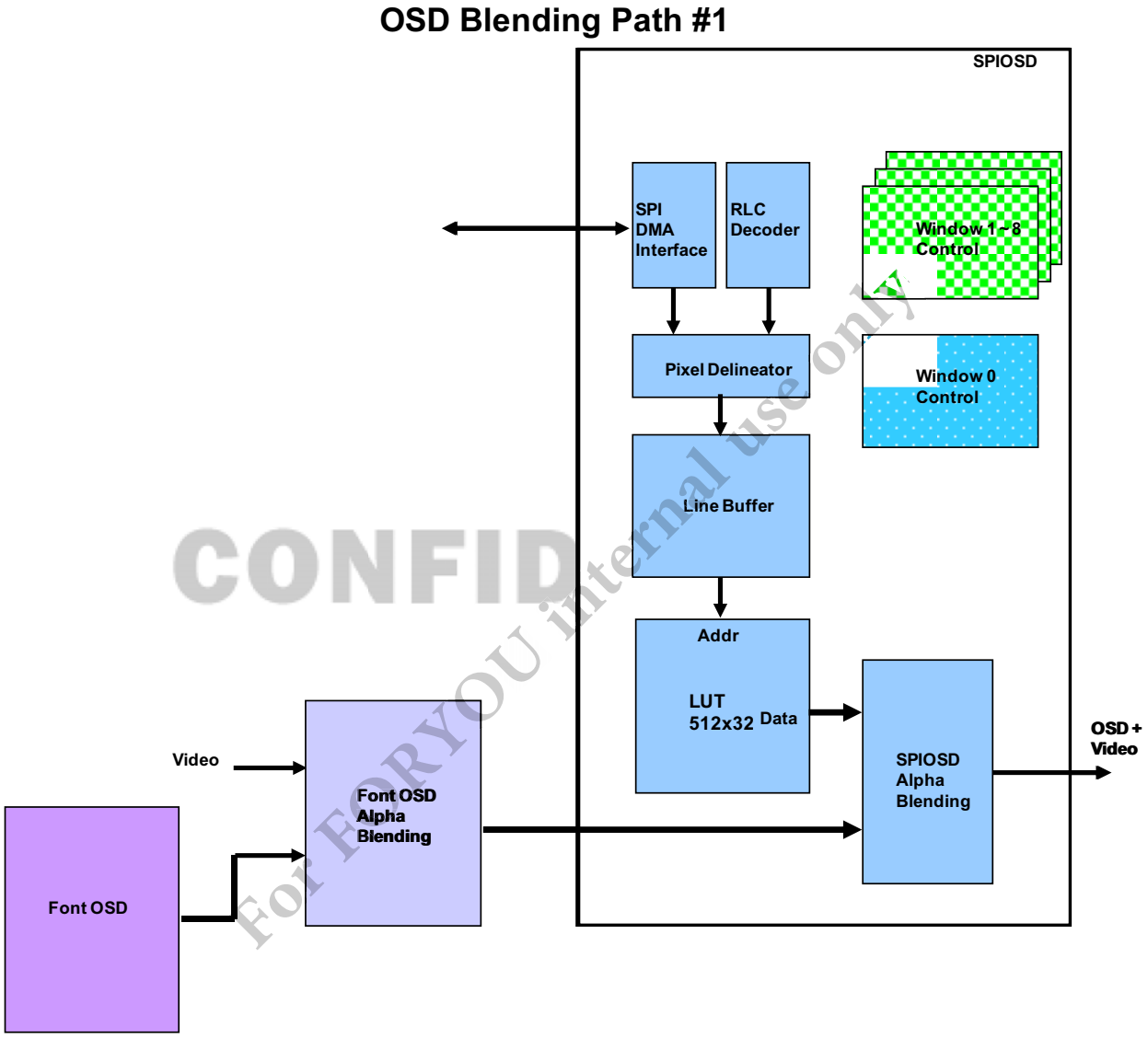


RLC data stored in memory:

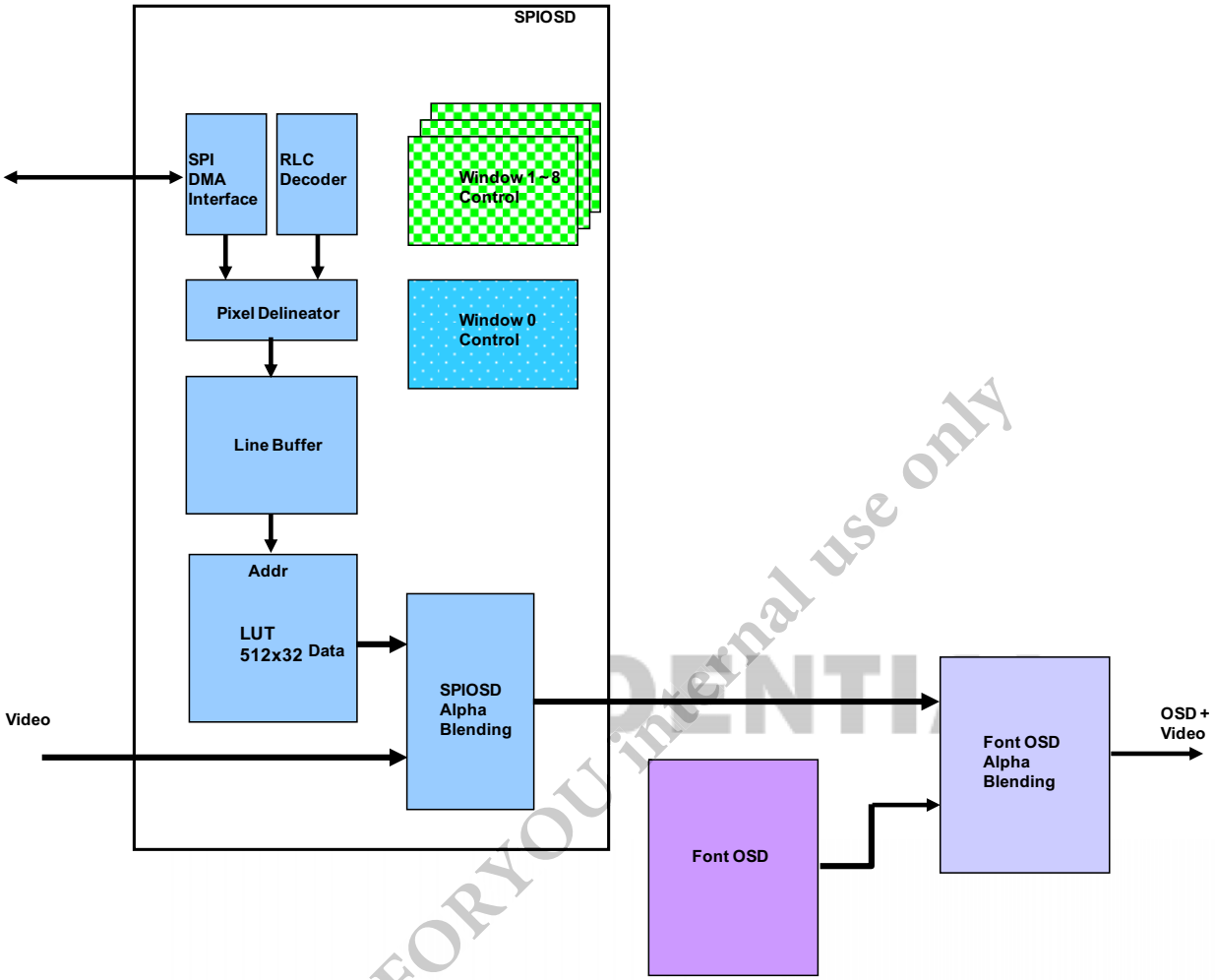


OSD DISPLAY PATH

In normal mixing order, Video input is mixed with Font OSD first. The resultant output is then mixed with SPIOSD. Alternatively, Video input can be mixed with SPIOSD first and then Font OSD.



OSD Blending Path #2



BUILT-IN MICROCONTROLLER

TW8836 has built-in 8052 microcontroller with program cache memory to enhance MCU performance. TW8836 MCU is 100% software compatible with industry standard 8052 with additional add-on features and faster instruction execution time.

The main features of TW8836 MCU

- Industry standard 8052 Core
- Timer 0, 1 and Timer 2
- Support 2 UARTs up to 115200bps
- Support External Interrupt INT0~INT6
- IO Port – Most of digital pins can be configured to GPIO
- Power Save Mode with internal 32KHz
- Watchdog

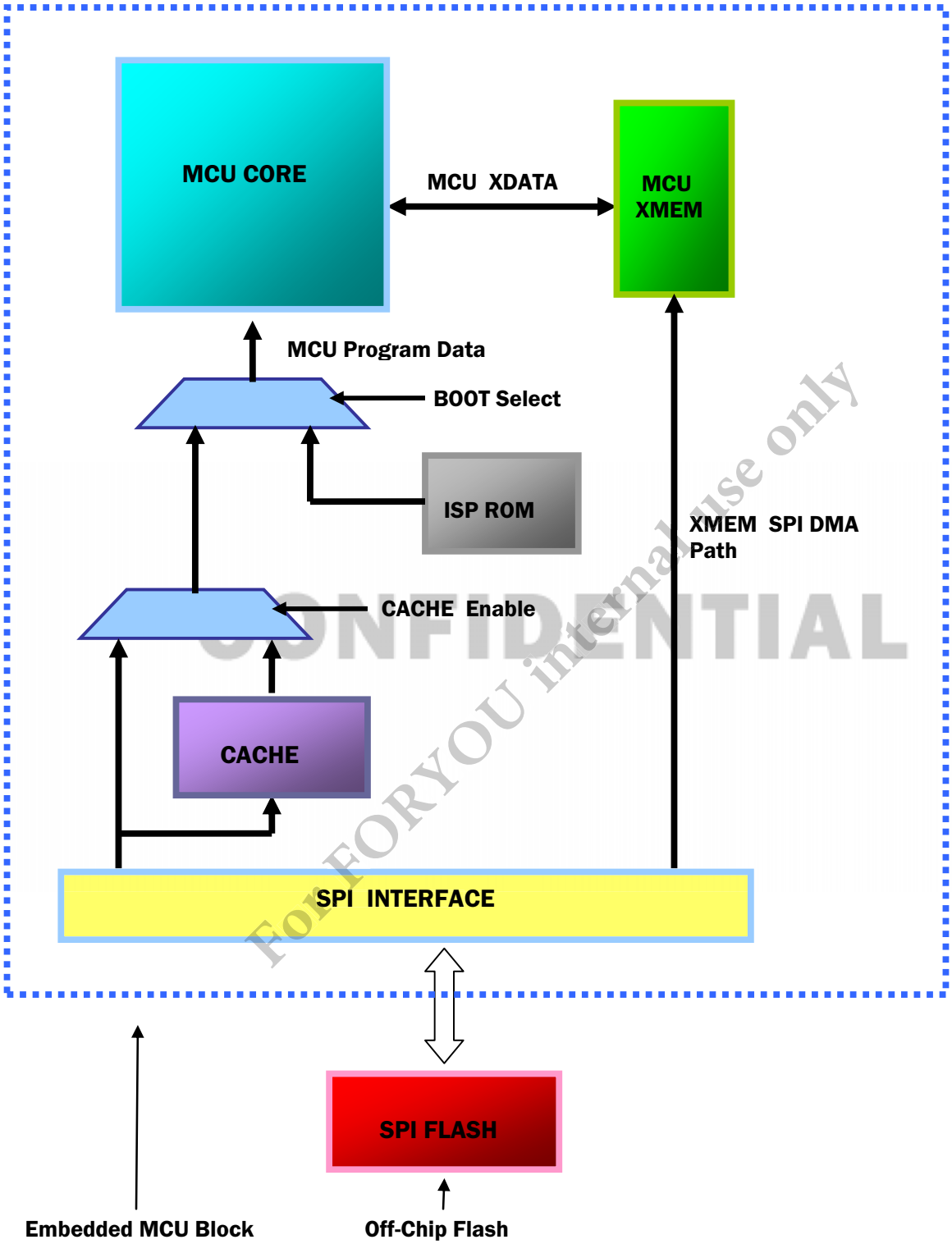
The additional add-on features for TW8836 MCU

- Program fetch from external SPI Flash with Single/Dual/Quad mode
- 256 B Code cache and 2K XDATA memory
- Additional timer 3 and timer 4 for 2 Baud Rate Generator
- 8 Extended Interrupt Units INT7~INT14
- Support IR receiver and IRQ output
- Internal ISP ROM Boot Selection
- SPI DMA Read/Write XMEM

Control register for MCU Operation

- SPI Flash Mode for MCU program fetch - 0x4C0 (bit2-0)
- SPI Clock Control - 0x4E1 (bit5-4), - 0x4E1 (bit2-0)
- MCU Cache Enable – SFR 0x9B (bit0)
- MCU Timer Clock Divider Control
  - 0x4E2, - 0x4E3 for Timer 0
  - 0x4E4, - 0x4E5 for Timer 1
  - 0x4E6, - 0x4E7 for Timer 2
  - 0x4E8, - 0x4E9 for Timer 3
  - 0x4EA, - 0x4EB for Timer 4
- Boot Strap Sequence
  TW8836 provides external boot select pin only for during device power up
- SPI DMA to MCU XMEM
  1.) Set SPI Flash Mode for DMA operation - 0x4C0 (bit2-0)
  2.) Set SPI DMA Length - {0x4DA, 0x4C8, 0x4C9}
  3.) Set SPI DMA Command - {0x4CA, 0x4CB, 0x4CC, 0x4CD, 0x4CE}
  4.) Set - 0x4C3 (bit7-6 = 2'b11) select DMA destination to MCU XMEM
  5.) Set - 0x4C3 (bit5-4) DMA access mode
  6.) Set - 0x4C4 (bit1) DMA read/write mode
  7.) Set - 0x4C6 (bit3-0), - 0x4C7 (bit7-0) for destination start address
  8.) Set - 0x4C4 (bit0 = 1) to start DMA execution

TW8836 MCU Block Diagram



Microcontroller Interface

The host interface is accessed via 2-wire serial bus interface. It always operates as a slave device.

TWO WIRE SERIAL BUS INTERFACE

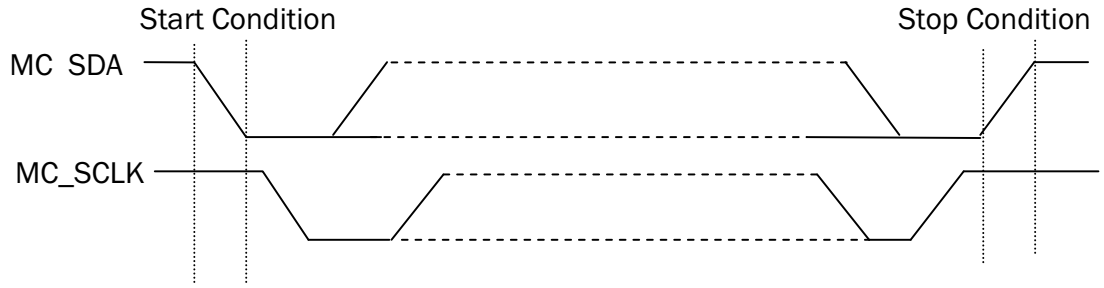


FIGURE 4. DEFINITION OF THE SERIAL BUS INTERFACE BUS START AND STOP

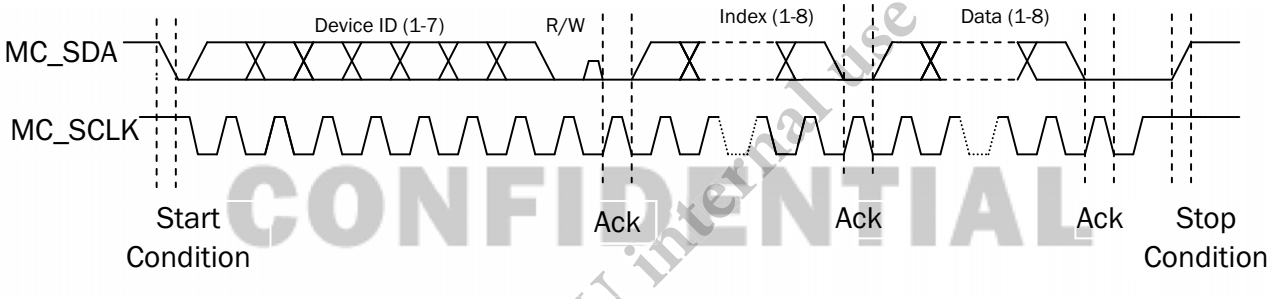


FIGURE 5. ONE COMPLETE REGISTER WRITE SEQUENCE VIA THE SERIAL BUS INTERFACE

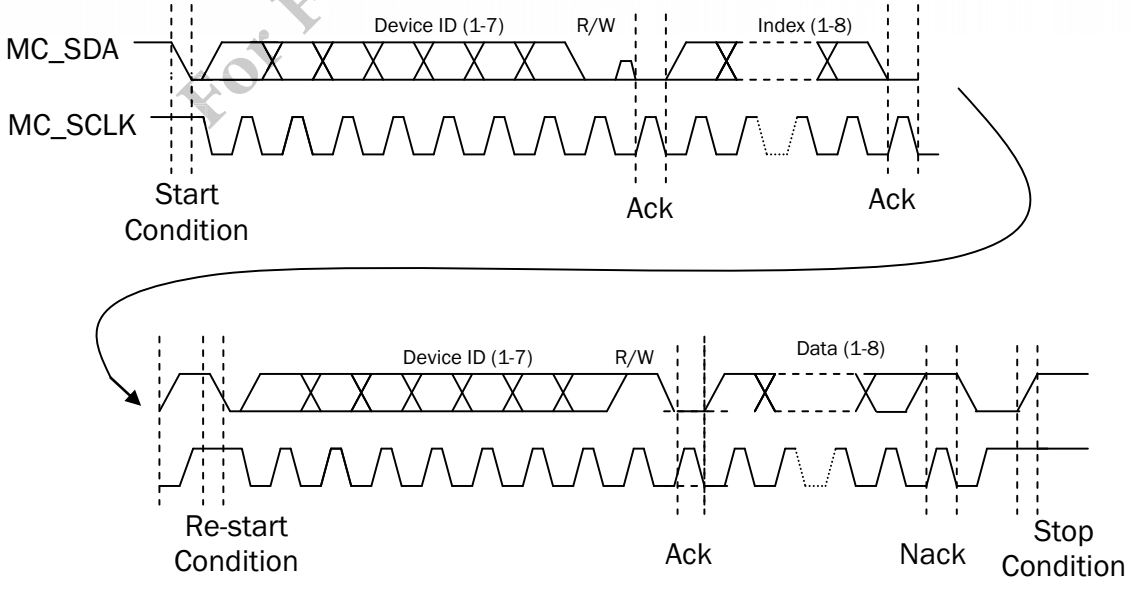


FIGURE 6. ONE COMPLETE REGISTER READ SEQUENCE VIA THE SERIAL BUS INTERFACE

The two wire serial bus interface is used to allow an external micro-controller to write control data to, and read control or other information from the internal registers. MC_SCLK is the serial clock and MC_SDA is the data line. Both lines are pulled high by resistors connected to VDD. Ics communicate on the bus by pulling MC_SCLK and MC_SDA low through open drain outputs. In normal operation the master generates all clock pulses, but control of the MC_SDA line alternates back and forth between the master and the slave. For both read and write, each byte is transferred MSB first, and the data bit is valid whenever MC_SCLK is high.

The device is operated as a bus slave device. The 7-bit device address field is fixed and concatenated with the read/write control bit to form the first byte transferred during a new transfer. If the read/write control bit is high the next byte will be read from the slave device. If it is low the next byte will be a write to the slave. When a bus master (the host microprocessor) drives MC_SDA from high to low, while MC_SCLK is high, this is defined to be a start condition (See Figure 4). All slaves on the bus listen to determine when a start condition has been asserted.

After a start condition, all slave devices listen for their device addresses. The host then sends a byte consisting of the 7-bit slave device ID and the R/W bit. This is shown in Figure 5. (The next byte is normally the index to the internal registers and is a write to the device therefore the first R/W bit is normally low.)

After transmitting the device address and the R/W bit, the master must release the MC_SDA line while holding MC_SCLK low, and wait for an acknowledgement from the slave. If the address matches the device address of a slave, the slave will respond by driving the MC_SDA line low to acknowledge the condition. The master will then continue with the next 8-bit transfer. If no device on the bus responds, the master transmits a stop condition and ends the cycle. Notice that a successful transfer always includes nine clock pulses.

To write to the internal register, the master sends another 8-bit of data, it loads this to the register pointed by the internal index register. The device will acknowledge the 8-bit data transfer and automatically increment the index in preparation for the next data. The master can do multiple writes if they are in ascending sequential order. After each 8-bit transfer the device will acknowledge the receipt of the 8-bits with an acknowledgement pulse. To end all transfers, the host has to issue a stop condition.

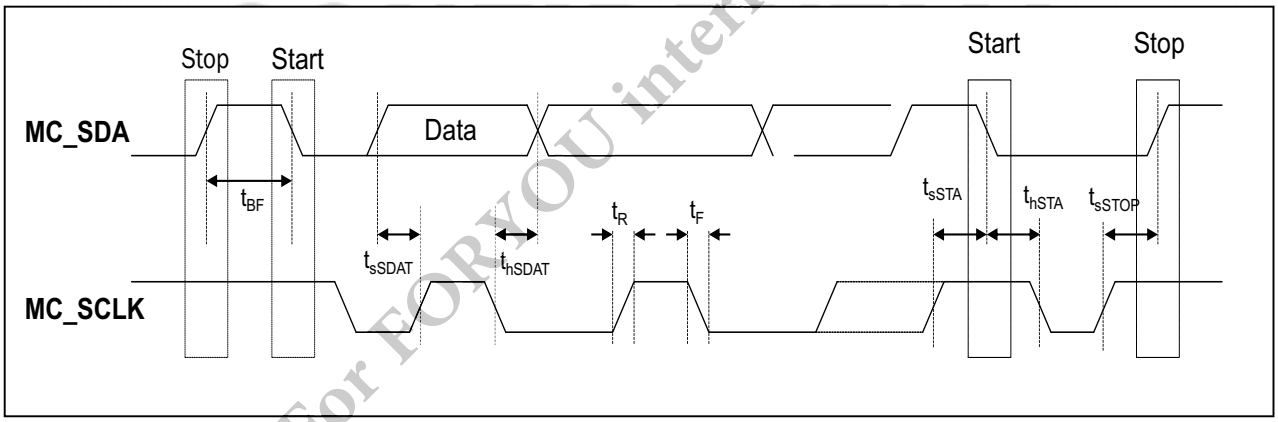
TABLE 3. SERIAL BUS INTERFACE 7-BIT SLAVE ADDRESS AND READ WRITE BIT

Serial Bus Interface 7-bit Slave Address							Read/Write bit
1	0	0	0	1	0	1	1=Read 0=Write

The device read cycle has two phases. The first phase is a write to the internal index register. The second phase is the read from the data register. (See Figure 6). The host initiates the first phase by sending the start condition. It then sends the slave device ID together with a 0 in the R/W bit position. The index is then sent followed by either a stop condition or a second start condition. The second phase starts with the second start condition. The master then resends the same slave device ID with a 1 in the R/W bit position to indicate a read. The slave will transfer the contents of the desired register. The master remains in control of the clock. After transferring eight bits, the slave releases and the master takes control of the MC_SDA line and acknowledge the receipt of data to the slave. To terminate the last transfer the master will issue a negative acknowledge (MC_SDA is left high during a clock pulse) and issue a stop condition.

TABLE 4. SERIAL BUS INTERFACE TIMING

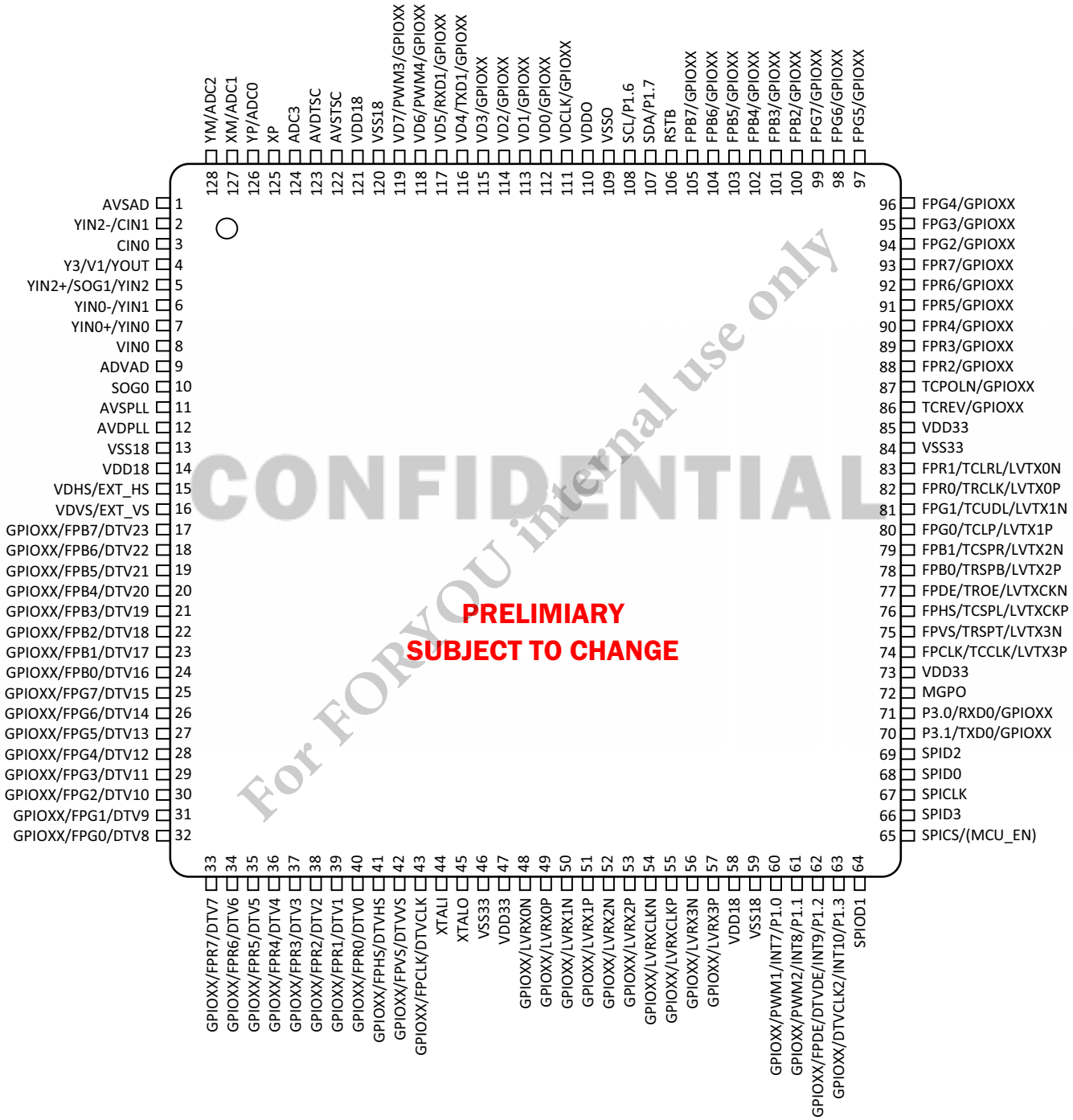
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
Bus Free Time between STOP and START	t_{BF}	740	-	-	ns
MC_SDA setup time	t_{sSDAT}	74	-	-	ns
MC_SDA hold time	t_{hSDAT}	50	-	900	ns
Setup time for START condition	t_{sSTA}	370	-	-	ns
Setup time for STOP condition	t_{sSTOP}	370	-	-	ns
Hold time for START condition	t_{hSTA}	74	-	-	ns
Rise time for MC_SCLK and MC_SDA	t_R	-	-	300	ns



SERIAL BUS INTERFACE TIMING

Pin Diagram

TW8836 128 PIN LQFP (TOP-VIEW)

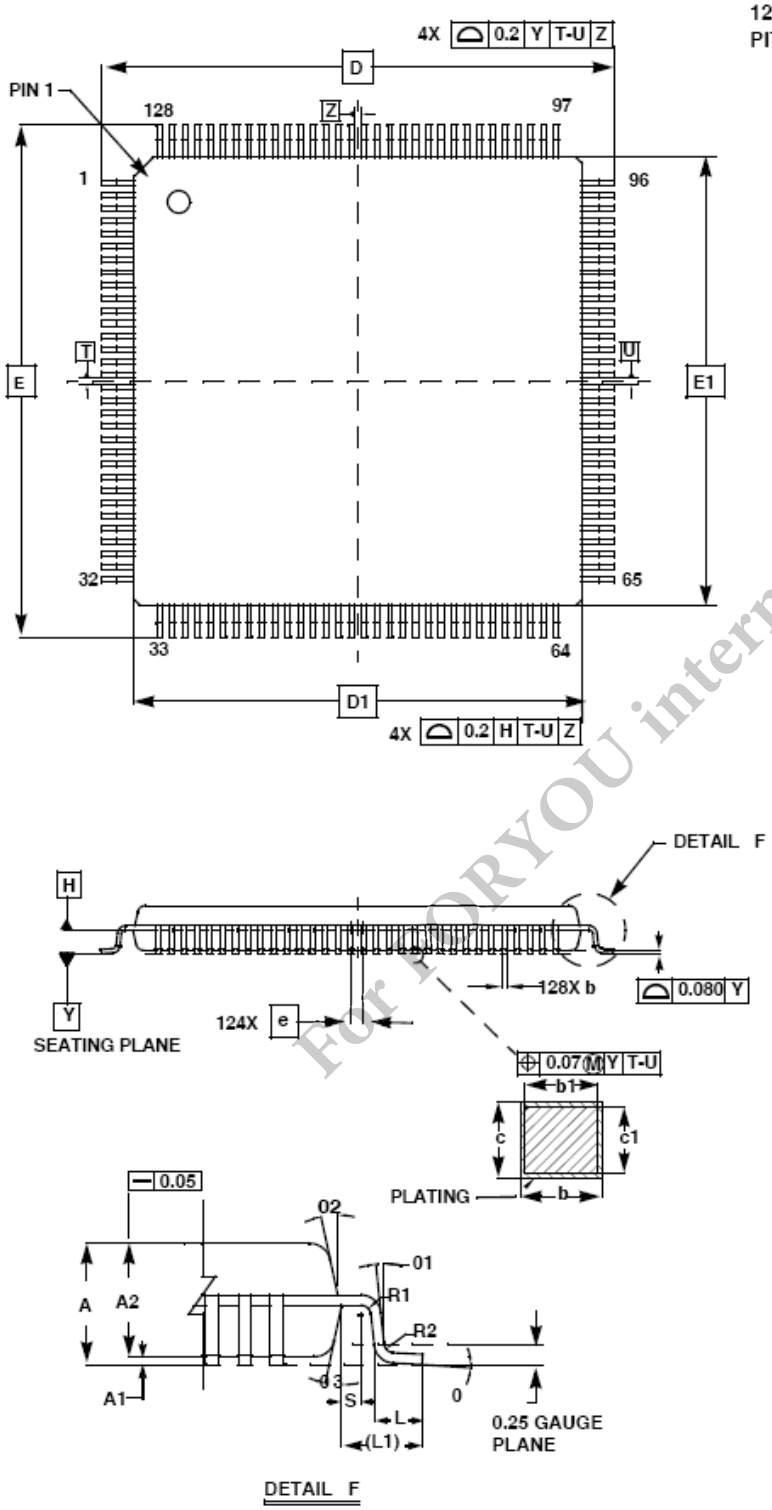


PRELIMIARY
SUBJECT TO CHANGE

Pin Descriptions (TBA)

Package Outline Drawing 1

Q128.14x14: 128 Lead Low Plastic Quad Flatpack Package (LQFP) 0.4mm pitch



Q128.14x14

128 LEAD LOW PLASTIC QUAD FLATPACK PACKAGE .4 MM PITCH

SYMBOL	MILLIMETERS			NOTES
	MIN	NOM	MAX	
A	-		1.60	-
A1	0.05		0.15	-
A2	1.35	1.40	1.45	-
b	0.13	0.16	0.23	4
b1	0.13	-	0.19	-
c	0.09	-	0.20	-
c1	0.09	-	0.16	-
D	16 BSC			-
D1	14 BSC			3
E	16 BSC			-
E1	14 BSC			3
L	0.45	0.60	0.75	-
L1	1.00 REF			-
R1	0.08	-	-	-
R2	0.08	-	0.20	-
S	0.20	-	-	-
0	0°	3.5°	7°	-
01	0°	-	-	-
02	11°	12°	13°	-
03	11°	12°	13°	-
N	128			-
e	0.40 BSC			-

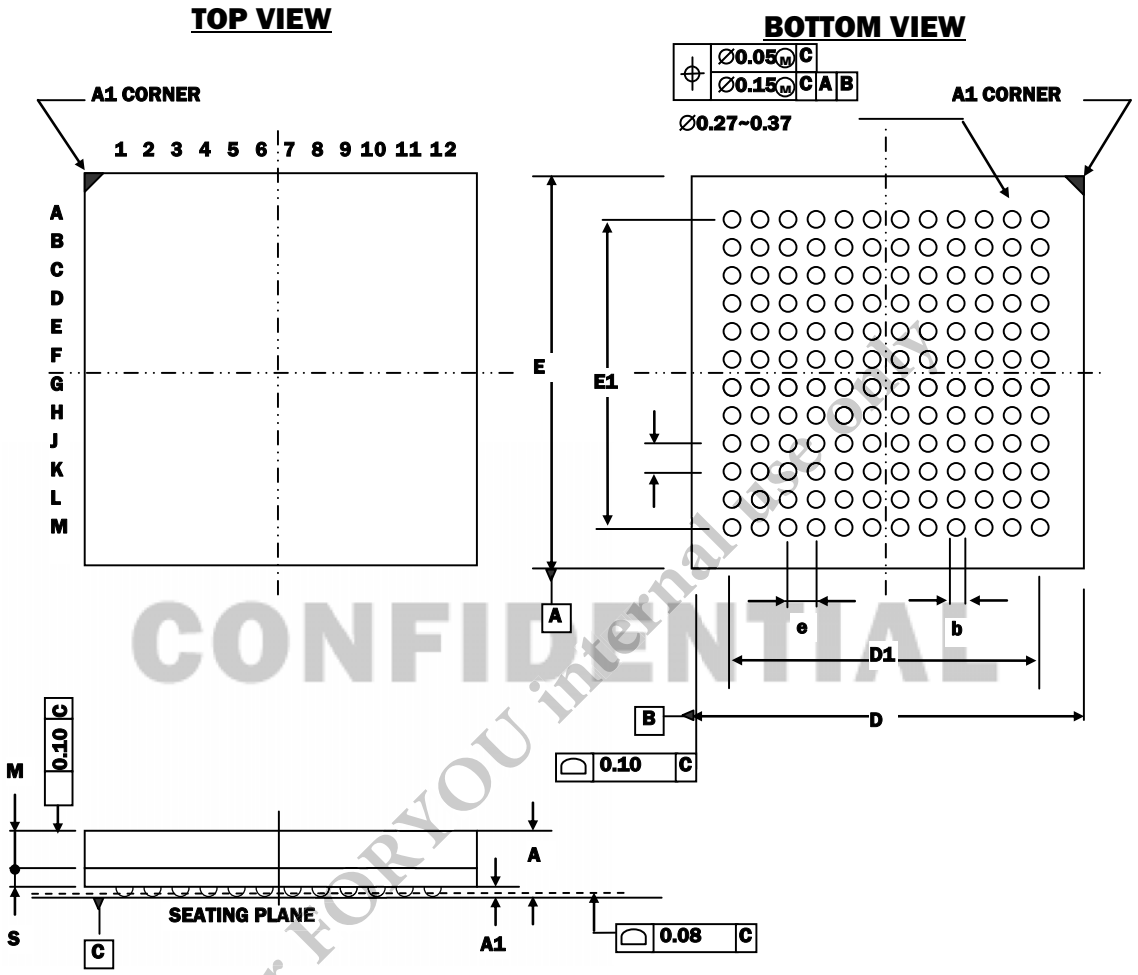
Rev. 1 7/11

NOTES:

1. Dimensions are in millimeters. Dimensions in ( ) for Reference Only.
2. Dimensions and tolerances per AMSEY14.5M-1994.
3. Dimensions D1 and E1 are excluding mold protrusion. Allowable protrusion is 0.25 per side. Dimensions D1 and E1 are exclusive of mold mismatch and determined by datum plane H.
4. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm. Dambar cannot be located at the lower radius or the foot. Minimum space between protrusion and an adjacent lead is 0.07 mm.

Package Outline Drawing 2

V144.7X7A : 144 Lead Thin, Fine Pitch Plastic ball Grid Array Package (TFBGA) Rev 0, 1/11



Symbol	Millimeter		
	Min.	Nom.	Max.
A	---	---	1.20
A1	0.16	---	0.26
M		0.53 Ref.	
S		0.26 Ref.	
b	0.27	0.30	0.37
e		0.50 Basic	
D	6.90	7.00	7.10
D1	---	5.50	---
E	6.90	7.00	7.10
E1	---	5.50	---

NOTE:
1. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
2. Dimension b is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Controlling dimension : Millimeter.

Parametric Information

PRELIMINARY ESTIMATES
SUBJECT TO CHANGE

AC/DC Electrical Parameters

TABLE 5. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
V_{DDA18} (Measured to V_{SSA18}) 1.8V (Note 1)	VDDAM	-	-	1.98	V
V_{DDA33} (Measured to V_{SSA33}) 3.3V (Note 1)	VDDA33M	-	-	3.6	V
V_{DD18} (Measured to V_{SS18}) 1.8V (Note 1)	VDD18M	-	-	1.98	V
V_{DD33} (Measured to V_{SS33}) 3.3V	VDD33M	-	-	3.6	V
Voltage on any Digital Signal Pin (See the note below)	-	V_{SS33} – 0.5	-	5.5	V
Analog Input Voltage (Supplied by 1.8V)	-	V_{SSA18} – 0.5	-	1.98	V
Storage Temperature	T_S	–65	-	+150	°C
Junction Temperature	T_J	-	-	+125	°C
Reflow Soldering	Tpeak	255 +5/-0 (10~30 seconds)			°C

NOTE:

1. VDDA18: AVDAD, AVDPLL
   VSSA18: AVSAD, AVSPLL
   V_{DDA33}: AVDTSC
   V_{SSA33}: AVSTSC
   V_{DD33}: VDD33
   V_{SS33}VSS33
   V_{DD18}: VDD18
   V_{SS18}: VSS18

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

This device employs high-impedance CMOS devices on all signal pins. It must be handled as an ESD-sensitive device. Voltage on any signal pin that exceeds the ranges list in Table 5 can induce destructive latch-up.

PARAMETER	SYMBOL	MIN (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	TYP	MAX (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	UNITS
SUPPLY					
Power Supply — IO 3.3V	V_{DD33}	3.15	3.3	3.6	V
Power Supply — Digital Core 1.8V	V_{DD18}	1.62	1.8	1.98	V
Power Supply — Analog 3.3V	V_{DDA33}	3.15	3.3	3.6	V
Power Supply — Analog 1.8V	V_{DDA18}	1.62	1.8	1.98	V
Ambient Operating Temperature	T_A	-40	-	+105	°C
Analog Supply Current 1.8V (CVBS)	Iaa18	-	38.2	-	mA
(Component 1080p)	Iaa18		189.3		mA
(DTV 1080p)	Iaa18		13		mA
Analog Supply Current 3.3V	Iaa33	-	3.6	-	mA
Digital I/O Supply Current 3.3V (Note **Error! Reference source not found.**)	Idd33	-	30	-	mA
Digital Core Supply Current(Note2) (CVBS, 27MHz)	Idd18	-	116	-	mA
(CVBS, 108MHz)	Idd18	-	141	-	mA
(Component 1080p, 108MHz)	Idd18	-	161	-	mA
(DTV 1080p, 108MHz)	Idd18	-	146	-	mA

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Digital I/O and core power supply current measurement is base on WVGA input (40MHz clock rate) with SMPTE pattern.

PARAMETER	SYMBOL	MIN (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	TYP	MAX (NOTE 1)	UNITS
DIGITAL INPUTS					
Input High Voltage (TTL)	V_{IH}	2.0	-	-	V
Input Low Voltage (TTL)	V_{IL}	-	-	0.8	V
Input High Voltage (XTI)	V_{IH}	2.0	-	V_{DD33} + 0.5	V
Input Low Voltage (XTI)	V_{IL}	-	-	0.8	V
Input High Current (V_{IN} = V $_{DD}$)	I_{IH}	-	-	10	µA
Input Low Current (V_{IN} = VSS)	I_{IL}	-	-	–10	µA
Input Capacitance (f = 1 MHz, V_{IN} = 2.4 V)	C_{IN}	-	5	-	pF
DIGITAL OUTPUTS					
Output High Voltage (I_{OH} = –4mA)	V_{OH}	2.4	-	V_{DD33}	V
Output Low Voltage (I_{OL} = 4mA)	V_{OL}	-	0.2	0.4	V
3-State Current	I_{OZ}	-	-	10	µA
Output Capacitance	C_O	-	5	-	pF

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

PARAMETER	SYMBOL	MIN (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	TYP	MAX (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	UNITS
ANALOG INPUT					
Analog Pin Input Voltage	Vi	-	1	-	Vpp
YIN0, YIN1, YIN2 and YIN3 Input Range (AC Coupling Required)		0.5	1.0	2.0	Vpp
CIN0, CIN1 Amplitude Range (AC Coupling Required)		0.5	1.0	2.0	Vpp
VIN0, VIN1 Amplitude Range (AC Coupling Required)		0.5	1.0	2.0	Vpp
SOG0, SOG1 Input Range		0.02	0.3	1.8	V
LEDS Input Range		-	-	-	V
DCDCS		-	-	-	V
Analog Pin Input Capacitance	C_A	-	7	-	pF
ADCS					
ADC Resolution	ADCR	-	9	-	Bits
ADC Integral Non-linearity	AINL	-	±1	-	LSB
ADC Differential non-linearity	ADNL	-	±1	-	LSB
ADC Clock Rate	f_{ADC}	-	27	60	MHz
Video Bandwidth (-3db)	BW	-	9	-	MHz

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

PARAMETER	SYMBOL	MIN (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	TYP	MAX (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	UNITS
HORIZONTAL PLL					
Line Frequency (50Hz)	f_{LN}	-	15.625	-	KHz
Line Frequency (60Hz)	f_{LN}	-	15.734	-	KHz
Static Deviation	Δf_H	-	-	6.2	%
SUBCARRIER PLL					
Subcarrier Frequency (NTSC-M)	f_{SC}	-	3579545	-	Hz
Subcarrier Frequency (PAL-BDGHI)	f_{SC}	-	4433619	-	Hz
Subcarrier Frequency (PAL-M)	f_{SC}	-	3575612	-	Hz
Subcarrier Frequency (PAL-N)	f_{SC}	-	3582056	-	Hz
Lock In Range	Δf_H	±450	-	-	Hz
CRYSTAL SPEC					
Nominal Frequency (Fundamental)		-	27	-	MHz
Deviation		-	-	±50	ppm
Load Capacitance	CL	-	20	-	pF
Series Resistor	RS	-	80	-	Ω

NOTE:

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Crystal Deviation crossover normal operation temperature range.

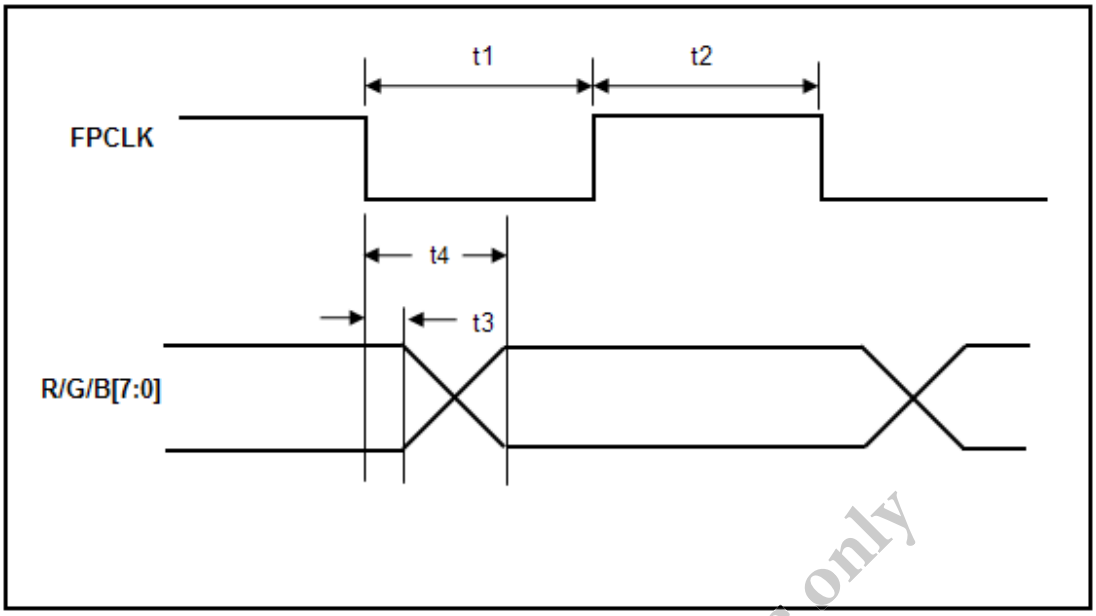


TABLE 6. OUTPUT TIMING

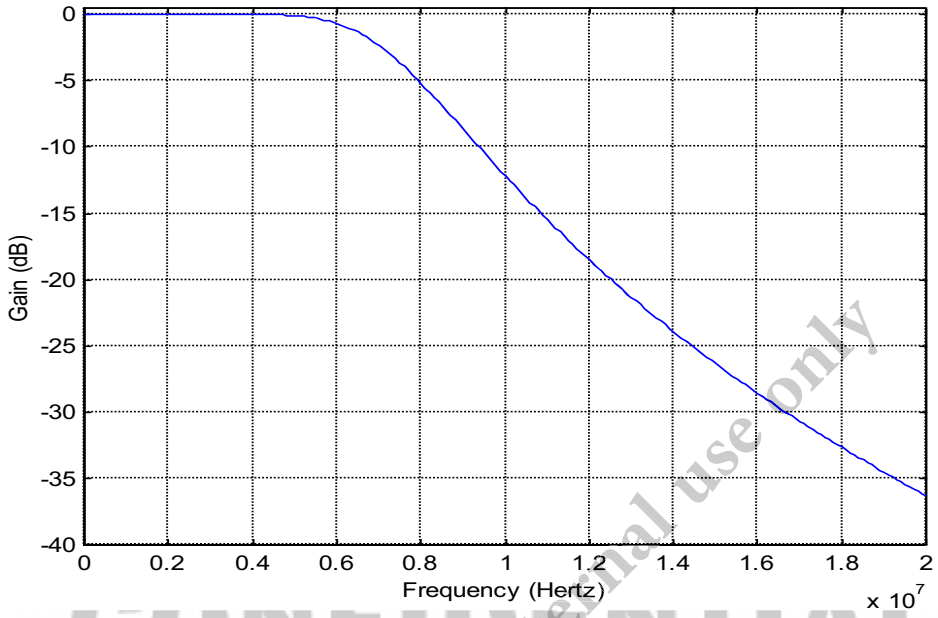
PARAMETER	SYMBOL	TEST CONDITIONS	MIN (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	TYP	MAX (NOTE ERROR! REFERENCE SOURCE NOT FOUND.)	UNIT
Duty Cycle FPCLK		FPCLK DIV = 0	40%	50%	60%	
FPCLK Low Time	t1	FPCLK = 9~80MHz	6.7	-	66.7	ns
FPCLK High Time	t2	FPCLK = 9~80MHz	6.7	-	66.7	ns
Output Hold Time	t3	FPCLK Div = 0, Pol = low	6.0	-	-	ns
		FPCLK Div = 1, Pol = low	9.0	-	-	ns
		FPCLK Div = 2, Pol = high	21.0	-	-	ns
		FPCLK Div = 3, Pol = low	34.5	-	-	ns
Output Delay Time	t4	FPCLK Div = 0, Pol = low	-	10.5	14.5	ns
		FPCLK Div = 1, Pol = low	-	13.5	17.5	ns
		FPCLK Div = 2, Pol = high	-	25.5	29.5	ns
		FPCLK Div = 3, Pol = low	-	39.5	43.5	ns

NOTE:

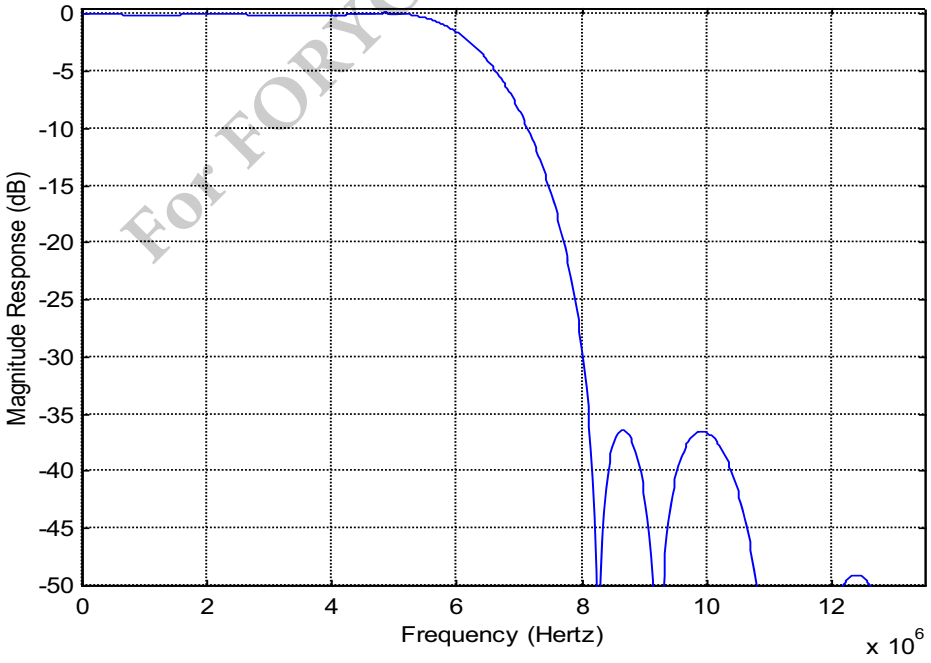
1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

Filter Curves

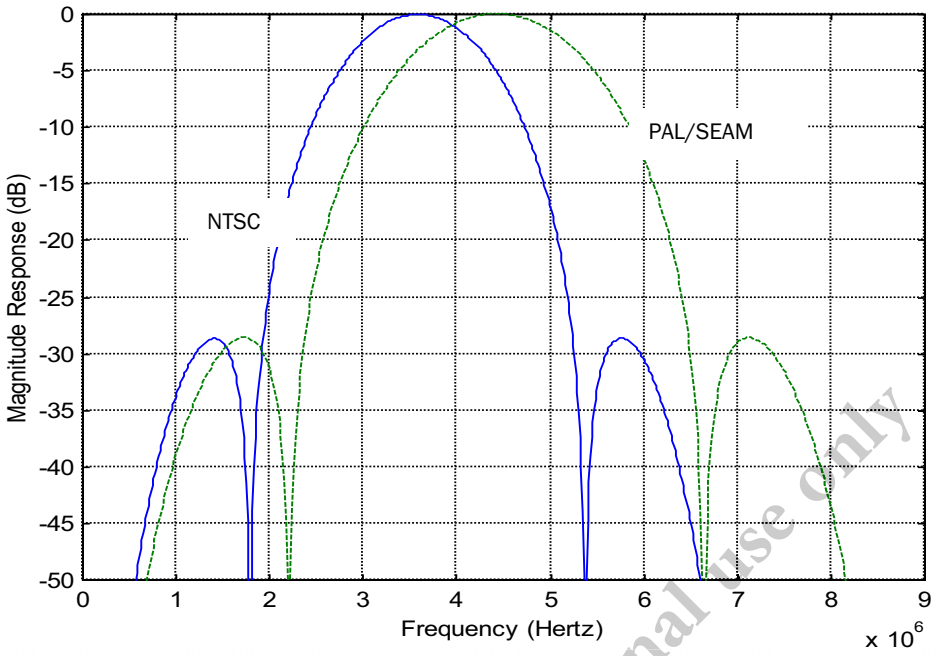
ANTI-ALIAS FILTER



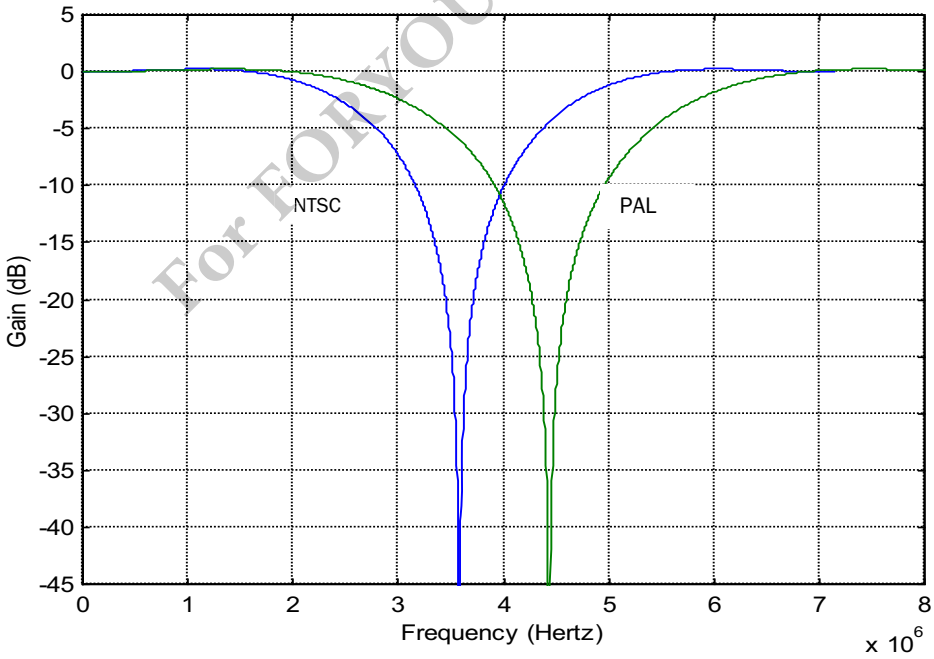
DECIMATION FILTER



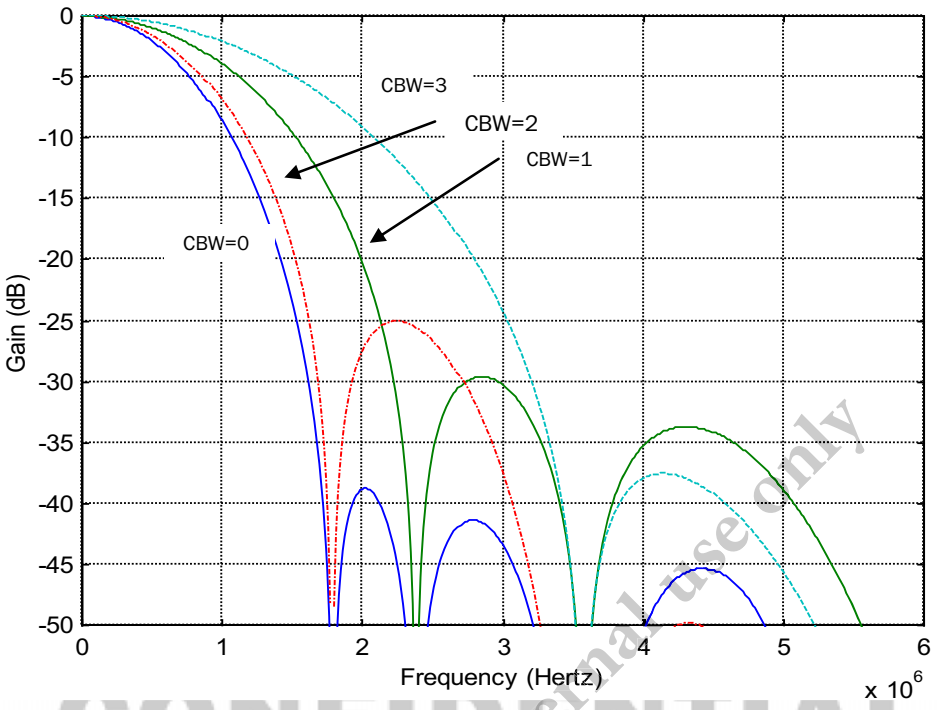
CHROMA BAND PASS FILTER CURVES



LUMA NOTCH FILTER CURVE FOR NTSC AND PAL



CHROMINANCE LOW-PASS FILTER CURVE



TW8836 Register Summary (TBA)

Life Support Policy

These products are not authorized for use as critical components in life support devices or systems.

Revision History

DATE	REVISION	CHANGE
April 2, 2012	0.3	Initial Preliminary Version Release
May 17, 2012	0.4	Updated block diagram and pin assignment
June 29, 2012	0.5	Insterted LVDS Rx information