# VLSI

## VLSI Technology, Inc.

## T1/E1 QUAD LINE INTERFACE UNIT

## FEATURES

• Four analog PCM line interfaces for T1 and E1 (CEPT) applications

• Four jitter attenuators, individually selectable for Tx or Rx direction

• Single external crystal reduces board cost and space requirements

• Standard 8-bit microprocessor interface with separate address, data, and control buses

• System interrupt for Tx monitor performance, LOS, AIS and FIFO overflow alarms

• Supports popular DS1/E1 framers

• Plastic surface-mount packaging: 144-pin Plastic Quad Flat Package (PQFP)

• Submicron CMOS technology (725 mW typ., 1.2 W worst-case)

• Functionally compatible with all industry-standard, single-channel transceivers

• Meets Bellcore TR499 and AT&T 62411 specifications

• Transmit pulse shaping per DSX-1 pulse template: 0 to 655 feet

• Transmit pulse shaping per CCITT G.703 pulse templates

• Integrates AMI, B8ZS, and HDB3 encoder/decoder

• Capable of local and remote loopback data path configuration

## APPLICATIONS

• n x T1/E1 access multiplexers and channel extenders

• Automatic protection switch front end designs

• High-density M01/M12/M13/EDSX cross-connect interfacing

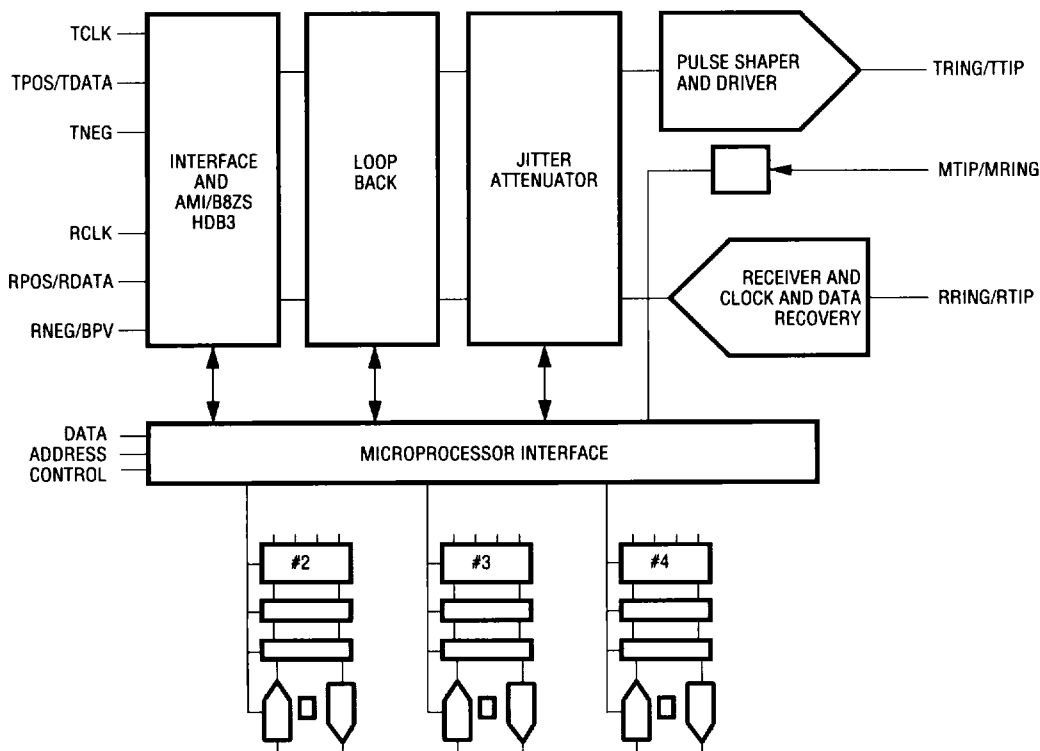• High-density, portable test equipment

## DESCRIPTION

The VNS14Q575 provides a single integrated solution for high-density T1/E1 short-haul transceiver applications. From a single clock, the VNS14Q575 terminates four PCM interfaces. Both DSX-1 (ANSI) or E1/CEPT (CCITT) formats are supported.

The VNS14Q575 jitter attenuation is user-selectable for transmit or receive directions on a per channel basis. A microprocessor interface, common to all four transceivers, provides extensive monitoring, loopback, and control capabilities.

Comprehensive monitoring features are included which allows visibility of all critical parameters. Advanced submicron CMOS processing and plastic surface-mount packaging offer substantial savings in power dissipation and system component cost. (See block diagram below.) The VNS14Q575 supports hardware mode operation for implementations with pin-selectable feature control.

## BLOCK DIAGRAM

## PIN DESCRIPTION

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| TPOS1/TDATA1 | INPUT | 141 | During Hardware Mode (Mode1=0), a high level on TPOS1 corresponds to a positive pulse on TTIP1 and TRING1. TPOS1 is sampled on falling edge of TCLK1. During Extended Hardware Mode (Mode1=1), the input TDATA1 passes through the line code encoder and is then driven on to the line through TTIP1 and TRING1. TDATA1 is sampled on the falling edge of TCLK1. |
| TPOS2/TDATA2 | INPUT | 144 | During Hardware Mode (Mode2=0), a high level on TPOS2 corresponds to a positive pulse on TTIP2 and TRING2. TPOS2 is sampled on falling edge of TCLK2. During Extended Hardware Mode (Mode2=1), the input TDATA2 passes through the line code encoder and is then driven on to the line through TTIP2 and TRING2. TDATA2 is sampled on the falling edge of TCLK2. |
| TPOS3/TDATA3 | INPUT | 23 | During Hardware Mode (Mode3=0), a high level on TPOS3 corresponds to a positive pulse on TTIP3 and TRING3. TPOS3 is sampled on falling edge of TCLK3. During Extended Hardware Mode (Mode3=1), the input TDATA3 passes through the line code encoder and is then driven on to the line through TTIP3 and TRING3. TDATA3 is sampled on the falling edge of TCLK3. |
| TPOS4/TDATA4 | INPUT | 26 | During Hardware Mode (Mode4=0), a high level on TPOS4 corresponds to a positive pulse on TTIP4 and TRING4. TPOS4 is sampled on falling edge of TCLK4. During Extended Hardware Mode (Mode4=1), the input TDATA4 passes through the line code encoder and is then driven on to the line through TTIP4 and TRING4. TDATA4 is sampled on the falling edge of TCLK4. |
| TNEG1 | INPUT | 140 | During Hardware Mode (Mode1=0), a high level on TNEG1 corresponds to a negative pulse on TTIP1 and TRING1. TNEG1 is sampled on the falling edge of TCLK1. During Extended Hardware Mode (Mode1=1), the input is ignored. |
| TNEG2 | INPUT | 143 | During Hardware Mode (Mode2=0), a high level on TNEG2 corresponds to a negative pulse on TTIP2 and TRING2. TNEG2 is sampled on the falling edge of TCLK2. During Extended Hardware Mode (Mode2=1), the input is ignored. |
| TNEG3 | INPUT | 24 | During Hardware Mode (Mode3=0), a high level on TNEG3 corresponds to a negative pulse on TTIP3 and TRING3. TNEG3 is sampled on the falling edge of TCLK. During Extended Hardware Mode (Mode3=1), the input is ignored. |
| TNEG4 | INPUT | 27 | During Hardware Mode (Mode4=0), a high level on TNEG4 corresponds to a negative pulse on TTIP4 and TRING4. TNEG4 is sampled on the falling edge of TCLK4. During Extended Hardware Mode (Mode4=1), the input is ignored. |
| TCLK1 | INPUT | 142 | Transmit clock input for LIU #1. TPOS1/TDATA1 and TNEG1 are sampled on the falling edge of TCLK1. TCLK1 has a frequency of 1.544 MHz ± 32 ppm for DS1 and 2.048 MHz ± 50 ppm for CEPT. |
| TCLK2 | INPUT | 1 | Transmit clock for LIU #2. TPOS2/TDATA2 and TNEG2 are sampled on the falling edge of TCLK2. TCLK2 has a frequency of 1.544 MHz ± 32 ppm for DS1 and 2.048 MHz ± 50 ppm for CEPT. |
| TCLK3 | INPUT | 22 | Transmit clock for LIU #3. TPOS3/TDATA3 and TNEG3 are sampled on the falling edge of TCLK3. TCLK3 has a frequency of 1.544 MHz ± 32 ppm for DS1 and 2.048 MHz ± 50 ppm for CEPT. |
| TCLK4 | INPUT | 25 | Transmit clock for LIU #4. TPOS4/TDATA4 and TNEG4 are sampled on the falling edge of TCLK4. TCLK4 has a frequency of 1.544 MHz ± 32 ppm for DS1 and 2.048 MHz ± 50 ppm for CEPT. |
| RPOS1/RDATA1 | OUTPUT | 135 | During Hardware Mode (Mode1=0), a high level on RPOS1 corresponds to a positive pulse on RTIP1 and RRING1. The output is valid on the rising edge of RCLK1. During Extended Hardware Mode (Mode1=1), data recovered from the RTIP1 and RRING1 inputs is output on RDATA1 after being decoded by the line decoder. RDATA1 is NRZ data and is stable and valid on the falling edge of RCLK1. |

## PIN DESCRIPTION (Cont.)

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| RPOS2/RDATA2 | OUTPUT | 128 | During Hardware Mode (Mode2=0), a high level on RPOS2 corresponds to a positive pulse on RTIP2 and RRING2. The output is valid on the rising edge of RCLK2. During Extended Hardware Mode (Mode2=1), data recovered from the RTIP2 and RRING2 inputs is output on RDATA2 after being decoded by the line decoder. RDATA2 is NRZ data and is stable and valid on the falling edge of RCLK2. |
| RPOS3/RDATA3 | OUTPUT | 38 | During Hardware Mode (Mode3=0), a high level on RPOS3 corresponds to a positive pulse on RTIP3 and RRING3. The output is valid on the rising edge of RCLK3. During Extended Hardware Mode (Mode3=1), data recovered from the RTIP3 and RRING3 inputs is output on RDATA3 after being decoded by the line decoder. RDATA3 is NRZ data and is stable and valid on the falling edge of RCLK3. |
| RPOS4/RDATA4 | OUTPUT | 43 | During Hardware Mode (Mode4=0), a high level on RPOS4 corresponds to a positive pulse on RTIP4 and RRING4. The output is valid on the rising edge of RCLK4. During Extended Hardware Mode (Mode4=1), data recovered from the RTIP4 and RRING4 inputs is output on RDATA4 after being decoded by the line decoder. RDATA4 is NRZ data and is stable and valid on the falling edge of RCLK4. |
| RCLK1 | OUTPUT | 136 | RCLK1 is the clock signal recovered from the signal received at RTIP1 and RRING1. |
| RCLK2 | OUTPUT | 129 | RCLK2 is the clock signal recovered from the signal received at RTIP2 and RRING2. |
| RCLK3 | OUTPUT | 37 | RCLK3 is the clock signal recovered from the signal received at RTIP3 and RRING3. |
| RCLK4 | OUTPUT | 42 | RCLK4 is the clock signal recovered from the signal received at RTIP4 and RRING4. |
| RNEG1/BPV1 | OUTPUT | 134 | During Hardware Mode (Mode1=0), a high level on RNEG1 corresponds to a negative pulse on RTIP1 and RRING1. The output is valid on the rising edge of RCLK1. During Extended Hardware Mode (Mode1=1), the Bipolar Violation Strobe BPV1 goes high for one bit period when a bipolar violation is detected in the received signal. |
| RNEG2/BPV2 | OUTPUT | 127 | During Hardware Mode (Mode2=0), a high level on RNEG2 corresponds to a negative pulse on RTIP2 and RRING2. The output is valid on the rising edge of RCLK2. During Extended Hardware Mode (Mode2=1), the Bipolar Violation Strobe BPV2 goes high for one bit period when a bipolar violation is detected in the received signal. |
| RNEG3/BPV3 | OUTPUT | 39 | During Hardware Mode (Mode3=0), a high level on RNEG3 corresponds to a negative pulse on RTIP3 and RRING3. The output is valid on the rising edge of RCLK3. During Extended Hardware Mode (Mode3=1), the Bipolar Violation Strobe BPV3 goes high for one bit period when a bipolar violation is detected in the received signal. |
| RNEG4/BPV4 | OUTPUT | 44 | During Hardware Mode (Mode4=0), a high level on RNEG4 corresponds to a negative pulse on RTIP4 and RRING4. The output is valid on the rising edge of RCLK4. During Extended Hardware Mode (Mode4=1), the Bipolar Violation Strobe BPV4 goes high for one bit period when a bipolar violation is detected in the received signal. |
| CSN | INPUT | 15 | Active low chip select is low during QLIU register access. |
| RDN | INPUT | 16 | Active low read enable signal is low during read access. The microprocessor data bus is driven with the addressed register's contents while RDN and CSN are both low. |
| WRN | INPUT | 17 | Active low write enable signal is low during write access. The contents of the data bus are latched into the addressed register on the rising edge of WRN while CSN is low. |
| D[7] | I/O | 3 | Bit 7 of bidirectional microprocessor data bus. |
| D[6] | I/O | 4 | Bit 6 of bidirectional microprocessor data bus. |
| D[5] | I/O | 5 | Bit 5 of bidirectional microprocessor data bus. |
| D[4] | I/O | 6 | Bit 4 of bidirectional microprocessor data bus. |
| D[3] | I/O | 7 | Bit 3 of bidirectional microprocessor data bus. |
| D[2] | I/O | 8 | Bit 2 of bidirectional microprocessor data bus. |

## PIN DESCRIPTION (Cont.)

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| D[1] | I/O | 9 | Bit 1 of bidirectional microprocessor data bus. |
| D[0] | I/O | 10 | Bit 0 of bidirectional microprocessor data bus. |
| INTN | OUTPUT | 2 | Active low interrupt to the microprocessor. INTN goes low when LOS, AIS, DPM, or jitter attenuator over/underflow conditions are detected. INTN remains asserted until the LOS, AIS or DPM register (depending on the interrupt cause) is read, unless the condition that caused the interrupt is still true, in which case, INTN remains asserted. |
| RESET | INPUT | 139 | Active high reset input. When RESET is asserted high, the whole chip is reset and the internal registers take on the values indicated in Table 7 on page 13. RESET should be asserted for a minimum period of 1 ms. |
| TEST | INPUT | 32 | Active high test-mode input. When TEST is high, the QLIU is in factory test mode. This input should be connected to ground during normal operation. |
| A[3] | INPUT | 18 | Bit 3 of microprocessor address bus. |
| A[2] | INPUT | 19 | Bit 2 of microprocessor address bus. |
| A[1] | INPUT | 20 | Bit 1 of microprocessor address bus. |
| A[0] | INPUT | 21 | Bit 0 of microprocessor address bus. |
| XTALIN | INPUT | 13 | High speed clock input. This input must be driven by a 50 MHz clock signal having 40/60% duty cycle symmetry (at VDD/2 level) and 25 ppm frequency stability. If CLKX2N is asserted high, however, a 100 MHz clock having at least 30/70% duty cycle and 25 ppm frequency stability must be applied. |
| CLKX2N | INPUT | 14 | When this input is high, the internal clock doubling circuitry is bypassed. This input would be held high if the 100 MHz clock required by various blocks within the QLIU was provided by the system at the XTALIN pin. In normal operation, this pin is left floating (there is an internal pull down resistor), so that the 50 MHz applied at XTALIN is doubled. |
| FRLOOP | INPUT | 31 | FRLOOP high puts all four LIU's into a remote loopback state, adds 25 clock cycles of delay to the remote loopback path, and disables local loopback and all data encoding modes. FRLOOP low enables normal loopback and data encoding modes. |
| JITMODE | INPUT | 30 | This pin selects between two jitter attenuation modes. When JITMODE is high, the jitter attenuators (of all four LIU's) meet the Bellcore TR499 specification. When JITMODE is low, the jitter attenuators meet the AT&T 62411 specification. |
| JITDIR1 | INPUT | 107 | Selects direction of jitter attenuator for LIU #1. When JITDIR1 is high, jitter attenuator is in the receive direction. When low, jitter attenuator is in the transmit direction. This pin is OR'd with the JITDIR1 bit in register 0x09. Therefore, if the JITDIR1 bit is set, this pin will have no effect. This input should be connected to analog VDD or VSS. It may also be switched using a DIP switch to VSS with a pull-up resistor to VDD or similar arrangement, but must not be driven by an active device. If not connected directly to VDD or VSS, the input must be decoupled with a 0.01 µF capacitor between this pin and analog VSS as close to the input pin as possible. |
| JITDIR2 | INPUT | 91 | Selects direction of jitter attenuator for LIU #2. When JITDIR2 is high, jitter attenuator is in the receive direction. When low, jitter attenuator is in the transmit direction. This pin is OR'd with the JITDIR2 bit in register 0x09. Therefore, if the JITDIR2 bit is set, this pin will have no effect. This input should be connected to analog VDD or VSS. It may also be switched using a DIP switch to VSS with a pull-up resistor to VDD or similar arrangement, but must not be driven by an active device. If not connected directly to VDD or VSS, the input must be decoupled with a 0.01 µF capacitor between this pin and analog VSS as close to the input pin as possible. |

## PIN DESCRIPTION (Cont.)

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| JITDIR3 | INPUT | 90 | Selects direction of jitter attenuator for LIU #3. When JITDIR3 is high, jitter attenuator is in the receive direction. When low, jitter attenuator is in the transmit direction. This pin is OR'd with the JITDIR3 bit in register 0x09. Therefore, if the JITDIR3 bit is set, this pin will have no effect. This input should be connected to analog VDD or VSS. It may also be switched using a DIP switch to VSS with a pull-up resistor to VDD or similar arrangement, but must not be driven by an active device. If not connected directly to VDD or VSS, the input must be decoupled with a 0.01 μF capacitor between this pin and analog VSS as close to the input pin as possible. |
| JITDIR4 | INPUT | 74 | Selects direction of jitter attenuator for LIU #4. When JITDIR4 is high, jitter attenuator is in the receive direction. When low, jitter attenuator is in the transmit direction. This pin is OR'd with the JITDIR4 bit in register 0x09. Therefore, if the JITDIR4 bit is set, this pin will have no effect. This input should be connected to analog VDD or VSS. It may also be switched using a DIP switch to VSS with a pull-up resistor to VDD or similar arrangement, but must not be driven by an active device. If not connected directly to VDD or VSS, the input must be decoupled with a 0.01 μF capacitor between this pin and analog VSS as close to the input pin as possible. |
| TTIP1 | OUTPUT | 100 | Positive bipolar transmit output data to the analog line interface for LIU #1. No data is transmitted when TCLK1 is not active. |
| TTIP2 | OUTPUT | 98 | Positive bipolar transmit output data to the analog line interface for LIU #2. No data is transmitted when TCLK2 is not active. |
| TTIP3 | OUTPUT | 83 | Positive bipolar transmit output data to the analog line interface for LIU #3. No data is transmitted when TCLK3 is not active. |
| TTIP4 | OUTPUT | 81 | Positive bipolar transmit output data to the analog line interface for LIU #4. No data is transmitted when TCLK4 is not active. |
| TRING1 | OUTUT | 103 | Negative bipolar transmit output data to the analog line interface for LIU #1. No data is transmitted when TCLK1 is not active. |
| TRING2 | OUTUT | 95 | Negative bipolar transmit output data to the analog line interface for LIU #2. No data is transmitted when TCLK2 is not active. |
| TRING3 | OUTUT | 86 | Negative bipolar transmit output data to the analog line interface for LIU #3. No data is transmitted when TCLK3 is not active. |
| TRING4 | OUTUT | 78 | Negative bipolar transmit output data to the analog line interface for LIU #4. No data is transmitted when TCLK4 is not active. |
| MTIP1 | INPUT | 60 | This input is used to monitor a TTIPx driver output. Any TTIPx output can be connected to MTIP1 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |
| MTIP2 | INPUT | 62 | This input is used to monitor a TTIPx driver output. Any TTIPx output can be connected to MTIP2 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |
| MTIP3 | INPUT | 64 | This input is used to monitor a TTIPx driver output. Any TTIPx output can be connected to MTIP3 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |
| MTIP4 | INPUT | 66 | This input is used to monitor a TTIPx driver output. Any TTIPx output can be connected to MTIP4 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |
| MRING1 | INPUT | 59 | This input is used to monitor a TRINGx driver output. Any TRINGx output can be connected to MRING1 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |
| MRING2 | INPUT | 61 | This input is used to monitor a TRINGx driver output. Any TRINGx output can be connected to MRING2 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |

## PIN DESCRIPTION (Cont.)

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| MRING3 | INPUT | 63 | This input is used to monitor a TRINGx driver output. Any TRINGx output can be connected to MRING3 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |
| MRING4 | INPUT | 65 | This input is used to monitor a TRINGx driver output. Any TRINGx output can be connected to MRING4 to monitor the output transceiver. This input is used by the Driver Performance Monitor to confirm that the transceiver for LIU #x is functioning. |
| RTIP1 | INPUT | 51 | Positive bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RRING1, then output on RPOS1, RNEG1 and RCLK1. |
| RTIP2 | INPUT | 54 | Positive bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RRING2, then output on RPOS2, RNEG2 and RCLK2. |
| RTIP3 | INPUT | 55 | Positive bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RRING3, then output on RPOS3, RNEG3 and RCLK3. |
| RTIP4 | INPUT | 58 | Positive bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RRING4, then output on RPOS4, RNEG4 and RCLK4. |
| RRING1 | INPUT | 52 | Negative bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RTIP1, then output on RPOS1, RNEG1 and RCLK1. |
| RRING2 | INPUT | 53 | Negative bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RTIP2, then output on RPOS2, RNEG2 and RCLK2. |
| RRING3 | INPUT | 56 | Negative bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RTIP3, then output on RPOS3, RNEG3 and RCLK3. |
| RRING4 | INPUT | 57 | Negative bipolar receive input from the analog line interface. Data and clock are recovered from the signal applied to this pin and RTIP4, then output on RPOS4, RNEG4 and RCLK4. |
| DPM1 | OUTPUT | 133 | Driver perfomance monitor output for line interface driver 1. If no valid AMI signal is present on MTIP1 and MRING1 for 64 ± 2 clock cycles, DPM1 will go HIGH. The output is cleared when a valid AMI signal is present. |
| DPM2 | OUTPUT | 126 | Driver perfomance monitor output for line interface driver 2. If no valid AMI signal is present on MTIP2 and MRING2 for 64 ± 2 clock cycles, DPM2 will go HIGH. The output is cleared when a valid AMI signal is present. |
| DPM3 | OUTPUT | 40 | Driver perfomance monitor output for line interface driver 3. If no valid AMI signal is present on MTIP3 and MRING3 for 64 ± 2 clock cycles, DPM3 will go HIGH. The output is cleared when a valid AMI signal is present. |
| DPM4 | OUTPUT | 45 | Driver perfomance monitor output for line interface driver 4. If no valid AMI signal is present on MTIP4 and MRING4 for 64 ± 2 clock cycles, DPM4 will go HIGH. The output is cleared when a valid AMI signal is present. |
| LOW1 | OUTPUT | 132 | This output is driven HIGH when the slicing threshold of the input differential signal received on RTIP1/RRING1 is less than 740 mV. |
| LOW2 | OUTPUT | 123 | This output is driven HIGH when the slicing threshold of the input differential signal received on RTIP2/RRING2 is less than 740 mV. |
| LOW3 | OUTPUT | 41 | This output is driven HIGH when the slicing threshold of the input differential signal received on RTIP3/RRING3 is less than 740 mV. |

## PIN DESCRIPTION (Cont.)

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| LOW4 | OUTPUT | 46 | This output is driven HIGH when the slicing threshold of the input differential signal received on RTIP4/RRING4 is less than 740 mV. |
| LEN01 | INPUT | 109 | The logic level applied to this pin in conjunction with the LEN11 and LEN21 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP1 and TRING1.[1] |
| LEN11 | INPUT | 110 | The logic level applied to this pin in conjunction with the LEN01 and LEN21 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP1 and TRING1.[1] |
| LEN21 | INPUT | 111 | The logic level applied to this pin in conjunction with the LEN01 and LEN11 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP1 and TRING1.[1] |
| LEN02 | INPUT | 112 | The logic level applied to this pin in conjunction with the LEN12 and LEN22 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP2 and TRING2.[1] |
| LEN12 | INPUT | 113 | The logic level applied to this pin in conjunction with the LEN02 and LEN22 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP2 and TRING2.[1] |
| LEN22 | INPUT | 114 | The logic level applied to this pin in conjunction with the LEN02 and LEN12 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP2 and TRING2.[1] |
| LEN03 | INPUT | 67 | The logic level applied to this pin in conjunction with the LEN13 and LEN23 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP3 and TRING3.[1] |
| LEN13 | INPUT | 36 | The logic level applied to this pin in conjunction with the LEN03 and LEN23 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP3 and TRING3.[1] |
| LEN23 | INPUT | 35 | The logic level applied to this pin in conjunction with the LEN03 and LEN13 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP3 and TRING3.[1] |
| LEN04 | INPUT | 72 | The logic level applied to this pin in conjunction with the LEN14 and LEN24 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP4 and TRING4.[1] |
| LEN14 | INPUT | 71 | The logic level applied to this pin in conjunction with the LEN04 and LEN24 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP4 and TRING4.[1] |
| LEN24 | INPUT | 70 | The logic level applied to this pin in conjunction with the LEN04 and LEN14 inputs determines the shape and amplitude of the AMI output transmit pulses on TTIP4 and TRING4.[1] |
| TOE1 | INPUT | 108 | This pin controls the tri-stating™ of the TTIP1 and TRING1 outputs. When TOE1 is driven HIGH, TTIP1 and TRING1 go to a high impedance state. |
| TOE2 | INPUT | 99 | This pin controls the tri-stating of the TTIP2 and TRING2 outputs. When TOE2 is driven HIGH, TTIP2 and TRING2 go to a high impedance state. |
| TOE3 | INPUT | 73 | This pin controls the tri-stating of the TTIP4 and TRING4 outputs. When TOE3 is driven HIGH, TTIP4 and TRING4 go to a high impedance state. |
| TOE4 | INPUT | 82 | This pin controls the tri-stating of the TTIP3 and TRING3 outputs. When TOE4 is driven HIGH, TTIP3 and TRING3 go to a high impedance state. |

**Note**:
1. See Table 3 on page 11.

## PIN DESCRIPTION (Cont.)

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| RSEL1 | INPUT | 125 | This pin is used in conjunction with RSEL0 to multiplex out the digital signal recovered from RTIPx and RRINGx onto the monitor outputs RBUFP and RBUFN. The selection of the channel which is monitored depends on the value of RSEL[1:0]. |
| RSEL0 | INPUT | 124 | This pin is used in conjunction with RSEL1 to multiplex out the digital signal recovered from RTIPx and RRINGx onto the monitor outputs RBUFP and RBUFN. The selection of the channel which is monitored depends on the value of RSEL[1:0]. |
| RBUFP | OUTPUT | 117 | This output is used to monitor the AMI signal which is received on RTIPx where the particular RTIP output to be monitored is selected wih RSEL[1:0]. The signal output on this pin is a digital signal slicing of the AMI pulse and is the width of the AMI pulse at the slicing threshold. |
| RBUFN | OUTPUT | 115 | This output is used to monitor the AMI signal which is received on RRINGx where the particular RRING output to be monitored is selected wih RSEL[1:0]. The signal output on this pin is a digital signal slicing of the AMI pulse and is the width of the AMI pulse at the slicing threshold. |
| ROEBUF | INPUT | 116 | This pin controls the tri-stating of the RBUFP and RBUFN outputs. When ROEBUF is driven HIGH, RBUFP and RBUFN will go to a high impedance state. |
| TSEL1 | INPUT | 47 | This pin is used in conjunction with TSEL0 to multiplex the digital P and N transmit data onto the monitor outputs TBUFP and TBUFN. The selection of the channel which is monitored depends on the value of TSEL[1:0]. |
| TSEL0 | INPUT | 48 | This pin is used in conjunction with TSEL1 to multiplex the digital P and N transmit data onto the monitor outputs TBUFP and TBUFN. The selection of the channel which is monitored depends on the value of TSEL[1:0]. |
| TBUFP | OUTPUT | 122 | This output is used to monitor the AMI signal which is transmitted on TTIPx where the particular TTIP output to be monitored is selected wih TSEL[1:0]. The signal output on this pin is a digital signal slicing of the AMI pulse and is the width of the AMI pulse at the slicing threshold. |
| TBUFN | OUTPUT | 120 | This output is used to monitor the AMI signal which is transmitted on TRINGx where the particular TRING output to be monitored is selected wih TSEL[1:0]. The signal output on this pin is a digital signal slicing of the AMI pulse and is the width of the AMI pulse at the slicing threshold. |
| TOEBUF | INPUT | 121 | This pin controls the tri-stating of the TBUFP and TBUFN outputs. When TOEBUF is driven HIGH, TBUFP and TBUFN will go to a high impedance state. |
| N/C | | 77 87 94 | These pins serve no functional purpose, but for improved noise performance reasons each N/C pin should be tied to the VDD pin right beside it. |
| VDDC | POWER | 34 118 137 | Power supply for the digital core logic. |
| VSSC | POWER | 33 119 138 | Ground for the digital core logic. |
| VDDR | POWER | 11 28 49 131 | Power supply for the I/O pad ring. |
| VSSR | POWER | 12 29 50 130 | Ground for the I/O pad ring. |

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## PIN DESCRIPTION (Cont.)

| Pin Name | Pin Type | Pin No. | Description |
|---|---|---|---|
| VDDA | POWER | 68 | Power supply for the analog circuitry (in receiver). |
| VSSA | POWER | 69 | Ground for the analog circuitry (in receiver). |
| VDDCX1 | POWER | 105 | Power supply for analog circuitry in the line driver for channel 1. |
| VDDCX2 | POWER | 93 | Power supply for analog circuitry in the line driver for channel 2. |
| VDDCX3 | POWER | 88 | Power supply for analog circuitry in the line driver for channel 3. |
| VDDCX4 | POWER | 76 | Power supply for analog circuitry in the line driver for channel 4. |
| VSSCX1 | POWER | 106 | Ground for analog circuitry in the line driver for channel 1. |
| VSSCX2 | POWER | 92 | Ground for analog circuitry in the line driver for channel 2. |
| VSSCX3 | POWER | 89 | Ground for analog circuitry in the line driver for channel 3. |
| VSSCX4 | POWER | 75 | Ground for analog circuitry in the line driver for channel 4. |
| VDDRX1 | POWER | 101 | Power supply for pads used by the line driver for channel 1. |
| VDDRX2 | POWER | 97 | Power supply for pads used by the line driver for channel 2. |
| VDDRX3 | POWER | 84 | Power supply for pads used by the line driver for channel 3. |
| VDDRX4 | POWER | 80 | Power supply for pads used by the line driver for channel 4. |
| VSSRX1 | POWER | 102 | Ground for pads used by the line driver for channel 1. |
| VSSRX2 | POWER | 96 | Ground for pads used by the line driver for channel 2. |
| VSSRX3 | POWER | 85 | Ground for pads used by the line driver for channel 3. |
| VSSRX4 | POWER | 79 | Ground for pads used by the line driver for channel 4. |

## FUNCTIONAL DESCRIPTION

### TABLE 1. INTERNAL REGISTERS

| ADDR | 0000 LOOP CTRL (R/W) | 0001 CODE CTRL (R/W) | 0010 INT STAT 1 (RO) | 0011 INT STAT 2 (RO) | 0100 MODE CTRL (R/W) | 0101 LEN1 (R/W) | 0110 LEN 2 (R/W) | 0111 SECURITY (R/W) | 1000 DJAT CTRL (R/W) | 1001 JITDIR (R/W) | 1111 INPUT VOLTAGE (R/W) |
|---|---|---|---|---|---|---|---|---|---|---|---|
| D[7] | RLOOP4 | RCODE4 | LOS4 | DJATOV4 | MODE4 | RLEN2 | RLEN4 | SEC7 | INTEN4 | UNUSED | ASM1 |
| D[6] | RLOOP3 | RCODE3 | LOS3 | DJATOV3 | MODE3 | LEN22 | LEN24 | SEC6 | INTEN3 | UNUSED | ASM0 |
| D[5] | RLOOP2 | RCODE2 | LOS2 | DJATOV2 | MODE2 | LEN12 | LEN14 | SEC5 | INTEN2 | UNUSED | RTSEL |
| D[4] | RLOOP1 | RCODE1 | LOS1 | DJATOV1 | MODE1 | LEN02 | LEN04 | SEC4 | INTEN1 | UNUSED | IMV3 |
| D[3] | LLOOP4 | TCODE4 | DPM4 | AIS4 | TAOS4 | RLEN1 | RLEN3 | SEC3 | RST4 | JITDIR4 | IMV2 |
| D[2] | LLOOP3 | TCODE3 | DPM3 | AIS3 | TAOS3 | LEN21 | LEN23 | SEC2 | RST3 | JITDIR3 | IMV1 |
| D[1] | LLOOP2 | TCODE2 | DPM2 | AIS2 | TAOS2 | LEN11 | LEN13 | SEC1 | RST2 | JITDIR2 | IMV0 |
| D[0] | LLOOP1 | TCODE1 | DPM1 | AIS1 | TAOS1 | LEN01 | LEN03 | SEC0 | RST1 | JITDIR1 | IVOUT |

### DESCRIPTION OF REGISTER FUNCTIONS

#### RLOOP

RLOOP1-4 going HIGH will enable remote loopback on Line Interfaces 1 through 4 respectively. (See Table 1 for register locations.) In remote loopback, the recovered clock and data input on RRTIPx and RRINGx are sent through the jitter attenuator and back out on the line via TTIPx and TRINGx. The recovered signals are also sent to RCLKx, RPOSx, and RNEGx (or RDATAx). A remote loopback bypasses the line code encoder/decoder, ensuring the transmitted signal matches the received signal.

#### LLOOP

LLOOP1-4 going HIGH will enable local loopback on Line Interfaces 1 through 4 respectively. (See Table 1 above for register locations.) During local loopback TCLKx, TPOSx, and TNEGx (or TDATAx) is output on RCLKx, RPOSx, and RNEGx (or RDATAx). Also during local loopback, receiver inputs are ignored, the jitter attenuator is bypassed, and loss of signal response is overridden.

#### Line Code Encoder/Decoder

In Extended Hardware Mode (MODEx=1), AMI, B8ZS and HDB3 codes are available. Data is input to the encoder through TDATAx. The outputs from the decoder are RDATAx and BPVx. The encoder and decoder are selected using LEN2x, LEN1x, LEN0x, TCODEx, and RCODEx as shown in Table 2 below.

#### Loss of Signal

The receiver reports loss of signal by setting the LOS1-4 bits to a one. When LOS is detected on any of the four line interfaces, the INTN output will go LOW. After the interrupt, the LOSx bits can be read to determine which line interface experienced the LOS. (See Table 1 above.) A loss of signal is indicated after 176 consecutive zeros have been received on RTIP/RRING, therefore meeting ITU Draft Rec G.775.

A LOS condition is cleared upon the receipt of a signal having at least 12.5% ones density measured over 32 bits at the RTIPx/RRINGx inputs. A logic one will remain in the LOSx bits until cleared by a read and absence of the LOS condition.

#### Driver Performance Monitor

The Driver Performance Monitor consists of a receiver that monitors a transmitted AMI signal on input pins MTIP and MRING. If no valid AMI signal is present on MTIPx and MRINGx for 64 ± 2 clock cycles, the corresponding DPMx bit is set HIGH. The DPMx bits can be read after an interrupt to determine which transmitter failed. (See Table 1 above.) After a valid AMI signal is present and the register is read, the bits are cleared. Otherwise, the DPMx bit will remain set to a one.

### TABLE 2. SELECTION OF ENCODER/DECODER

|  | LEN2x/1x/0x | |
|---|---|---|
|  | 000 | 010-111 |
| TCODEx = 0 | HDB3 encoder | B8ZS encoder |
| TCODEx = 1 | AMI encoder | AMI encoder |
| RCODEx = 0 | HDB3 decoder | B8ZS decoder |
| RCODEx = 1 | AMI decoder | AMI decoder |

## Digital Jitter Attenuator

The DJATOV bits are set to a one when an overflow or an underflow has occurred in the digital FIFO. The bits are cleared by resetting the affected DJAT.

## Transmit All-Ones Select

When TAOSx bits are set HIGH, transmit all-ones is selected and continuous ones are transmitted on TTIPx and TRINGx. (See Table 1, page 10.) The TPOSx and TNEGx (or TDATAx) inputs are ignored. The combination of TAOS with any loopback mode is illegal; the resulting operation is undefined. The jitter attenuator of LIUx is disabled when TAOSx is HIGH, thereby conserving power. The all-ones insertion is at the frequency of LIU1. Any LIU with TAOSx HIGH will be clocked at the same frequency as LIU1.

## Alarm Indication Signal

The AISx bits are set HIGH when less than three zeros are detected out of 2048 bit periods. When AISx is HIGH,

the INTN output will go LOW. After four or more zeros out of 2048 bits and the INT STAT2 register is read, the AISx bits will be cleared.
(See Table 1, page 10.)

## Hardware Mode and Extended Hardware Mode

The MODEx bits determine if the individual line interface unit is in Hardware Mode or in Extended Hardware Mode. (See Table 1, page 10.) In the Hardware Mode (MODEx bits=0), data is input on TPOS and TNEG, and output on RPOS, and RNEG. In Extended Hardware Mode (MODEx bits=1), data is input on TDATA and output on RDATA. In Extended Hardware Mode, BPV is available for detecting bipolar violations. B8ZS or HDB3 encoding and decoding is also available. (See Table 2 on page 10.)

## Line Length Selection on External Pin or Register

The RLENx bit selects whether the line lengths are selectable by external pins

or by internal register. When the RLENx bit is zero, the length is selectable from external pins. Wnen the RLENx bit is one, the line length is selectable via internal registers.

## Line Length Selection

Line length selection is available on pins and registers. The pins can be grounded and the registers used to select the line length. On power up, the registers are cleared and the external pins can be used to select the line length. (See registers in Table 1 on page 10, and line length codes in Table 3 below.)

## Jitter Attenuator Direction Select

The direction of the jitter attenuator in each LIU can be set via this register or via the JITDIR[4:1] pins. When a logic one is written to JITDIRx, the jitter attenuator for LIUx is put on the receive path, otherwise, it is on the transmit path. The JITDIRx bit is OR'd with the JITDIRx pin.

## TABLE 3. LINE LENGTH SECTION

| LEN2x | LEN1x | LEN0x | Option |
|-------|-------|-------|--------|
| 0 | 0 | 0 | PCM-30 G.703 |
| 0 | 0 | 1 | FCC Part 68, Option A |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | ANSI T1.403 and DSX-1  0-133 feet |
| 1 | 0 | 0 | 133-266 feet |
| 1 | 0 | 1 | 266-399 feet |
| 1 | 1 | 0 | 399-533 feet |
| 1 | 1 | 1 | 533-655 feet |

## Transmitters

T1 (DSX-1) or PCM-30 G.703 pulse shapes may be selected. Pulse shaping and signal level are determined by "line length select" inputs on page 11. The VNS14Q575 line driver is designed to drive a 75-ohm equivalent load.

For T1 DSX-1 applications, line lengths from 0 to 655 feet (distance between the transmitter and the DSX-1 cross connect) are selectable. A typical output pulse is shown in the adjacent diagram. These pulse settings can also be used to meet CCITT pulse shape requirements for 1.544-MHz operation.

The E1 G.703 pulse shape is supported with line length selection input pins or bits LEN2x/1x/0x = 000. The pulse width will meet the G.703 pulse shape template (shown in the adjacent graph and specified in Table 4 on page 13).

## Security Register

To protect the integrity of data being processed, registers that affect the data path are protected against accidental changes by a security register. Writing to registers that do not affect the data integrity (Input Voltage Monitor Register and the Security Register) are not affected by this feature, nor is reading any register. To write to a protected register, its address is first written into SEC7-0. Writing is then enabled to that address. If a write is attempted to any other protected register, the write will not occur. Once any write is attempted, writing is disabled until another write to SEC7-0. Since all register addresses are in the range 0 to 15, SEC7-4 must always be written with zeros.

## Reset Bits

The RSTx bits will reset the jitter attenuator centering the FIFO read and write pointers. When a logic one is written to the RSTx bit, the rising edge of the bit causes a pulse to be generated which resets the jitter attenuator. The bit is not autocleared and so must be cleared by the μP before being set again.

## Interrupt Enable

INTENx will enable the interrupt to the INTN pin when the FIFO overflows or underflows. Interrupts due to LOS, AIS, or DPM are not maskable.

## TYPICAL PULSE SHAPE AT DSX-1 CROSS CONNECT
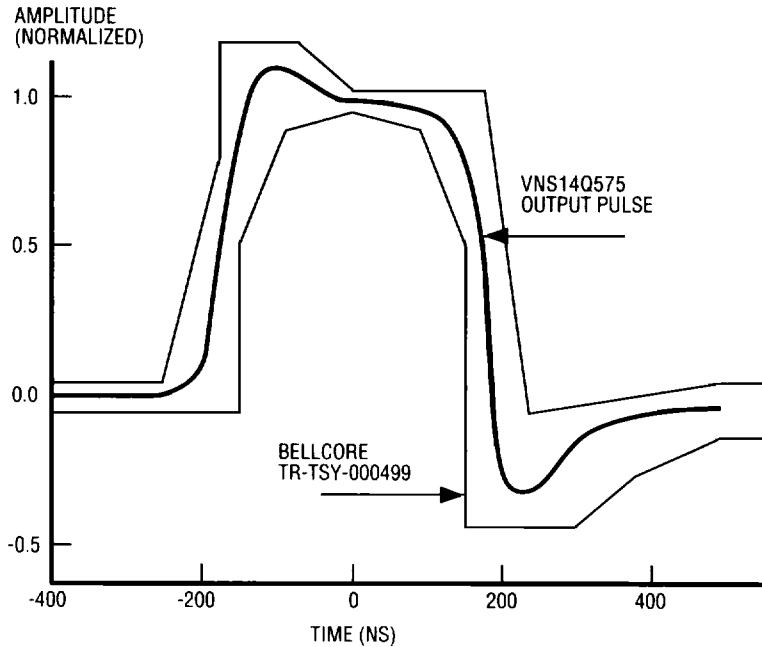


## MASK OF THE PULSE AT THE 2.048 MB/s
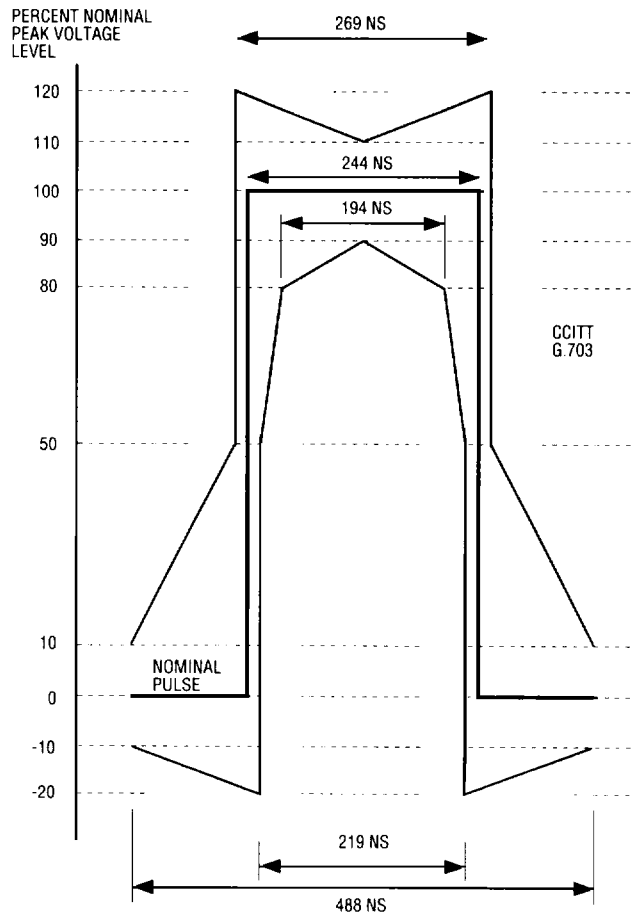
## TABLE 4. CCITT PULSE SPECIFICATIONS

| | Coaxial Cable 75 Ω Load | Shielded Twisted Pair 120 Ω Load |
|---|---|---|
| Nominal peak voltage of a mark (pulse) | 2.37 V | 3 V |
| Peak voltage of a space (no pulse) | 0 ± 0.237 V | 0 ± 0.3 V |
| Nominal pulse width | 244 ns | |
| Ratio of the amplitudes of positive and negative pulse at the center of the pulse interval | 0.95 to 1.05[1] | |
| Ratio of the widths of positive and negative pulses at the nominal half amplitude | 0.95 to 1.05 | |

### Input Monitor Voltage Select

The IMVx bits will select different internal reference voltages to compare to the receive input voltage peak. (See Table 5.) If the input voltage is above the reference voltage, a one will be written into the IVOUT register. The monitor select bits ASMx and RTSEL select which receiver is being monitored with the digital result bit read from the IVOUT register. (See Table 6.) The register is cleared when it is read or when a different reference voltage is selected.

Since the reference voltage is derived from a resistor divider network between $V_{DD}$ and $V_{SS}$, the voltage monitor circuit is only accurate when $V_{DD}$ = 5.0 V.

### Monitoring Capability

Additional monitor pins have been added to make monitoring directly available at the device pins. (A block diagram of these features is shown on page 15. Also see pin descriptions.)

### LOW1 to LOW4 Signal Pins

LOWx output pins go HIGH when the slicing threshold of the differential signal received on RTIP-RRING is less than 384 mV.

## TABLE 5. INPUT MONITOR VOLTAGES

| IMV3 | IMV2 | IMV1 | IMV0 | Internal Voltage Reference |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | V1 - 0.5 |
| 0 | 0 | 0 | 1 | V2 - 1.71 |
| 0 | 0 | 1 | 0 | V3 - 1.87 |
| 0 | 0 | 1 | 1 | V4 - 2.04 |
| 0 | 1 | 0 | 0 | V5 - 2.23 |
| 0 | 1 | 0 | 1 | V6 - 2.44 |
| 0 | 1 | 1 | 0 | V7 - 2.66 |
| 0 | 1 | 1 | 1 | V8 - 2.91 |
| 1 | 0 | 0 | 0 | V9 - 3.18 |
| 1 | 0 | 0 | 1 | V10 - 3.47 |
| 1 | 0 | 1 | 0 | V11 - 3.79 |
| 1 | 0 | 1 | 1 | V12 - 4.14 |

## TABLE 6. MONITOR RECEIVER SELECT

| RTSEL | ASM1 | ASM0 | IVOUT |
|---|---|---|---|
| 0 | 0 | 0 | Tip receive 1 |
| 0 | 0 | 1 | Tip receive 2 |
| 0 | 1 | 0 | Tip receive 3 |
| 0 | 1 | 1 | Tip receive 4 |
| 1 | 0 | 0 | Ring receive 1 |
| 1 | 0 | 1 | Ring receive 2 |
| 1 | 1 | 0 | Ring receive 3 |
| 1 | 1 | 1 | Ring receive 4 |

## TABLE 7. REGISTER VALUES AFTER RESET

| | | | |
|---|---|---|---|
| RLOOP1-4 | 0h | AIS1-4 | 0h |
| LLOOP1-4 | 0h | MODE1-4 | 0h |
| RCODE1-4 | Fh | LENXX-LENXX | 0h |
| TCODE1-4 | Fh | SEC0-7 | Fh |
| LOS1-4 | 0h | IMV0-3, ASMO-1, RTSEL | 0h |
| DPM1-4 | 0h | TAOS1-4 | 0h |

**Note:**
1. When configured with a 0.47 μF nonpolarized capacitor in series with the Tx transformer primary.

## JITTER AND WANDER ATTENUATION

The jitter attenuator function is to reduce wander and jitter in the transmit clock signal or in the receive clock signal. The specification for the jitter attenuator exceeds AT&T Publication 62411, Bellcore TR499 and ITU G.735 requirements. A typical jitter attenuation curve is shown below.

### TYPICAL JITTER ATTENUATION CURVE

ATTENUATION (dB)

0

10

20

30

40

50

60

62411 SPECIFICATION
(1990 VERSION)

MINIMUM ATTENUATION

MAXIMUM
ATTENUATION

ACTUAL
ATTENUATION

1          10          100          1000          10,000

FREQUENCY (Hz)

### INPUT JITTER TOLERANCE

1000.0

100.0

10.0

1.0

SINE WAVE JITTER AMPLITUDE
PEAK TO PEAK (UI) - LOG SCALE
MEASURED IN A NOISE-FREE ENVIRONMENT

AT&T 62411 SPECIFICATION

138 UI

28 UI

4.9 Hz

0.7 kHz

0.4 kHz

MINIMUM TOLERANCE
LEVEL

MINIMUM LEVEL TO
RESYNCHRONIZE

0.4 UI
0.2 UI

0.1          1.0          10          100          1 K          10 K          100 K

SINE WAVE JITTER FREQUENCY (Hz)

14

## QLIU BLOCK DIAGRAM (Showing Extended Monitor Features)
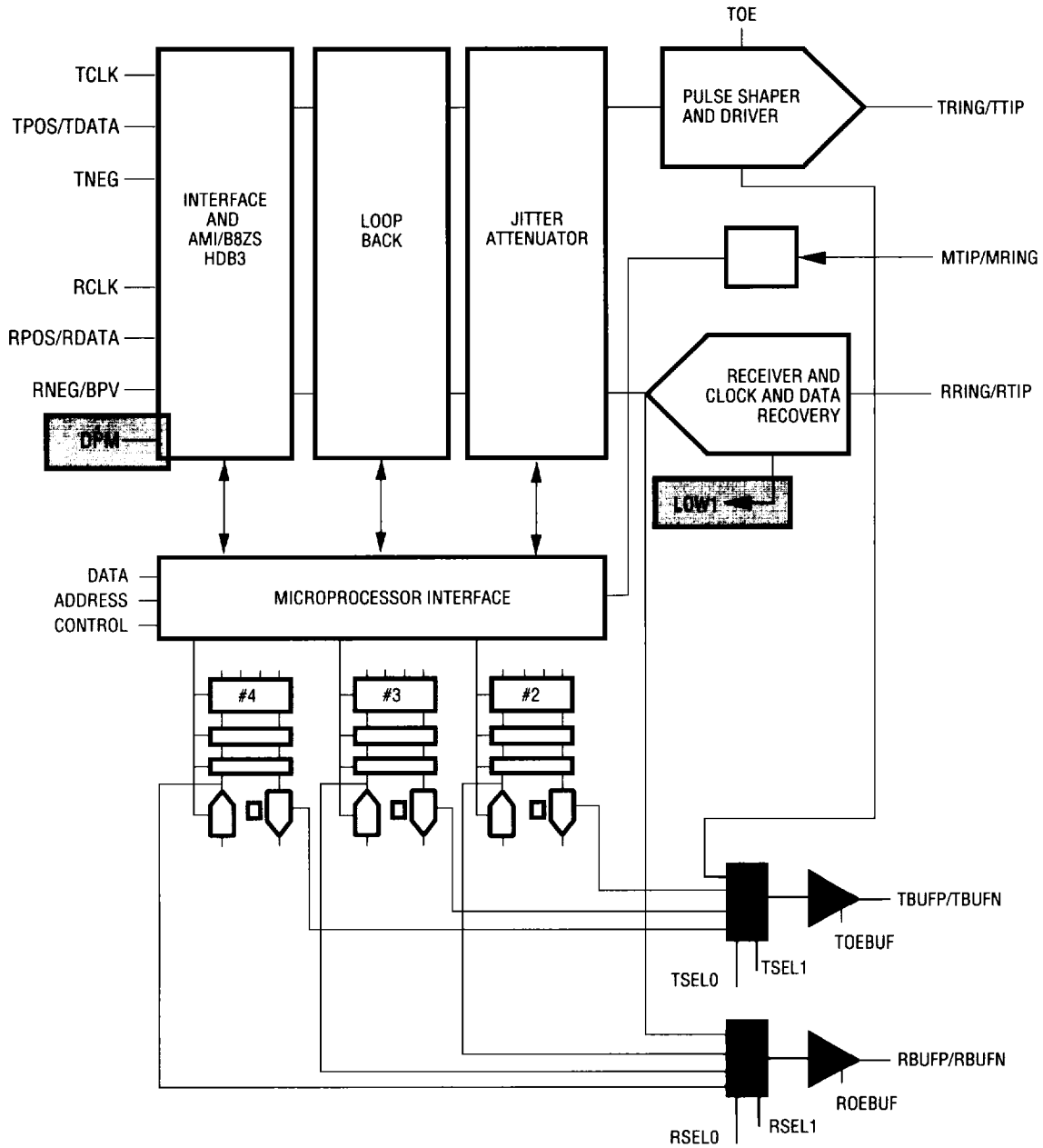
### DPM1 TO DPM4 DRIVER PERFORMANCE MONITOR PINS

The driver performance monitor consists of a receiver that monitors a transmitted AMI signal on input pins MTIP and MRING. If no valid AMI signal is present on MTIPx and MRINGx for 64 ± 2 clock cycles, the corresponding DPMx bit is set HIGH and the corresponding DPMx pin will go HIGH. The bits are cleared on read if a valid AMI signal is present. The DPMx pins will go LOW when a valid AMI signal is present.

### TBUFP, TOEBUF, TSEL1, TSEL0

This extended output is a sample of the TTIP DAC output. The DAC output is sampled by a comparator that slices at greater than 60% of the internal DAC output amplitude for shortest line drive setting. The width of this created digital pulse is the width of TTIP and can be used to evaluate the integrity of TTIP. The digital value for each TTIPx is passed to TBUFP through a mux selected by TSEL1 and TSEL0. TOEBUF HIGH will cause the TBUFP output to be high impedance.

| TSEL1 | TSEL0 | TBUFP |
|-------|-------|--------|
| 0 | 0 | TBUFP1 |
| 0 | 1 | TBUFP2 |
| 1 | 0 | TBUFP3 |
| 1 | 1 | TBUFP4 |

### TBUFN, TOEBUF, TSEL1, TSEL0

This extended output is a sample of the TRING DAC output. The DAC output is sampled by a comparator that slices at greater than 60% of the DAC output amplitude for shortest line drive setting. The width of this created digital pulse is the width of TRING and can be used to evaluate the integrity of TRING. The digital value for each TRINGx is passed to TBUFN through a mux selected by TSEL1 and TSEL0. TOEBUF HIGH will cause the TBUFN output to be high impedance.

| TSEL1 | TSEL0 | TBUFN |
|-------|-------|--------|
| 0 | 0 | TBUFN1 |
| 0 | 1 | TBUFN2 |
| 1 | 0 | TBUFN3 |
| 1 | 1 | TBUFN4 |

### RBUFP, ROEBUF, RSEL1, RSEL0

The RBUFP extended output is a sample of the RTIP input. The received signal is the P representation of the received AMI signal. The digital value for each RTIPx is passed to RBUFP through a mux selected by RSEL1 and RSEL0. ROEBUF HIGH will cause the RBUFP output to be high impedance.

| RSEL1 | RSEL0 | RBUFP |
|-------|-------|--------|
| 0 | 0 | RBUFP1 |
| 0 | 1 | RBUFP2 |
| 1 | 0 | RBUFP3 |
| 1 | 1 | RBUFP4 |

### RBUFN, ROEBUF, RSEL1, RSEL0

The RBUFN extended output is a sample of the RRING input. The received signal is the N representation of the received AMI signal. The digital value for each RRINGx is passed to RBUFN through a mux selected by RSEL1 and RSEL0. ROEBUF HIGH will cause the RBUFN output to be high impedance.

| RSEL1 | RSEL0 | RBUFN |
|-------|-------|--------|
| 0 | 0 | RBUFN1 |
| 0 | 1 | RBUFN2 |
| 1 | 0 | RBUFN3 |
| 1 | 1 | RBUFN4 |

## ELECTRICAL CHARACTERISTICS (TA = -40° to +85° C, V = 5 V ±5%, GND = 0 V)

| Sym | Parameter | Min | Max | Units | Test Conditions |
|-----|-----------|-----|-----|-------|-----------------|
| PD | Total power dissipation[1] | | 1200 | mW | 100% ones density and maximum line length at 5.25 V |
| VIH | High-level input voltage | 2.0 | | V | |
| VIL | Low-level input voltage | | 0.8 | V | |
| VOH | High-level output voltage[2] | 2.4 | | V | IOUT= 400 µA |
| VOL | Low-level output voltage[2] | | 0.4 | V | IOUT=1.6 mA |
| ILL | Input leakage current | 0 | +10 | µA | |
| I3L | Tri-state leakage current | 0 | +10 | µA | |

**Notes:**
1. Power dissipation while driving 75 Ω load over operating temperature range. Includes device and load. Digital input levels are within 10% of the supply rails. Digital outputs are driving a 50 pF capacitive load.
2. Output drivers will output CMOS logic levels into CMOS loads.

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## ANALOG SPECIFICATIONS (TA = -40° to +85° C, V = 5 V ±5%, GND = 0 V)

| Parameter | | Min | Typ | Max | Units | Test Condition |
|---|---|---|---|---|---|---|
| AMI output pulse amplitudes | DSX-1 | 2.4 | 3.0 | 3.6 | V | Measured at the DSX |
| | CEPT | 2.7 | 3.0 | 3.3 | V | Measured at line side |
| Recommended output load at TTIP and TRING | | 75 | | | Ω | |
| Jitter added by the transmitter[1] | 10 Hz - 8 kHz | | | 0.02 | UI | |
| | 8 kHz - 40 kHz | | | 0.025 | UI | |
| | 10 Hz - 40 kHz | | | 0.025 | UI | |
| | Broadband | | | 0.05 | UI | |
| Sensitivity below DSX | (0 dB = 2.4 V) | 12.0 | | | dB | Peak voltage with 772 KHz |
| | | 600 | | | mV | attenuation, QRSS data |
| Loss of signal threshold | | | 0.74 | | V | |
| Data decision threshold | DSX-1 | | 65 | | % peak | |
| | CEPT | | 50 | | % peak | |
| Allowable consecutive zeros before LOS | | | 176 | | | |
| Input jitter tolerance 10 kHz - 100 kHz | | 0.4 | | | UI | |
| Jitter attenuation curve corner frequency[2,3] | | | 4.2 | 6 | Hz | |
| Minimum transmitter return loss[4] | 51 kHz - 102 kHz | 20 | | | dB | |
| | 102 kHz - 2.048 MHz | 19 | | | dB | |
| | 2.048 MHz - 3.072 MHz | 18 | | | dB | |

## MASTER CLOCK AND TRANSMIT TIMING CHARACTERISTICS

| Symbol | Parameter | | Min | Typ[5] | Max | Units |
|---|---|---|---|---|---|---|
| | Master clock frequency (CLKX2N low) | T1 | | 50 ± 25 ppm | | MHz |
| | | E1 | | 50 ± 25 ppm | | MHz |
| | Master clock duty cycle[6] (CLKX2N low) | | 40 | | 60 | % |
| | Master clock frequency (CLKX2N high) | T1 | | 100 ± 25 ppm | | MHz |
| | | E1 | | 100 ± 25 ppm | | MHz |
| | Master clock duty cycle[6] (CLKX2N high) | | 30 | | 70 | % |
| | Transmit clock frequency | T1 | | 1.544 | | MHz |
| | | E1 | | 2.048 | | MHz |
| | Transmit clock tolerance | T1 | | | ±32 | ppm |
| | | E1 | | | ±50 | |
| | Transmit clock duty cycle | | 30 | | 70 | % |
| $t_{SUT}$ | TPOS/TNEG to TCLK set-up time | | 25 | | | ns |
| $t_{HT}$ | TCLK to TPOS/TNEG hold time | | 25 | | | ns |

## TRANSMIT CLOCK TIMING
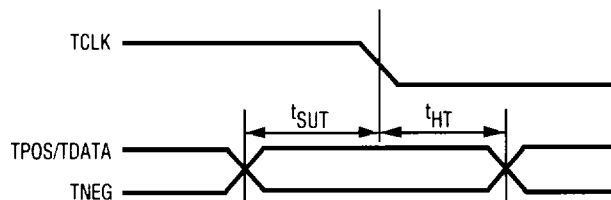


### Notes:
1. Input signal to TCLK is jitter free.
2. Circuit attenuates jitter at 20 dB/decade above the corner frequency.
3. For 62411 mode only.
4. With two 24.9 Ω resistors in series with transmit transformer primary.
5. Typical figures are at +25° C.
6. Measured at 1/2 VDD Level (u.o.m. 2.5 V).

## RECEIVE TIMING CHARACTERISTICS

| Symbol | Parameter | | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| RCLKd | Receive clock duty cycle[2,3] | T1 | 25 | 40 | 65 | % |
| RCLKd | | E1 | 30 | 50 | 50 | % |
| $t_{PW}$ | Receive clock cycle period[2,3,4] | T1 | 400 | 600/650 | 900 | ns |
| $t_{PW}$ | | E1 | 370 | 450/490 | 600 | ns |
| $t_{PWH}$ | Receive clock pulse width HIGH[2,3] | T1 | | 250 | | ns |
| $t_{PWH}$ | | E1 | | 190 | | ns |
| $t_{PWL}$ | Receive clock pulse width LOW[2,3] | T1 | 150 | 400 | 650 | ns |
| $t_{PWL}$ | | E1 | 180 | 300 | 420 | ns |
| $t_{PR}$ | RCLK to RPOS/RNEG delay | T1 | 2 | 5 | 12 | ns |
| $t_{PR}$ | | E1 | 2 | 5 | 12 | ns |

### RECEIVE TIMING

**HARDWARE MODE**
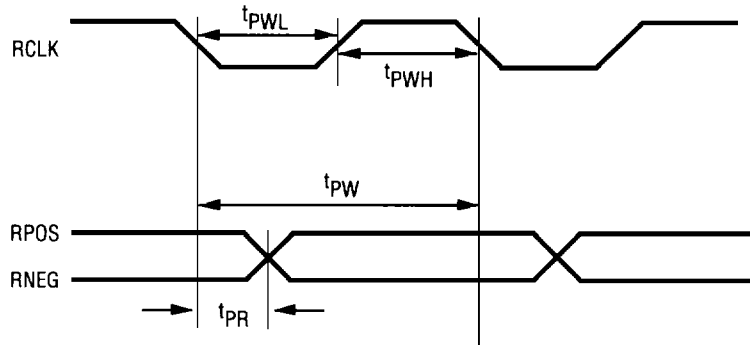


**EXTENDED HARDWARE MODE**
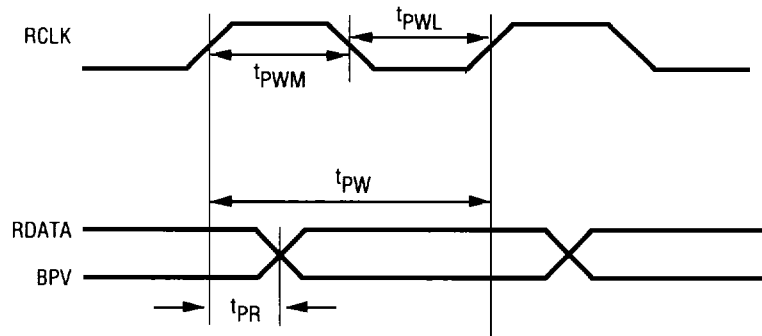


**Notes:**
1. Typical figures are at +25° C and are for design aid only, and not subject to testing.
2. This table assumes that the jitter attenuator is not in the receive data path. If the jitter attenuator is selected to be in the receiver, RCLK has the characteristics provided in the jitter attenuator section (on page 14).
3. RCLK duty cycle widths will vary depending on extent of received pulse jitter displacement. Max and Min RCLK duty cycles are for worst-case jitter conditions (0.4-UI clock displacement for 1.544 MHz, 0.2-UI clock displacement for 2.048 MHz).
4. The width of RCLK varies in steps of 50 ns (30 or 40 ns in E1) and alternates between fast and slow cycles to produce an average pulse width of 648 ns in T1 or 488 ns in E1.

## MICROPROCESSOR INTERFACE TIMING CHARACTERISTICS (TA = -40° to +85° C, VDD = 5 V ±5%)

### MICROPROCESSOR WRITE ACCESS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SAW}$ | Address to valid write set-up time | 25 | | ns |
| $t_{SDW}$ | Data to valid write set-up time | 20 | | ns |
| $t_{HDW}$ | Data to valid write hold time | 20 | | ns |
| $t_{HAW}$ | Address to valid write hold time | 20 | | ns |
| $t_{VWR}$ | Valid write pulse width | 40 | | ns |

### MICROPROCESSOR WRITE TIMING
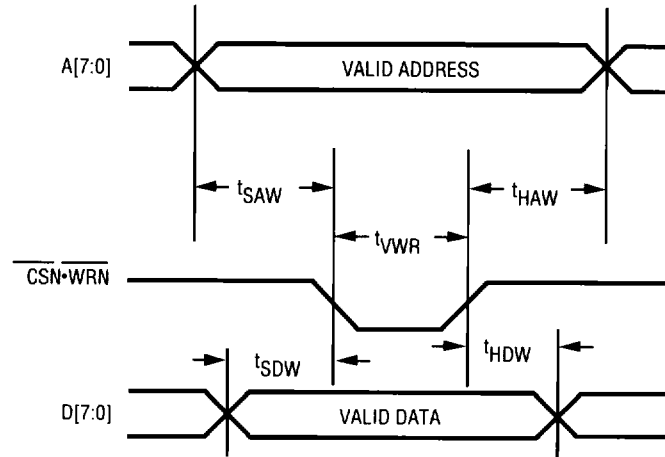


### MICROPROCESSOR READ ACCESS

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SAR}$ | Address to valid read set-up time | 25 | | ns |
| $t_{HAR}$ | Address to valid read hold time | 20 | | ns |
| $t_{PRD}$ | Valid read to valid data propagation delay | | 80 | ns |
| $t_{ZRD}$ | Valid read deasserted to output tri-state | | 30 | ns |
| $t_{PINTH}$ | Valid read deasserted to INT HIGH | | 30 | ns |

### MICROPROCESSOR READ TIMING
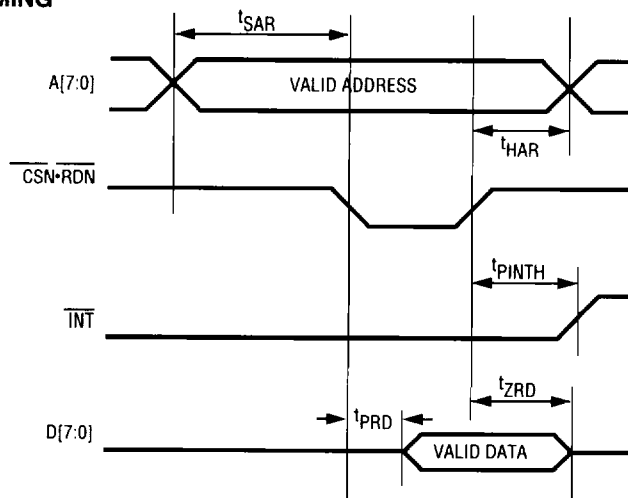
## EXTENDED MONITOR TIME (TA = -40° to +85° C, VDD = 5 V ±5%)

**EXTENDED TIMING**

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{OE}$ | OE low to output active | | 50 | ns |
| $t_{DIS}$ | OE high to output high impedance | | 50 | ns |
| $t_{BUFP}$ | SEL to valid data | | 70 | ns |

**EXTENDED MONITOR TIMING**
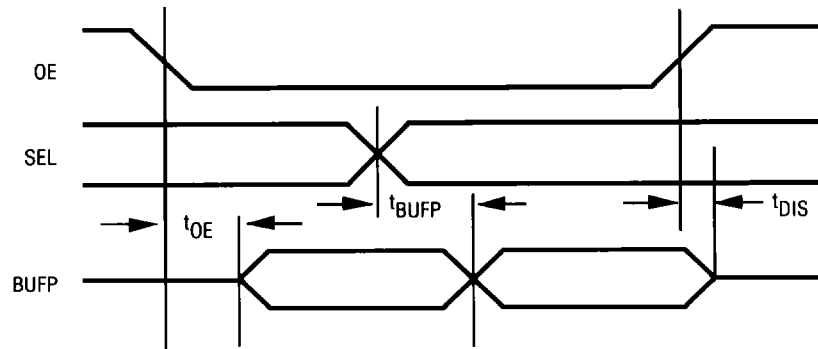
## APPLICATIONS INFORMATION

### LINE INTERFACE CIRCUIT

The recommended line interface circuitry for one channel is shown in the figure below. The TTIP and TRING outputs are coupled to the line through a pulse transformer. This transmit transformer requires different turns ratios depending on the application. The table below summarizes the required turns ratios and a possible part number for each application. The transformers listed are manufactured by Pulse Engineering, Inc. The purpose of resistors R3 and R4 is to increase the transmitter return loss. R3 and R4 are both 24.9 ohm, 1% resistors. R3 and R4 should

not be included for T1 applications. They are only required for E1 operations. Note that a 0.47-µF non-polarized capacitor should be placed in series with the transmit transformer primary to prevent any build up in the core of the transformer due to DC imbalance at the differential outputs of the circuit.

| Application | Turns Ratio | Part No. |
|-------------|-------------|----------|
| T1 | 1:1.15 | PE65388 |
| 75 ohm E1 | 1:1.266 | PE65389 |
| 120 ohm E1 | 1:1.58 | PE64940 |

The RTIP and RRING inputs are coupled to the line via a center-tapped pulse transformer having a turns ratio of 2:1. The center tap is connected to

ground and the resistor pair consisting of R1 and R2 provide the line termination. R1 and R2 are 150 ohms each or 240 ohms each for 75 ohm and 120 ohm E1 respectively. They are 200 ohms each for T1. (All resistor values have tolerance of 1%.) For the receive transformer, the Pulse Engineering PE64931 is the recommended part.

**LINE INTERFACE**
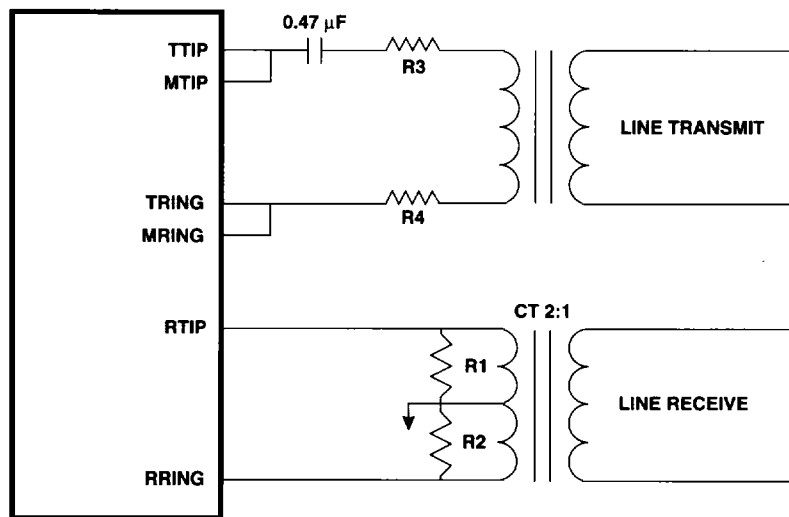
## PACKAGE OUTLINES

### 144-LEAD METRIC QUAD FLAT PACK
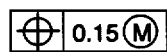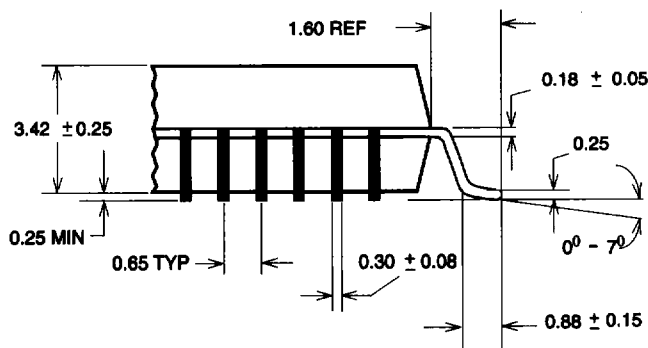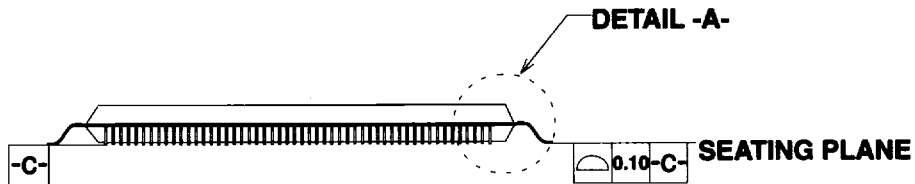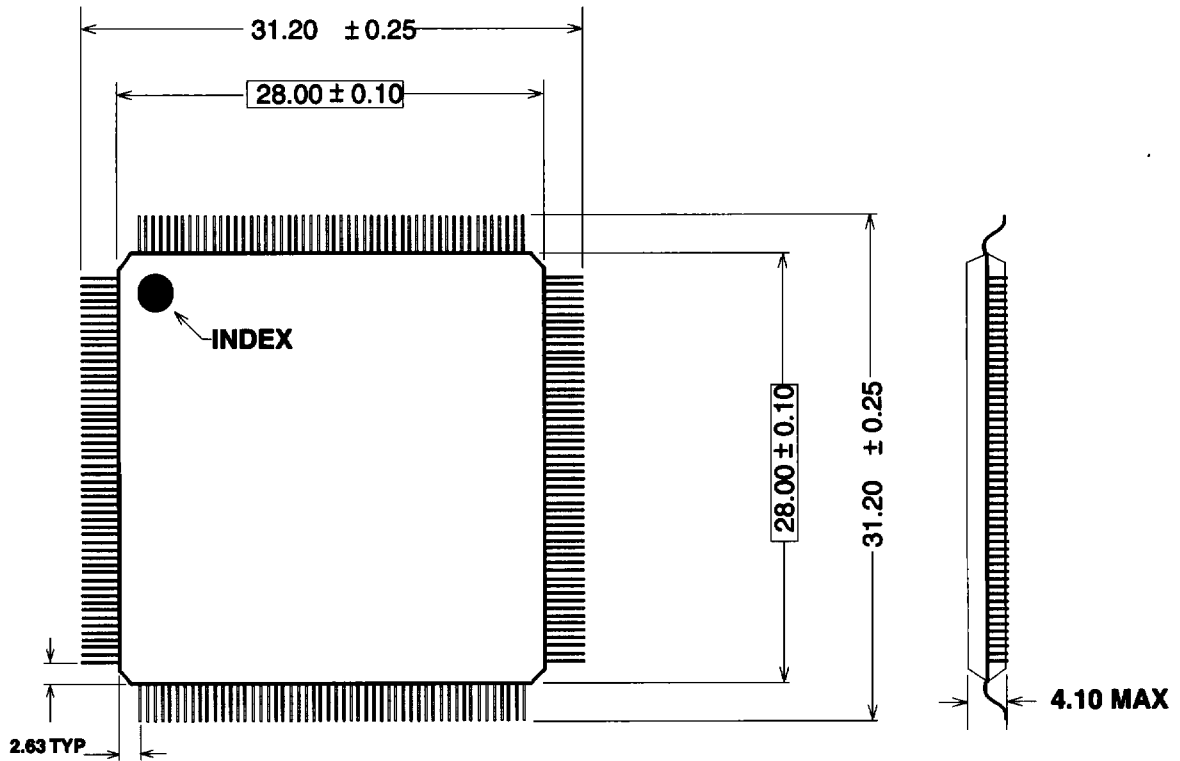


**DETAIL -A-**

# PIN DIAGRAM

## 144-LEAD METRIC QUAD FLAT PACK

Top pins (Pin 144 to Pin 109): tpos[2], tneg[2], tclk[1], tpos[1], tneg[1], rst, Vss, Vdd, rclk[1], rpos[1], rneg[1], dpm[1], los[1], Vdd, Vss, rclk[2], rpos[2], rneg[2], dpm[2], rsel[1], rsel[0], los[2], tbufp, toebuf, tbufn, Vss, Vdd, rbufp, roebuf, rbufn, len[22], len[12], len[02], len[21], len[11], len[01]

Pin 144 / Pin 1

Pin 109 / Pin 108

Left side (Pin 1 to Pin 36):
tclk[2]
int
d[7]
d[6]
d[5]
d[4]
d[3]
d[2]
d[1]
d[0]
Vdd
Vss
xtalin
clkx2N
cs
rd
wr
a[3]
a[2]
a[1]
a[0]
tclk[3]
tpos[3]
tneg[3]
tclk[4]
tpos[4]
tneg[4]
Vdd
Vss
jitmode
frloop
test
Vss
Vdd
len23
len13

Right side (Pin 108 to Pin 73):
t1oe
jatdir[1]
Vss
Vdd
n/c
tring[1]
Vss
Vdd
ttip[1]
t2oe
ttip[2]
Vdd
Vss
tring[2]
n/c
Vdd
Vss
jatdir[2]
jatdir[3]
Vss
Vdd
n/c
tring[3]
Vss
Vdd
ttip[3]
t3oe
ttip[4]
Vdd
Vss
tring[4]
n/c
Vdd
Vss
jatdir[4]
t4oe

Pin 36 / Pin 37

Pin 73 / Pin 72

Bottom pins (Pin 37 to Pin 72): rclk[3], rpos[3], rneg[3], dpm[3], los[3], rclk[4], rpos[4], rneg[4], dpm[4], tsel[1], tsel[0], Vdd, Vss, rtip[1], rring[1], rring[2], rtip[2], rtip[3], rring[3], rring[4], rtip[4], mring[1], mtip[1], mring[2], mtip[2], mring[3], mtip[3], mring[4], mtip[4], len[03], Vdd, Vss, len[24], len[14], len[04]

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