

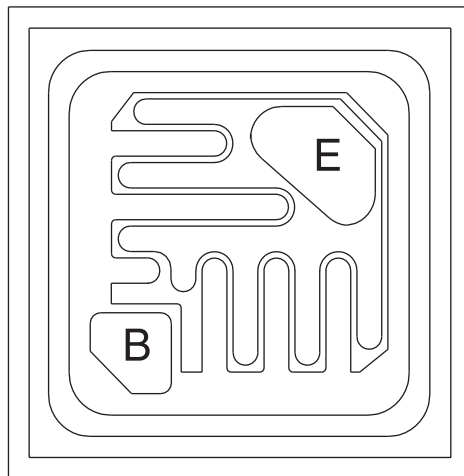
**PROCESS CP716V**  
**Small Signal Transistors**  
PNP - High Voltage Transistor Chip



**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	19.7 x 19.7 MILS
Die Thickness	7.1 MILS
Base Bonding Pad Area	4.0 x 4.0 MILS
Emitter Bonding Pad Area	4.7 x 4.7 MILS
Top Side Metalization	Al - 30,000Å
Back Side Metalization	Au - 18,000Å

**GEOMETRY**



BACKSIDE COLLECTOR R0

**GROSS DIE PER 4 INCH WAFER**

29,659

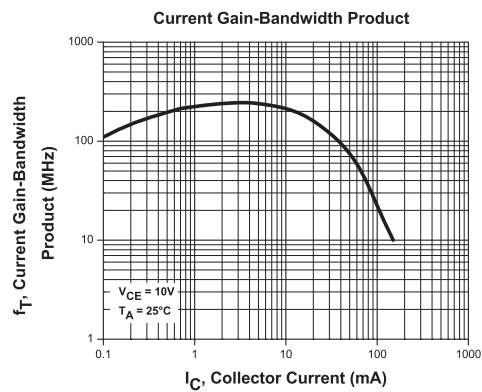
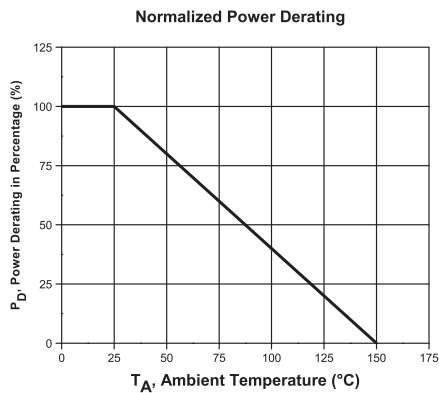
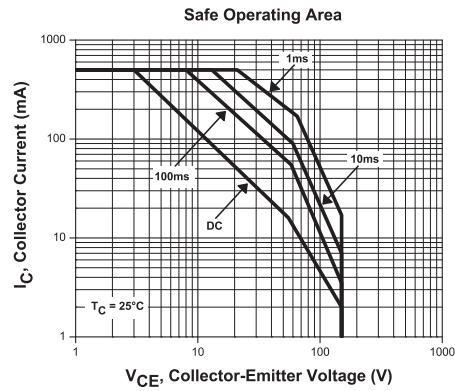
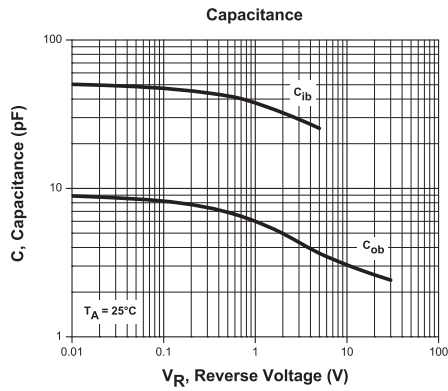
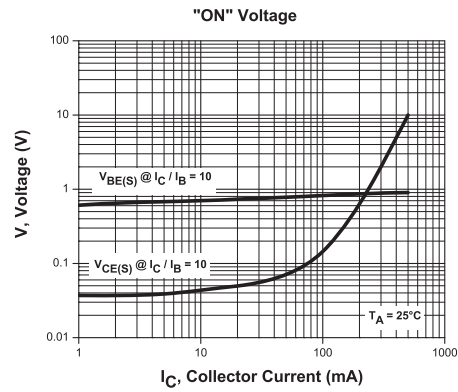
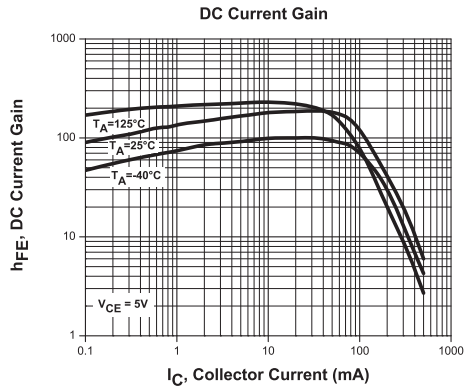
**PRINCIPAL DEVICE TYPES**

CMUT5401  
CMPT5401  
CXT5401

R2 (22-March 2010)

# PROCESS CP716V

## Typical Electrical Characteristics



R2 (22-March 2010)