18-Bit 3.3V Registered Buffer

ICS162834

Recommended Applications:

- PC133 Registered Memory Module
- PC motherboards
- Servers and workstations
- Provides complete PC133 DIMM solution with ICSVF2509, ICSVF2510 PLL.

Product Features:

- Meets JESD 82-2 specification
- Internal series resistors to reduce switching noise
- ±12 mA device capability
- Low voltage operation
  - V_{DD} = 3.3 ± 0.3V
- 0.50 mm pitch, 56-Pin TSSOP package

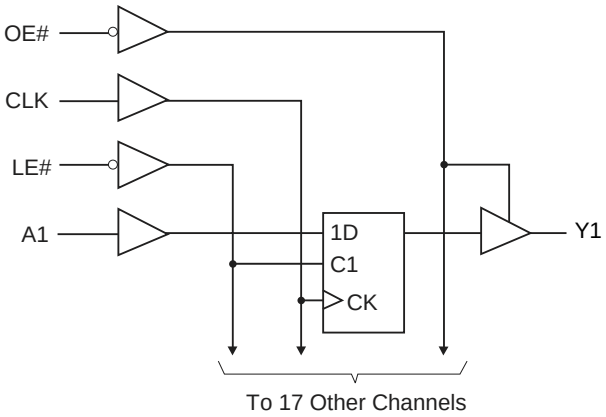
Function Table[1]

Inputs				Outputs
OE#	LE#	CLK	Ax	Yx
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y_0(2)
L	H	L	X	Y_0(3)

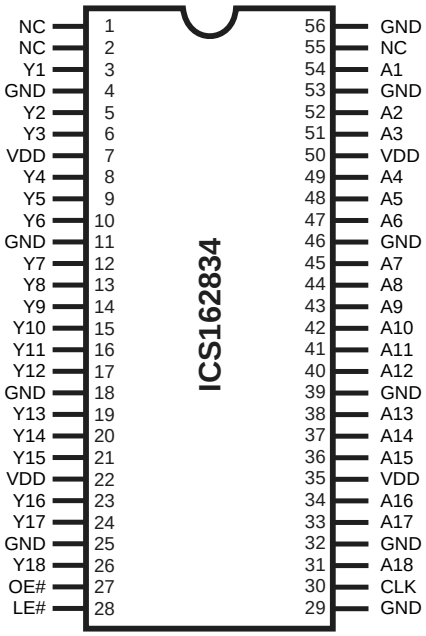
Notes:

1. H = HIGH Voltage Level
   L = LOW Voltage Level
   X = Don't Care
   Z = High-Impedance
   ↑ = LOW-to-HIGH Transition
2. Output level before the indicated steady-state input conditions were established, provided that CLK is HIGH before LE# went LOW.
3. Output level before the indicated steady-state input conditions were established.

Block Diagram



Pin Configurations



56-Pin TSSOP

6.10 mm. Body, 0.50 mm. pitch

Pin Description

Pin Names	Description
OE#	Output Enable Input (Active Low)
CLK	Clock Input
LE#	Latch Enable Input
Ax	Data Input
Yx	Data Outputs
V_{DD}	Supply Voltage
GND	Ground

General Description

The ICS162834 low voltage 18-bit register combines D-type latches and D-type flip-flops to allow data flow in transparent, latched and clocked modes. Date flow is controlled by output-enable (OE#), latch enable (LE#), and clock (CLK) inputs. The device operates in transparent mode when LE# is held low. The device operates in clocked mode when LE# is high and CLK is toggled. Data transfers from the inputs (A[18:1]) to outputs (Y[18:1]) on a positive edge transition of the clock. When OE# is low, the output state is enabled. When OE# is high, the output port is in a high impedance state.

The 18-bit registered buffer is designed to operate with a 3.0V to 4.6V supply voltage.

All inputs support operation with standard LVTTL interface levels. This includes data inputs, clock inputs and control inputs. Device outputs meet the requirements of the PC133 Registered DIMM specification. The device functions as defined supports latched, registered and flow through modes of operations. The PC133 Specification requires only registered mode.

Package is a 56 thin shrink small-outline package as defined by JEDEC Publication, JEP95, MO-153.

Absolute Maximum Ratings

Storage Temperature . . . . . –65°C to + 150°C
Supply Voltage (V_{DD}) . . . . . -0.5 to 4.6V
Input Voltage (V_I) . . . . . -0.5 to 4.6V
Output Voltage (V_O) . . . . . -0.5 to V_{DDQ} + 0.5
Input Clamp Current (I_{IK}) . . . . . 50 mA
Output Clamp Current (I_{OK}) . . . . . ±50 mA
Continuous Output Current (I_O) . . . . . ±50 mA
V_{DD}, V_{DDQ} or GND Current/Pin . . . . . ±100 mA
Package Thermal Impedance, O_{JA} . . . . . 64°C/W

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	TYP	MAX
V_{DD}	Supply Voltage		3.0	3.3	3.6
V_{IN}	Voltage Applied to input pins		-0.3		3.6
V_{OUT}	Voltage Applied to output or I/O pins	Outputs enabled	0		V_{DD}
		Outputs high-Z	0		V_{DD}
T_A	Operating free-air temperature		0		70

Switching Characteristics

Symbol	Parameter	V_{CC} = 3.3V ± 0.15V		UNITS
		MIN	MAX	
t_{PLH}, t_{PHL}	Propagation Delay CLK to Yx	1.8	3.5	ns
$t_{SK(0)}$	Output Skew*	-	500	ps
f_{CLOCK}		150	-	MHz

* Skew between any two putputs of the same package and switching in the same direction

Electrical Characteristics - DC

T_A = 0 - 70° C; V_{DD} = 3.3 ± 0.3V, V_{DDQ}=3.3 ± 0.3V; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS	V_{DD} (V)	MIN	TYP	MAX	UNITS
V_{IH}	HIGH-level input voltage		3.0 - 3.6	2.0			V
V_{IL}	LOW-level input voltage		3.0 - 3.6			0.8	V
V_{OH}	HIGH-level output voltage	I_{OH} = -12 mA, V_{IH} = 2.0V	3.0	2.2			V
V_{OL}	Low-level output voltage	I_{OL} = 12 mA, V_{IL} = 0.8V	3.0			0.8	
I_I	Input leakage current	V_I = V_{DD} or GND	3.0 - 3.6			±10	µA
I_{OZ}	Off-state leakage current	V_O = V_{DD} or GND#, OE = V_{DD}				±20	µA
I_{DD}	Quiescent Supply Current	V_I = V_{DD} or GND, I_O = 0				±40	µA

* Parameters are characterized over recommended operating conditions.

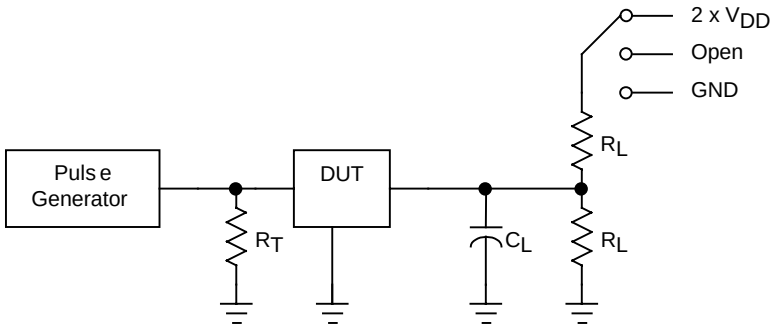
Critical Register Specifications*

SYMBOL	PARAMETERS	CONDITION	V_{DD} (V)	MIN	TYP	MAX	UNITS
t_{PD}**	Propagation Delay (CK to Y)	R_L = 500 Ω, C_L = 50 pF	3.0 - 3.6	1.4		3.5	ns
t_{PD}**	Propagation Delay (CK to Y)	R_L = 500 Ω, C_L = 30 pF	3.0 - 3.6	0.7		2.5	ns
t_S	Setup time (A before CK)		3.0 - 3.6	1.0			ns
t_H	Hold time (A after CK)		3.0 - 3.6	0.6			ns
C_I	Clock input capacitance		3.0 - 3.6	3.3	4.0	6.0	pF

* Parameters are characterized over recommended operating conditions.

** The t_{PD} value in this table would equate to the 'Time-to-Vm' delay described in the post register timing specifications of the PC133 registered DIMM Specification. The first value applies to DIMMs with nine SDRAM loads per register output, and the second to DIMMs with eighteen SDRAM loads per register output. These values should serve as only an initial starting point,

Test Circuit and Switching Waveforms

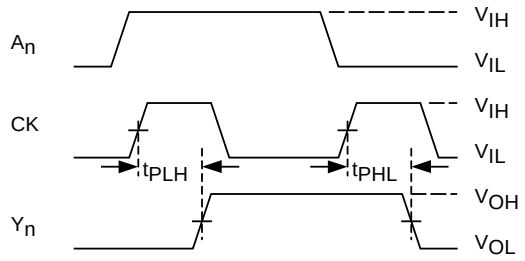


Test Circuit

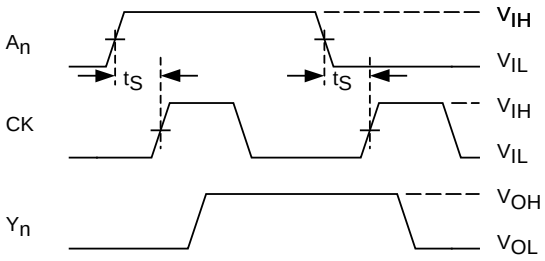
Test circuit component values:
R_L = Load Resistor = 500 Ω
C_L = Load Capacitance and includes probe and jig capacitance
R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generator
V_{IN} = 0 to V_{DD}
$t_r = t_f$ 2.0 ns (10% to 90%) unless otherwise specified.

Parameter Tested	Switch Position
t_{PLH}	Open
t_{PHL}	Open
t_{PZH}	GND
t_{PZL}	2 x V_{DD}
t_{PHZ}	GND
t_{PLZ}	2 x V_{DD}

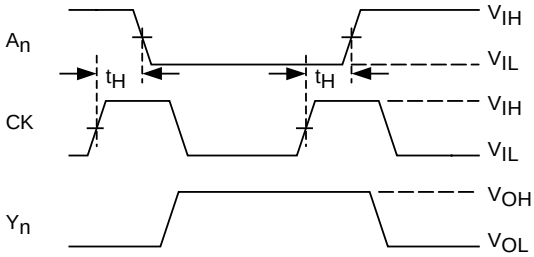
PROPAGATION DELAY MEASUREMENT



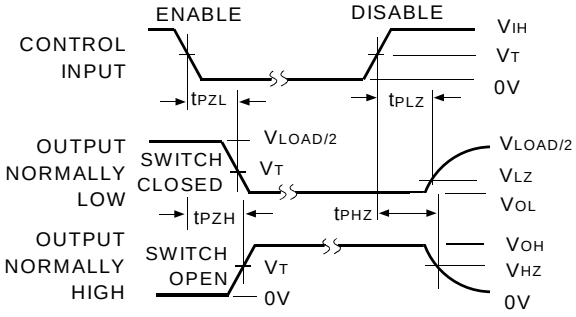
SETUP TIME MEASUREMENTS



HOLD TIME MEASUREMENTS

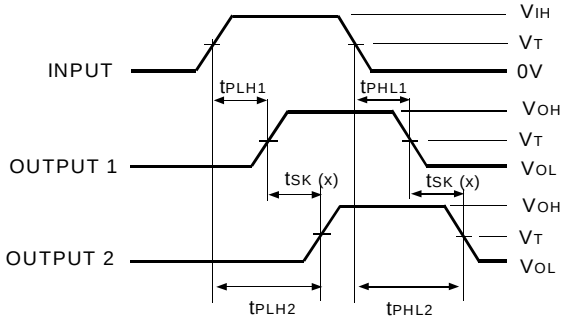


ENABLE AND DISABLE TIMES



NOTE:
1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH.

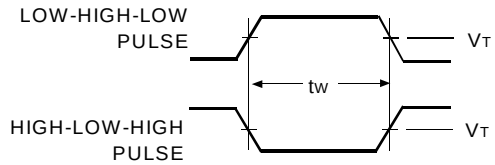
OUTPUT SKEW - $t_{SK(X)}$



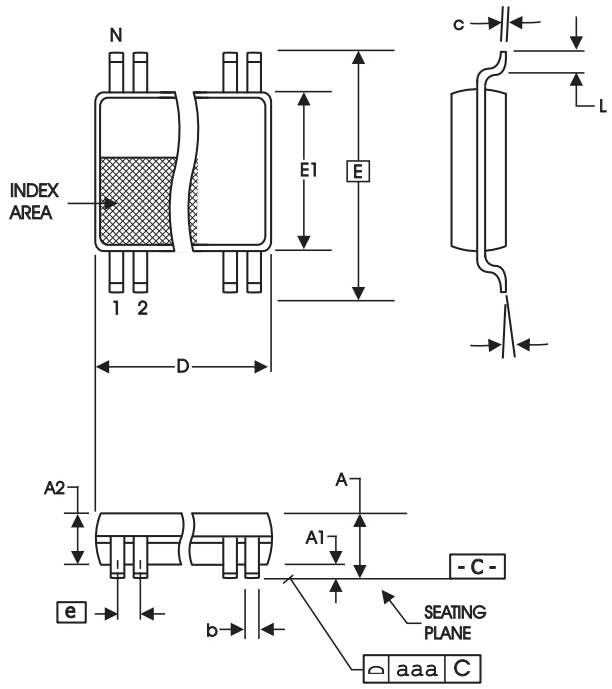
$t_{SK(x)} = |t_{PLH2} - t_{PLH1}|$ or $|t_{PHL2} - t_{PHL1}|$

NOTES:
1. For t_{SK}(o) OUTPUT1 and OUTPUT2 are any two outputs.
2. For t_{SK}(b) OUTPUT1 and OUTPUT2 are in the same bank.

PULSE WIDTH



Switching Waveforms



6.10 mm. Body, 0.50 mm. pitch TSSOP
(240 mil) (0.020 mil)

SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	--	1.20	--	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.032	.041
b	0.17	0.27	.007	.011
c	0.09	0.20	.0035	.008
D	SEE VARIATIONS		SEE VARIATIONS	
E	8.10 BASIC		0.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		0.020 BASIC	
L	0.45	0.75	.018	.030
N	SEE VARIATIONS		SEE VARIATIONS	
α	0°	8°	0°	8°
aaa	--	0.10	--	.004

'ARIATIONS

N	D mm.		D (inch)	
	MIN	MAX	MIN	MAX
56	13.90	14.10	.547	.555

Reference Doc.: JEDEC Publication 95, MO-153

10-0039

Ordering Information

ICS162834AG-T

Example:

ICS XXXX y **G - PPP - T**

- **T** — **Designation for tape and reel packaging**
- **PPP** — **Pattern Number (2 or 3 digit number for parts with ROM code patterns)**
- **G** — **Package Type**
  G = TSSOP
- y — **Revision Designator** (will not correlate with datasheet revision)
- **XXXX** — **Device Type (consists of 3 or 4 digit numbers)**
- **ICS** — **Prefix**
  ICS, AV = Standard Device

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