LOW SKEW, 1-4 LVCMOS/LVTTL-TO-LVDS FANOUT BUFFER
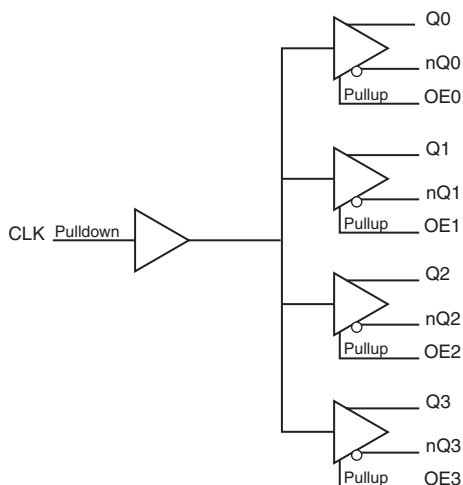
ICS854105

GENERAL DESCRIPTION

The ICS854105 is a low skew, high performance 1-to-4 LVCMOS/LVTTL-to-LVDS Clock Fanout Buffer and a member of the HiPerClockS™ family of High Performance Clock Solutions from IDT. Utilizing Low Voltage Differential Signaling (LVDS), the ICS854105 provides a low power, low noise, solution for distributing clock signals over controlled impedances of 100Ω. The ICS854105 accepts an LVCMOS/LVTTL input level and translates it to LVDS output levels.

Guaranteed output and part-to-part skew characteristics make the ICS854105 ideal for those applications demanding well defined performance and repeatability.

FEATURES

- Four LVDS outputs

- One single-ended LVCMOS/LVTTL clock input

- CLK can accept the following input levels: LVCMOS, LVTTL

- Maximum output frequency: 250MHz

- Translates single-ended input signals to LVDS levels

- Additive phase jitter, RMS: 0.15ps (typical)

- Output skew: TBD

- Part-to-part skew: TBD

- Propagation delay: 1.3ns (typical)

- 3.3V operating supply

- 0°C to 70°C ambient operating temperature

- Industrial temperature information available upon request

- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

BLOCK DIAGRAM

PIN ASSIGNMENT

ICS854105
16-Lead TSSOP
4.4mm x 5.0mm x 0.92mm package body
G Package
Top View

TABLE 1. PIN DESCRIPTIONS

Number	Name	Type		Description
1	OE0	Input	Pullup	Output enable pin for Q0, nQ0 output. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
2	OE1	Input	Pullup	Output enable pin for Q1, nQ1 outputs. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
3	OE2	Input	Pullup	Output enable pin for Q2, nQ2 outputs. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
4	V_{DD}	Power		Positive supply pin.
5	GND	Power		Power supply ground.
6	CLK	Input	Pulldown	Single-ended clock input. LVCMOS/LVTTL interface levels.
7	nc	Unused		No connect.
8	OE3	Input	Pullup	Output enable pin for Q3, nQ3 outputs. If OE pin is LOW, outputs will drive HiZ. LVCMOS/LVTTL interface levels.
9, 10	nQ3, Q3	Output		Differential output pair. LVDS interface levels.
11, 12	nQ2, Q2	Output		Differential output pair. LVDS interface levels.
13, 14	nQ1, Q1	Output		Differential output pair. LVDS interface levels.
15, 16	nQ0, Q0	Output		Differential output pair. LVDS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 2. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ

TABLE 3. OE[3:0] FUNCTION TABLE

Inputs	Outputs
OE[3:0]	Q0/nQ0:Q3/nQ3
0	HiZ (default)
1	Active

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{DD}	4.6V
Inputs, V_I	-0.5V to V_{DD} + 0.5V
Outputs, I_O	
Continuous Current	10mA
Surge Current	15mA
Package Thermal Impedance, θ_{JA}	93.3°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 4A. POWER SUPPLY DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Positive Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			60		mA

TABLE 4B. LVCMOS / LVTTL DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	CLK	$V_{DD} = V_{IN} = 3.465V$			150	µA
		OE[0:3]	$V_{DD} = V_{IN} = 3.465V$			5	µA
I_{IL}	Input Low Current	CLK	$V_{DD} = 3.465V, V_{IN} = 0V$	-5			µA
		OE[0:3]	$V_{DD} = 3.465V, V_{IN} = 0V$	-150			µA

NOTE: Outputs terminated with 50Ω to V_{DD}/2. See Parameter Measurement Information, "Output Load Test Circuit".

TABLE 4C. LVDS DC CHARACTERISTICS, V_{DD} = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OD}	Differential Output Voltage			350		mV
ΔV_{OD}	V_{OD} Magnitude Change			30		mV
V_{OS}	Offset Voltage			1.3		V
ΔV_{OS}	V_{OS} Magnitude Change			20		mV

TABLE **5. AC C**HARACTERISTICS, V_{DD} = 3.3V±5%, T$_A$ = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
f_{MAX}	Output Frequency				250	MHz
t_{PD}	Propagation Delay; NOTE 1			1.3		ns
$t$jit	Buffer Additive Phase Jitter, RMS; refer to Additive Phase Jitter Section	(12kHz to 20MHz)		0.15		ps
$t$sk(o)	Output Skew; NOTE 2, 4			TBD		ps
$t$sk(pp)	Part-to-Part Skew; NOTE 3, 4			TBD		ps
t_R / t_F	Output Rise/Fall Time	20% to 80%		400		ps
odc	Output Duty Cycle			50		%

All parameters measured at f_{MAX} unless noted otherwise.
NOTE 1: Measured from the V_{DD}/2 of the input to the differential output crossing point.
NOTE 2: Defined as skew between outputs at the same supply voltage and with equal load conditions.
Measured at V_{DD}/2 of the input to the differential output crossing point.
NOTE 3: Defined as skew between outputs on different devices operating at the same supply voltages
and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at
the differential cross points.
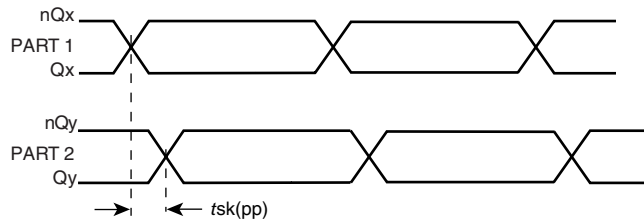NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

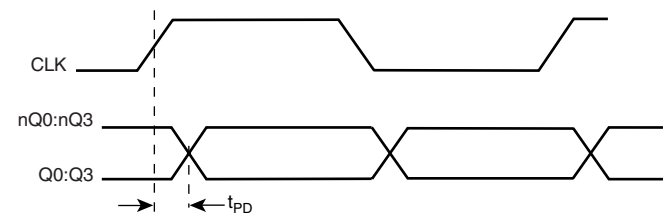# PARAMETER MEASUREMENT INFORMATION
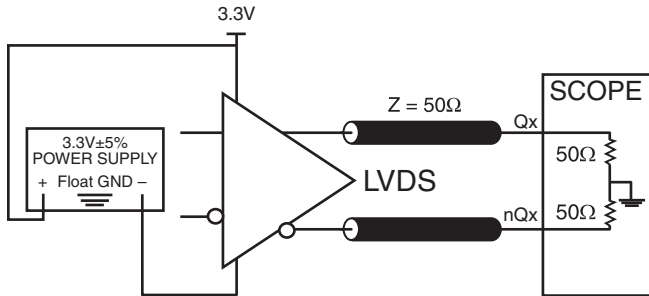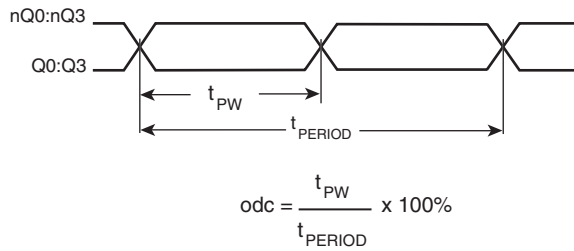

3.3V OUTPUT LOAD AC TEST CIRCUIT
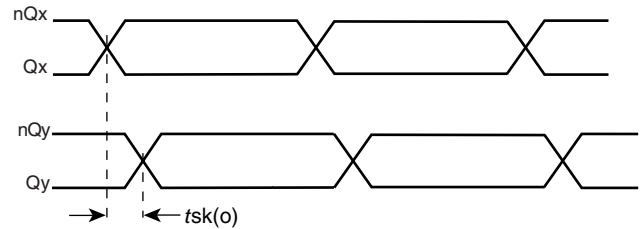
OUTPUT SKEW

PART-TO-PART SKEW

PROPAGATION DELAY

$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

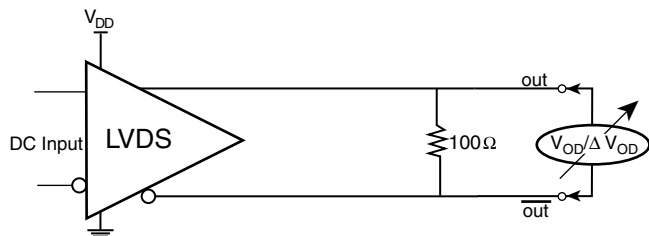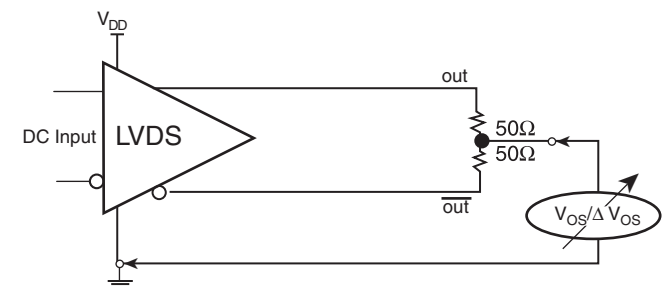**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**
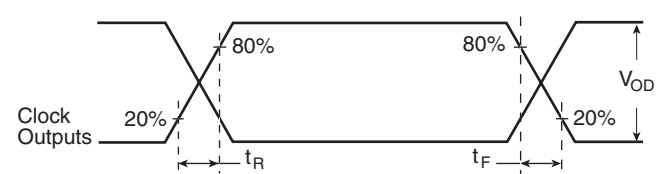
OUTPUT RISE/FALL TIME

DIFFERENTIAL OUTPUT VOLTAGE

OFFSET VOLTAGE

APPLICATION INFORMATION

RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS
INPUTS:
LVCMOS CONTROL PINS:
All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

OUTPUTS:
LVDS
All unused LVDS output pairs can be either left floating or terminated with 100Ω across. If they are left floating, there should be no trace attached.

3.3V LVDS DRIVER TERMINATION

A general LVDS interface is shown in *Figure 1.* In a 100Ω differential transmission line environment, LVDS drivers require a matched load termination of 100Ω across near the receiver input. For a multiple LVDS outputs buffer, if only partial outputs are used, it is recommended to terminate the unused outputs.
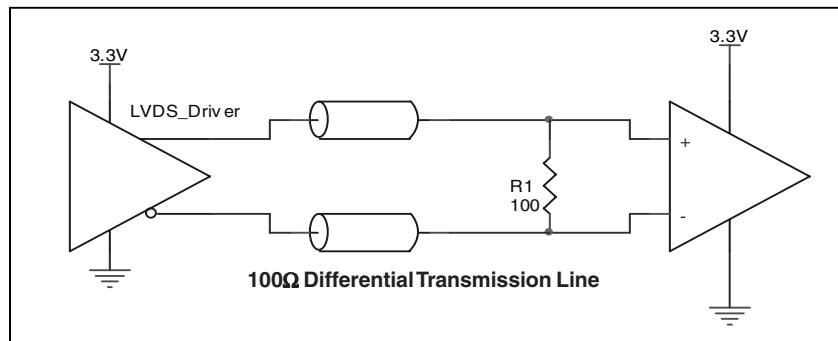

FIGURE 1. TYPICAL LVDS DRIVER TERMINATION

POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS854105.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS854105 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

- Power$_{\_MAX}$ = V_{DD_MAX} * I_{DD_MAX} = 3.465V * 60mA = **207.9mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 88.9°C/W per Table 6 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:
70°C + 0.208W * 88.9°C/W = 88.5°C. This is well below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

TABLE 6. THERMAL RESISTANCE θ_{JA} FOR 16-PIN TSSOP, FORCED CONVECTION

θ_{JA} vs. 0 Air Flow (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	93.3°C/W	88.9°C/W	86.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

RELIABILITY INFORMATION

TABLE 7. θ_{JA} VS. AIR FLOW TABLE FOR 16 LEAD TSSOP

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Multi-Layer PCB, JEDEC Standard Test Boards	93.3°C/W	88.9°C/W	86.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

TRANSISTOR COUNT
The transistor count for ICS854105 is: 286

Pin compatible with SN65LVDS105

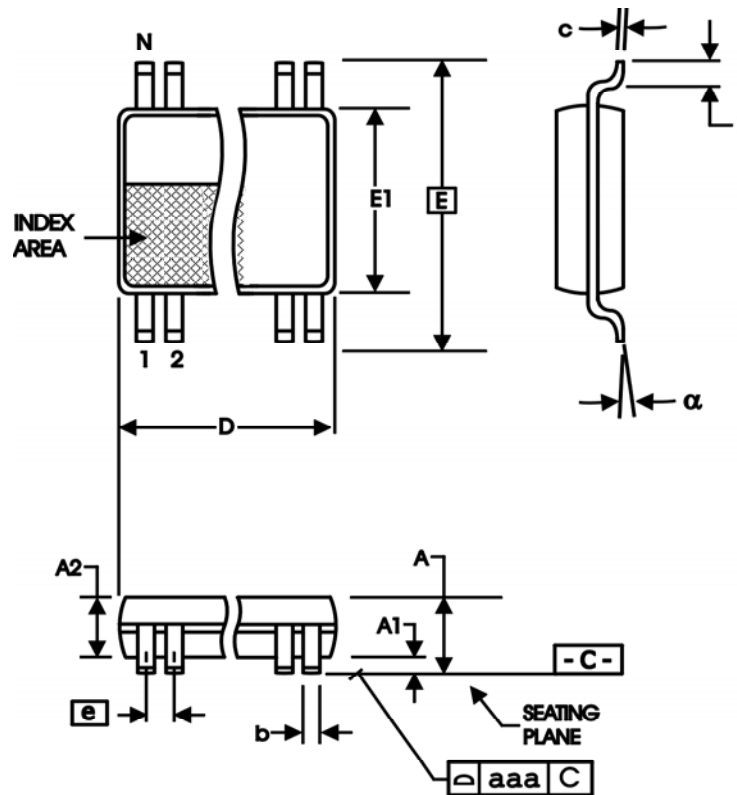**PACKAGE OUTLINE - G SUFFIX FOR 16 LEAD TSSOP**

TABLE 8. PACKAGE DIMENSIONS

SYMBOL	Millimeters	
	Minimum	Maximum
N	16	
A	--	1.20
A1	0.05	0.15
A2	0.80	1.05
b	0.19	0.30
c	0.09	0.20
D	4.90	5.10
E	6.40 BASIC	
E1	4.30	4.50
e	0.65 BASIC	
L	0.45	0.75
α	0°	8°
aaa	--	0.10

Reference Document: JEDEC Publication 95, MO-153

TABLE 9. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
ICS854105AG	854105AG	16 Lead TSSOP	tube	0°C to 70°C
ICS854105AGT	854105AG	16 Lead TSSOP	2500 tape & reel	0°C to 70°C
ICS854105AGLF	TBD	16 Lead TSSOP	tube	0°C to 70°C
ICS854105AGLFT	TBD	16 Lead TSSOP	2500 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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