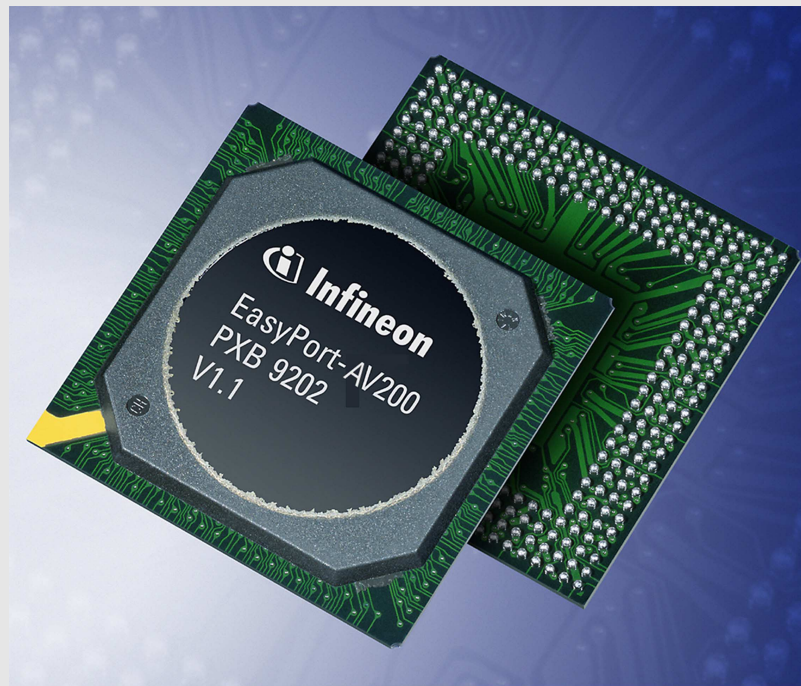


Infineon's EasyPort™ is a comprehensive broadband communication processor family. Based on a powerful 64-bit MIPS CPU core sub-system, the EasyPort™ features packet and ATM cell processing functionality for data and voice/data Integrated Access Devices (IADs), small and medium enterprise gateways, access routers, and Voice over IP (VoIP) gateways. The EasyPort™ family supports T1/E1 framers, standard xDSL transceivers, and 10BaseS™ Ethernet over VDSL technology. EasyPort™ has the compute power and architecture to support firewalls and Virtual Private Networks (VPN), as well as future applications and new connectivity options such as Wireless LANs and Bluetooth™.

When used in combination with VINETIC™, Infineon's system solution supports VoATM and VoIP on the same hardware platform, and supports up to 32 compressed voice channels.

Using the EasyPort™ processor family, communication system vendors gain a powerful set of tools enabling the transportation of data, video and voice services integrated on the same hardware and software platform.



# EasyPort™

## Packet Processing

- Embedded RISC coprocessor
- Embedded data memory
- Two 10/100 Mbit/s Ethernet MAC controllers, one integrated Ethernet PHY
- USB 1.1 device controller
- AAL5 (SAR) controller
- DMA controller with a linked list descriptor buffer

## Voice Data Processing

- Embedded RISC coprocessor
- Two IOM-2/PCM interfaces
- 32 HDLC hardware accelerators
- AAL2 (CPS) controller
- Simple control of DuSLIC, SICOFI and FALC® devices via a Synchronous Serial Interface (SSC)

## ATM Cell Processing

- ATM Layer controller
- UTOPIA Level 1 and 2
- Support for up to 128 VCCs
- Traffic classes: CBR, VBR, UBR+, GFR, UBR
- Cell Buffer Manager with integrated DMA controller for up to 255 user cell queues
- Queue specific traffic shaper in hardware
- Cell filtering (2 filters; maskable VPI/VCI)
- EPD, PPD congestion control
- OAM according to ITU-T I.610

## Embedded Processor Subsystem

- 200 MHz MIPS CPU core including MMU with 32 dual entry TLB

- External Bus Unit (50 MHz, 16-bit) for accessing system memory (SRAM, Flash memory) and external peripherals
- Independent SDRAM I/F (100 MHz, 32-bit, 256 MBytes)

## Security Features

- Security (VPN) and VoIP support
- DES/3DES encryption/decryption hardware accelerator
- Throughput optimized dataflow for VPN/IPsec processing
- QoS optimized VoIP voice data flow

## Others

- Power management
- Lifeline service support

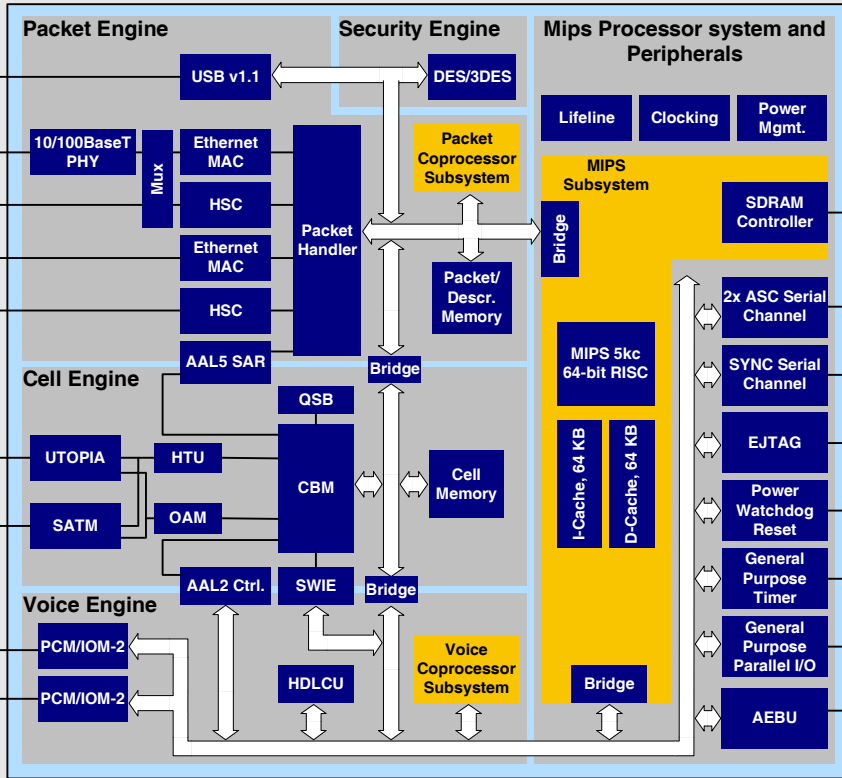
# EasyPort™

Multi-Service Access Processor Family

PXB 9101/9102/9201/9202

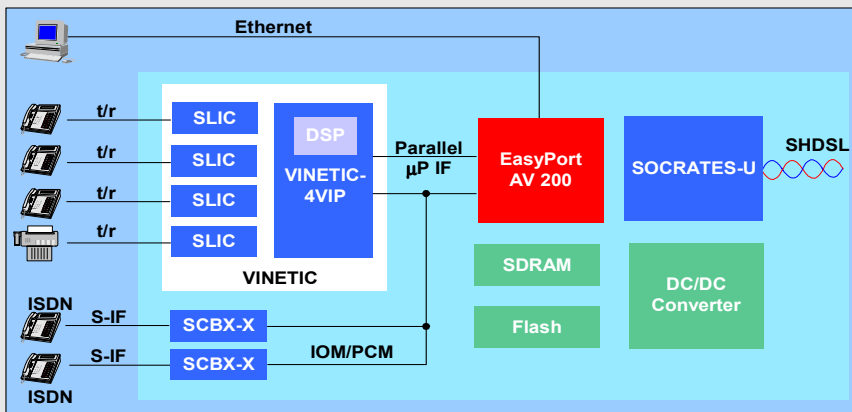


## EasyPort Block Diagram



### Ordering Information

| Product Name   | Sales Code | Ordering Code | Target Application    | CPU Clock | WAN I/F  | Voice Support |          | Security Support |               |
|----------------|------------|---------------|-----------------------|-----------|----------|---------------|----------|------------------|---------------|
|                |            |               |                       |           |          | VoATM         | VoIP     | HW               | Target Mbit/s |
| EasyPort-AV200 | PXB 9202   | Q67233-H1608  | ATM Data/<br>Voice    | 200 MHz   | UTOPIA   | up to 32      |          | DES/3DES         | 5             |
| EasyPort-AS200 | PXB 9102   | Q67233-H1609  | ATM Data/<br>Security | 200 MHz   | UTOPIA   | -             | up to 2  | 3DES, CoP-S      | 10            |
| EasyPort-ES200 | PXB 9101   | Q67233-H1611  | IP Data/<br>Security  | 200 MHz   | Ethernet | -             | up to 2  | 3DES, CoP-S      | 15            |
| EasyPort-EV200 | PXB 9201   | Q67233-H1610  | IP Data/VoIP          | 200 MHz   | Ethernet | -             | up to 32 | DES/3DES         | 5             |



## EasyPort Application Example

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