MOSEL-VITELIC ***V104J8/9***
(256K x 8, 256K x 9) CMOS
MEMORY MODULE

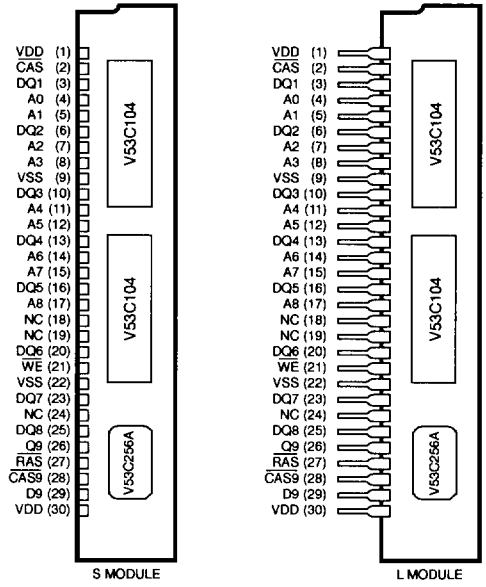
Features

- 262,144 x 8 (or x 9) bit organization
- Utilizes 256K x 4 and 256K x 1 CMOS DRAMs
- Fast Page mode operation
- Fast access times 70 ns, 80 ns and 100 ns
- Low power dissipation
- Common $\overline{CAS}$ control for eight common Data-in and Data-out lines
- Separate $\overline{CAS}$ control for one separate pair of Data-in and Data-out (x 9 organization)
- Single 5 V ±10% supply
- All I/O are fully TTL compatible
- Standard 30-lead single-in-line module

Description

The V104J8/9 Memory Module is organized as 262,144 x 8 (or 9) bits in a 30-lead single-in-line module. The 256K x 8 memory module uses two Vitelic 256K x 4 DRAMs. The 256K x 9 memory module uses two Vitelic 256K x 4 DRAMs and one Vitelic 256K x 1 DRAM. Decoupling capacitors, mounted beneath each package, are surface mounted on the epoxy substrate board. The onboard capacitors eliminate the need for bypassing on the mother board and offer superior performance due to reduced lead inductance.

V104J
Pin Configuration
x 9 Organization

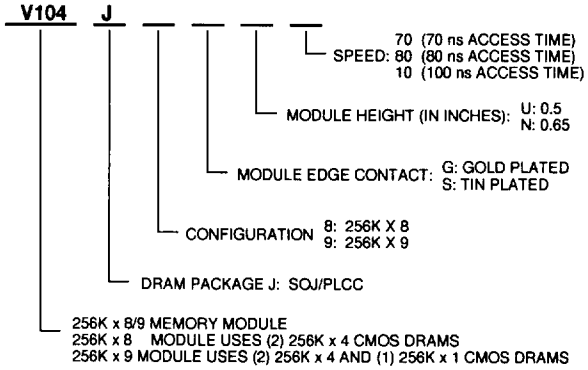


NOTE: ***x 8 Organization***
Pins 26, 28, 29 are not connected

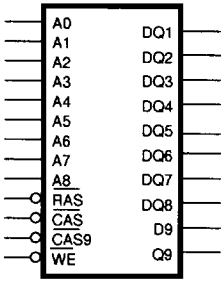
Device Usage Chart

Operating Temperature Range	Bit Organization		Module Type		Access Time (ns)			Power	
	x 8	x 9	S	L	70	80	100	Std	Low
0°C–70°C	•	•	•	•	•	•	•	•	•

Part Number Information



Logic Symbol x 9 Organization



x 8 Organization

$\overline{CAS9}$, D9, Q9 are not connected

Pin Names (x 9 Organization)

Name	Description
A0–A8	Address Inputs
$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$, $\overline{CAS9}$	Column Address Strobes
$\overline{WE}$	Write Enable
DQ1–DQ8	Data In/Data Out
D9	Data In
Q9	Data Out
V_{DD}	5 V Supply
V_{SS}	Ground
NC	No Connection

x 8 Organization

$\overline{CAS9}$, D9, Q9 are not connected

Absolute Maximum Ratings*

Ambient Temperature
Under Bias .....–10°C to +80°C
Storage Temperature (plastic) ....–55°C to +125°C
Voltage on any Pin Except V_{DD}
Relative to V_{SS} .....–1.0 to +7.0 V
Voltage on V_{DD} relative to V_{SS} .....–1.0 to +7.0 V
Data Out Current .....50 mA
Power Dissipation .....3.0 W

*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

Capacitance*

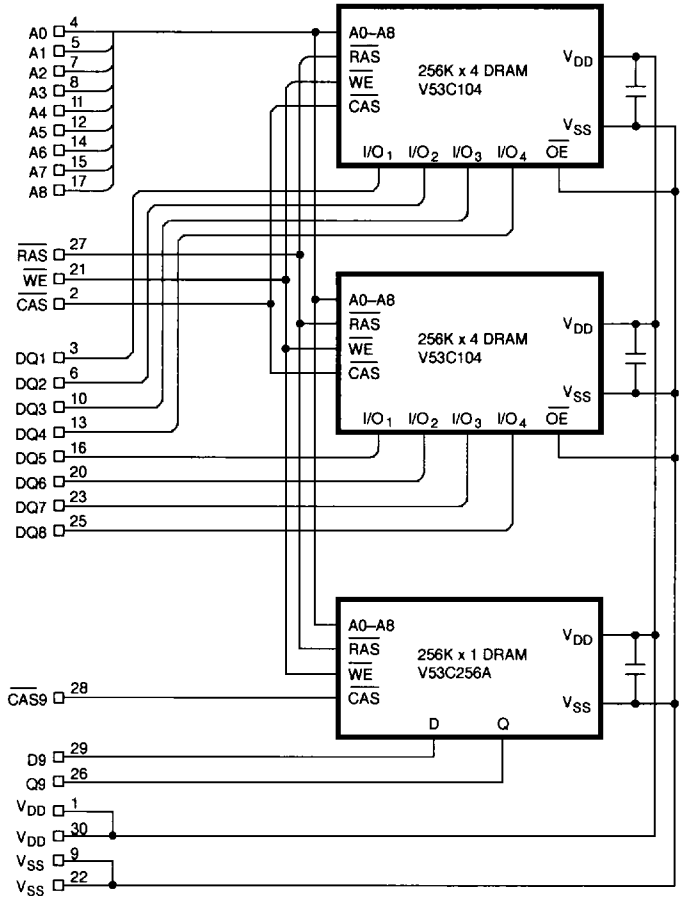
T_A = 0°C TO 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V

Symbol	Parameter	Min.	Max.	Unit
C_{IN}	Input Capacitance, Address Inputs		12	pF
C_{IN}	Input Capacitance, $\overline{RAS}$, $\overline{WE}$		15	pF
$C_{IN(DQ)}$	Input Capacitance, Data Inputs		14	pF
$C_{IN(CAS)}$	Input Capacitance, $\overline{CAS}$		10	pF
$C_{IN(CAS9)}$	Input Capacitance, $\overline{CAS9}$		5	pF
$C_{IN(D9)}$	Input Capacitance, D9		4	pF
$C_{O(Q9)}$	Output Capacitance, Q9		6	pF
$C_{O(VDD)}$	Decoupling Capacitance	0.2		µF

*Note: Capacitance is sampled and not 100% tested

Functional Diagram

x 9 Organization



NOTE: ***x 8 Organization***
Pins 26, 28, 29 are not connected

DC and Operating Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Power	Access Time (ns)	V104J8		V104J9		Unit	Test Conditions	Notes
				Min.	Max.	Min.	Max.			
I_{LI}	Input Leakage Current (any input pin)			–20	20	–30	30	µA	$V_{SS} \le V_{IN} \le V_{DD}$	
I_{LO}	Output Leakage Current (for High-Z State)			–10	10	–10	10	µA	$V_{SS} \le V_{OUT} \le V_{DD}$ $\overline{RAS}$,$\overline{CAS}$ at V_{IH}	
I_{DD1}	V_{DD} Supply Current, Operating		70		170		240	mA	$t_{RC} = t_{RC}$ (min.)	1,2
			80		150		210			
			100		130		180			
I_{DD2}	V_{DD} Supply Current, TTL Standby	STD			4		7.5	mA	$\overline{RAS}$,$\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			4		6			
I_{DD3}	V_{DD} Supply Current, $\overline{RAS}$-Only Refresh		70		170		240	mA	$t_{RC} = t_{RC}$ (min.)	2
			80		150		210			
			100		130		180			
I_{DD4}	V_{DD} Supply Current, Fast Page Mode Operation		70		130		175	mA	Minimum Cycle	1,2
			80		110		150			
			100		100		135			
I_{DD5}	V_{DD} Supply Current, Standby, Output Enabled	STD			6		10	mA	$\overline{RAS}$=V_{IH},$\overline{CAS}$=V_{IL} other inputs ≥ V_{SS}	1
		LOW			4		6.5			
I_{DD6}	V_{DD} Supply Current, CMOS Standby	STD			2		5	mA	$\overline{RAS} \ge V_{DD}$ –0.2 V, $\overline{CAS}$ at V_{IH} other inputs ≥ V_{SS}	
		LOW			2		3.2			
V_{IL}	Input Low Voltage (all inputs)			–1	0.8	–1	0.8	V		3
V_{IH}	Input High Voltage (all inputs)			2.4	VDD +1	2.4	VDD +1	V		3
V_{OL}	Output Low Voltage				0.4		0.4	V	I_{OL} = 4.2 mA	
V_{OH}	Output High Voltage			2.4		2.4		V	I_{OH} = –5 mA	

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AC Characteristics

T_A = 0°C to 70°C, V_{DD} = 5 V ±10%, V_{SS} = 0V unless otherwise noted
AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t_{RL1RH1}	t_{RAS}	$\overline{RAS}$ Pulse Width	70	75K	80	75K	100	75K	ns	
2	t_{RL2RL2}	t_{RC}	Read or Write Cycle Time	130		150		180		ns	
3	t_{RH2RL2}	t_{RP}	$\overline{RAS}$ Precharge Time	50		60		70		ns	
4	t_{RL1CH1}	t_{CSH}	$\overline{CAS}$ Hold Time	70		80		100		ns	
5	t_{CL1CH1}	t_{CAS}	$\overline{CAS}$ Pulse Width	20		20		25		ns	
6	t_{RL1CL1}	t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay	20	50	20	60	25	75	ns	4
7	t_{WH2CL2}	t_{RCS}	Read Command Setup Time	0		0		0		ns	
8	t_{AVRL2}	t_{ASR}	Row Address Setup Time	0		0		0		ns	
9	t_{RL1AX}	t_{RAH}	Row Address Hold Time	10		10		15		ns	
10	t_{AVCL2}	t_{ASC}	Column Address Setup Time	0		0		0		ns	
11	t_{CL1AX}	t_{CAH}	Column Address Hold Time	15		15		20		ns	
12	$t_{CL1RH1(R)}$	$t_{RSH(R)}$	$\overline{RAS}$ Hold Time (Read Cycle)	20		20		25		ns	
13	t_{CH2RL2}	t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	5		5		10		ns	
14	t_{CH2WX}	t_{RCH}	Read Command Hold Time Referenced to $\overline{CAS}$	0		0		0		ns	5
15	t_{RH2WX}	t_{RRH}	Read Command Hold Time Referenced to $\overline{RAS}$	0		0		0		ns	5
16	t_{CL1QV}	t_{CAC}	Access Time from $\overline{CAS}$		20		20		25	ns	6,7
17	t_{RL1QV}	t_{RAC}	Access Time from $\overline{RAS}$		70		80		100	ns	6,8,9
18	t_{AVQV}	t_{CAA}	Access Time from Column Address		35		40		50	ns	6,7,10
19	t_{CL1QX}	t_{LZ}	$\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
20	t_{CH2QZ}	t_{HZ}	$\overline{CAS}$ to High-Z Output	0	20	0	20	0	20	ns	16
21	t_{RL1AX}	t_{AR}	Column Address Hold Time from $\overline{RAS}$	55		60		75		ns	
22	t_{RL1AV}	t_{RAD}	$\overline{RAS}$ to Column Address Delay Time	15	35	15	40	20	55	ns	11

AC Characteristics (Cont'd.)

#	JEDEC Symbol	Symbol	Parameter	70/70L		80/80L		100/100L		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
23	$t_{CL1RH1(W)}$	$t_{RSH(W)}$	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		25		ns	
24	t_{WL1CH1}	t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	20		20		25		ns	
25	t_{WL1CL2}	t_{WCS}	Write Command Setup Time	0		0		0		ns	12,13
26	t_{CL1WH1}	t_{WCH}	Write Command Hold Time	15		15		20		ns	
27	t_{WL1WH1}	t_{WP}	Write Pulse Width	15		15		20		ns	
28	t_{RL1WH1}	t_{WCR}	Write Command Hold Time from $\overline{RAS}$	55		60		75		ns	
29	t_{WL1RH1}	t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	20		20		25		ns	
30	t_{DVWL2}	t_{DS}	Data in Setup Time	0		0		0		ns	14
31	t_{WL1DX}	t_{DH}	Data in Hold Time	15		15		20		ns	14
32	t_{CL1CH1}	t_{CRW}	$\overline{CAS}$ Pulse Width (RMW)	75		75		90		ns	
33	t_{CL2CL2}	t_{PC}	Fast Page Mode Read or Write Cycle Time	45		50		55		ns	
34	t_{CH2CL2}	t_{CP}	$\overline{CAS}$ Precharge Time	10		10		10		ns	
35	t_{AVRH1}	t_{CAR}	Column Address to $\overline{RAS}$ Setup Time	35		40		45		ns	
36	t_{CH2QV}	t_{CAP}	Access Time from Column Precharge		40		45		50	ns	7
37	t_{RL1DX}	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	55		60		75		ns	
38	t_{CL1RL2}	t_{CSR}	$\overline{CAS}$ Setup Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	10		10		10		ns	
39	t_{RH2CL2}	t_{RPC}	$\overline{RAS}$ to $\overline{CAS}$ Precharge Time	10		10		10		ns	
40	t_{RL1CH1}	t_{CHR}	$\overline{CAS}$ Hold Time $\overline{CAS}$-before-$\overline{RAS}$ Refresh	30		30		30		ns	
	t_T	t_T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t_{RI}	Refresh Interval (512 Cycles)		8		8		8	ms	17

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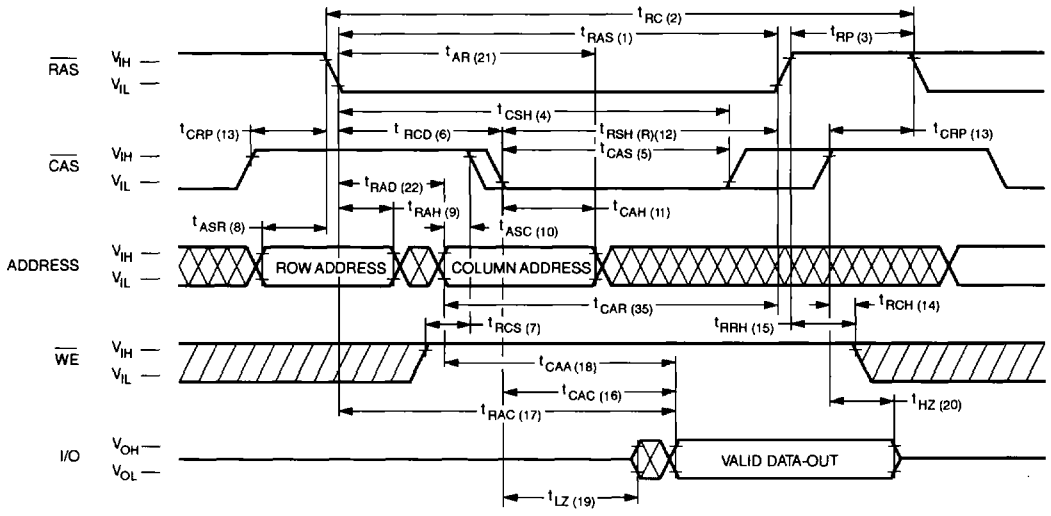
Notes:

1. I_{DD} is dependent on output loading when the device output is selected. Specified I_{DD} (max.) is measured with the output open.
2. I_{DD} is dependent upon the number of address transitions. Specified I_{DD} (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified V_{IL} (min.) is steady state operating. During transitions, V_{IL} (min.) may undershoot to −1.0 V for a period not to exceed 20 ns. All AC parameters are measured with V_{IL} (min.) ≥ V_{SS} and V_{IH} (max.) ≤ V_{DD}.
4. t_{RCD} (max.) is specified for reference only. Operation within t_{RCD} (max.) limits insures that t_{RAC} (max.) and t_{CAA} (max.) can be met. If t_{RCD} is greater than the specified t_{RCD} (max.), the access time is controlled by t_{CAA} and t_{CAC}.
5. Either t_{RRH} or t_{RCH} must be satisified for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longer of t_{CAA}, t_{CAC} or t_{CAP}.
8. Assumes that $t_{RAD} \leq t_{RAD}$ (max.). If t_{RAD} is greater than t_{RAD} (max.), t_{RAC} will increase by the amount that t_{RAD} exceeds t_{RAD} (max.).
9. Assumes that $t_{RCD} \leq t_{RCD}$ (max.). If t_{RCD} is greater than t_{RCD} (max.), t_{RAC} will increase by the amount that t_{RCD} exceeds t_{RCD} (max.).
10. Assumes that $t_{RAD} \geq t_{RAD}$ (max.).
11. Operation within the t_{RAD} (max.) limit ensures that t_{RAC} (max.) can be met. t_{RAD} (max.) is specified as a reference point only. If t_{RAD} is greater than the specified t_{RAD} (max.) limit, the access time is controlled by t_{CAA} and t_{CAC}.
12. t_{WCS} is not a restrictive operating parameter.
13. t_{WCS} (min.) must be satisfied in an Early Write Cycle.
14. t_{DS} and t_{DH} are referenced to the latter occurrence of $\overline{CAS}$ or $\overline{WE}$.
15. t_T is measured between V_{IH} (min.) and V_{IL} (max.). AC-measurements assume t_T = 5 ns.
16. t_{LZ} and t_{HZ} define the time at which D_{OUT} reaches an open circuit condition and are not referenced to the output voltage levels.
17. An initial 200 µs pause and 8 $\overline{RAS}$-containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

Waveforms of Read Cycle



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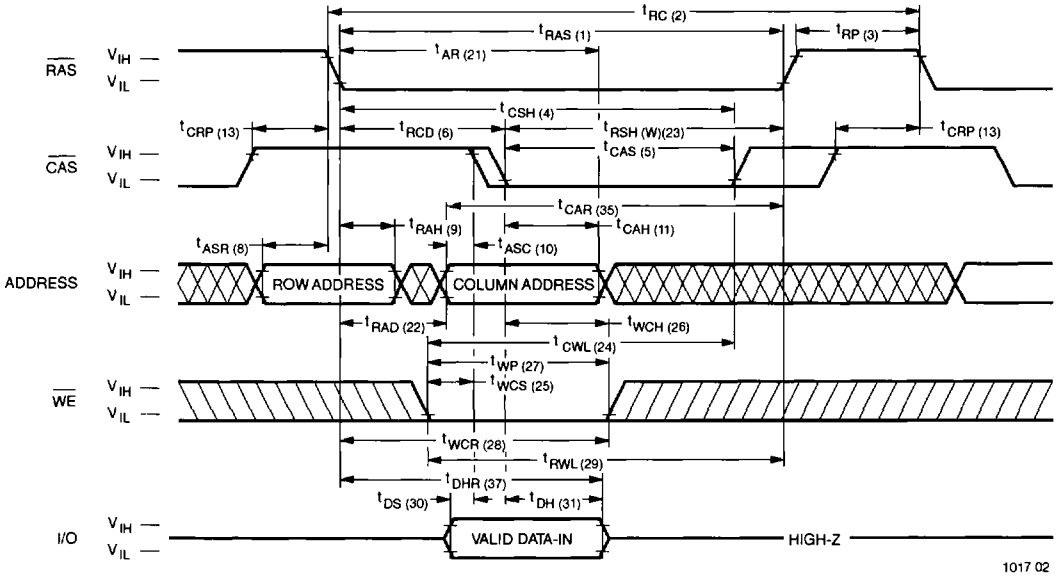
Waveforms of Early Write Cycle



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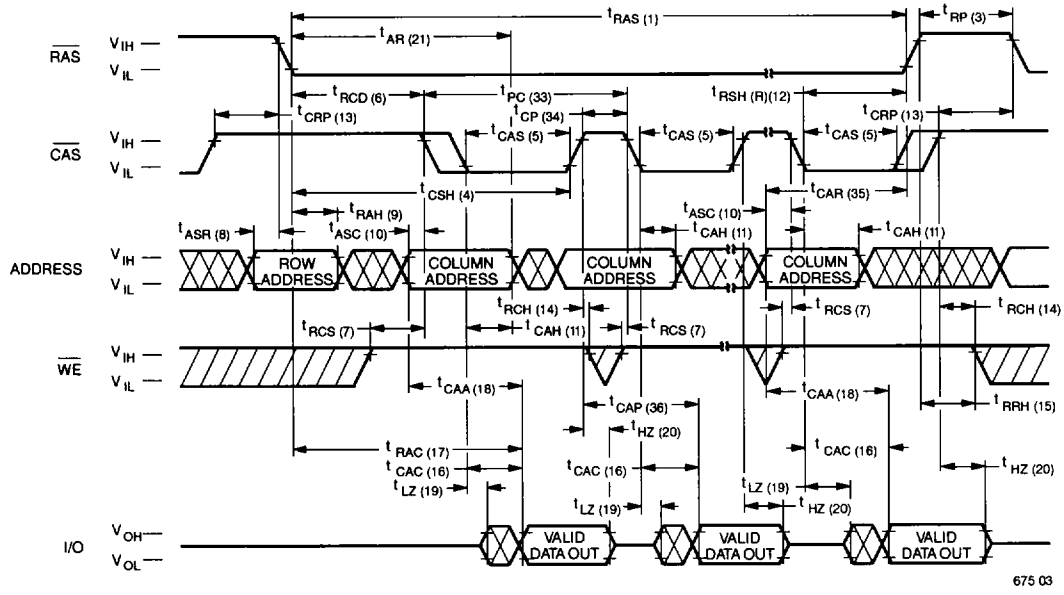
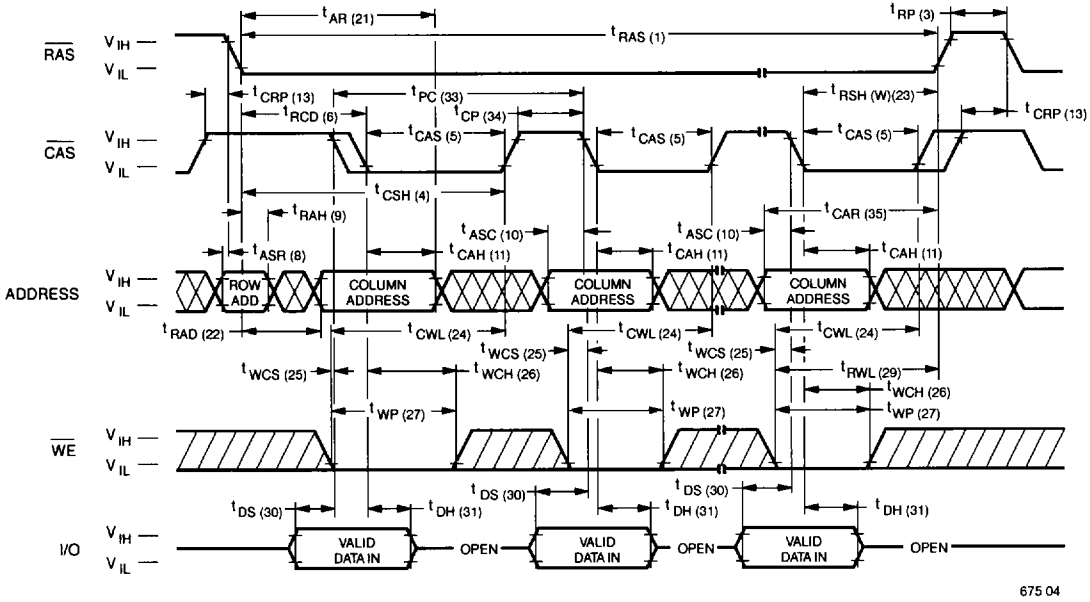
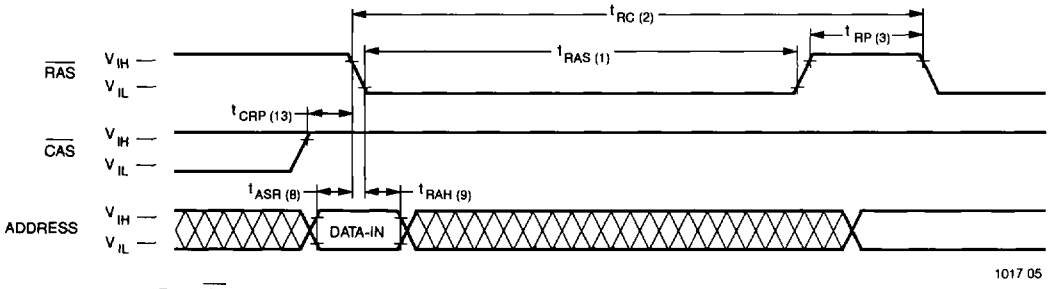
Waveforms of Fast Page Mode Read Cycle



Waveforms of Fast Page Mode Write Cycle

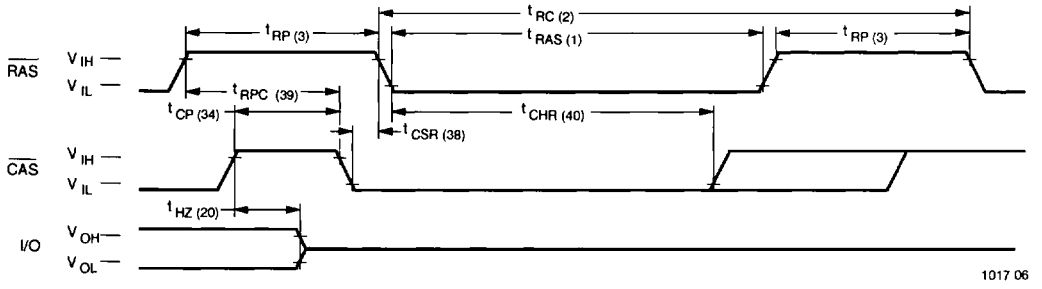


Waveforms of $\overline{RAS}$-Only Refresh Cycle



NOTE: $\overline{WE}$ = Don't care

Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Cycle



NOTE: $\overline{WE}$, A_0–A_8 = Don't care

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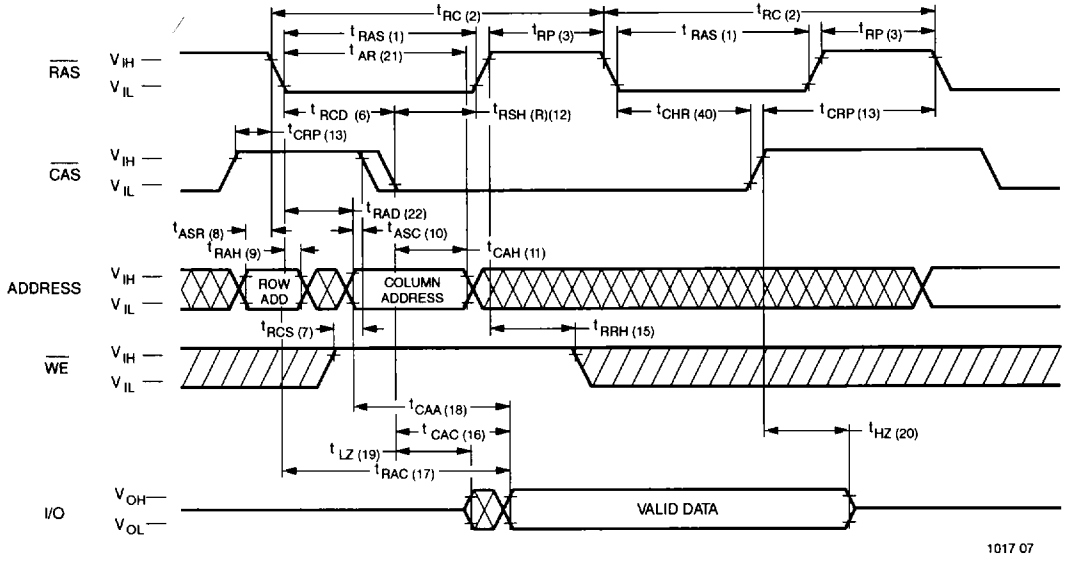
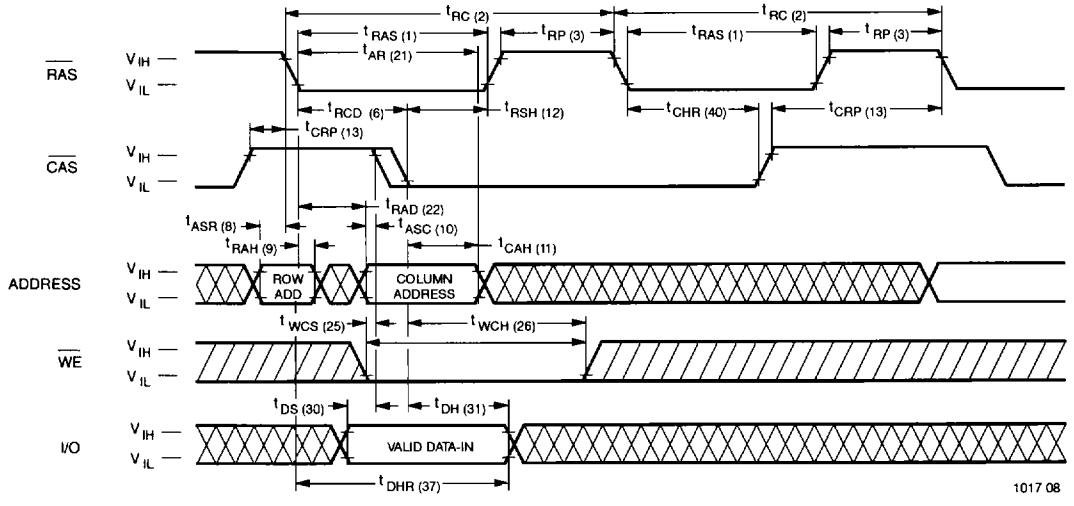
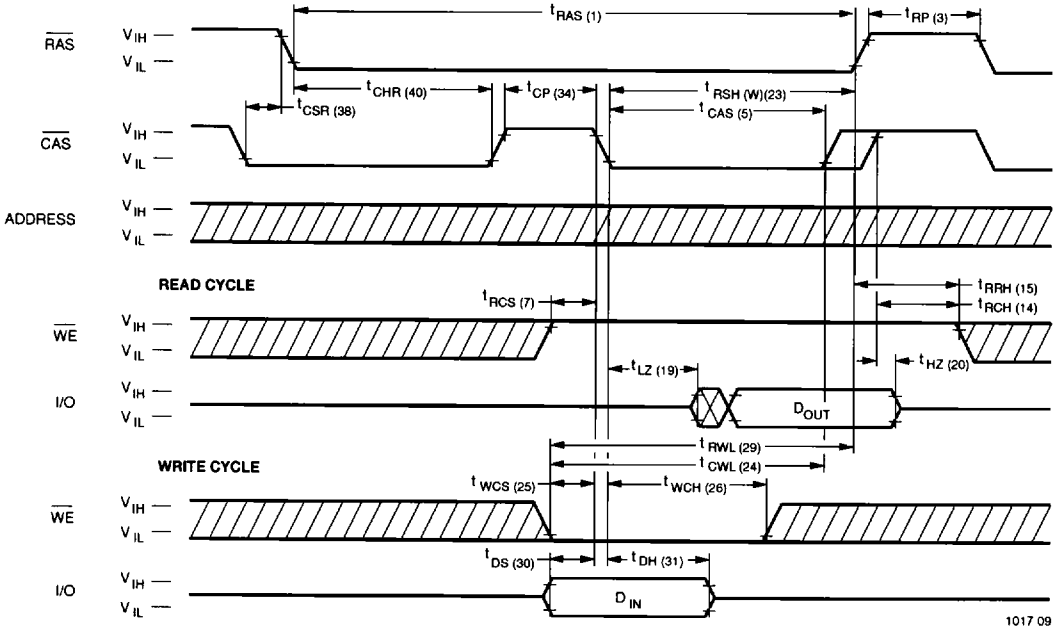
Waveforms of Hidden Refresh Cycle (Read)



Waveforms of Hidden Refresh Cycle (Write)



Waveforms of $\overline{CAS}$-before-$\overline{RAS}$ Refresh Refresh Counter Test Cycle



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