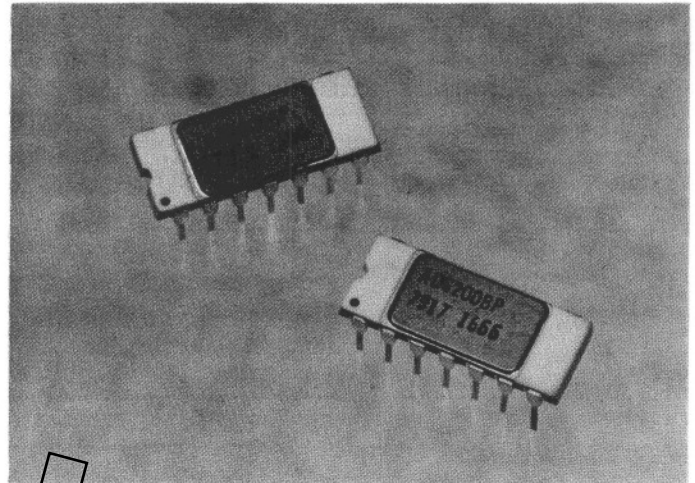


FEATURES

- Latch-Proof DI CMOS
- Overvoltage-Proof: $V_{SUPPLY} \pm 25V$
- Superior DG-200 Replacement
- Break-Before-Make Switching Action
- R_{ON} : 100Ω max over Full Temperature Range
- Direct TTL/CMOS Interface



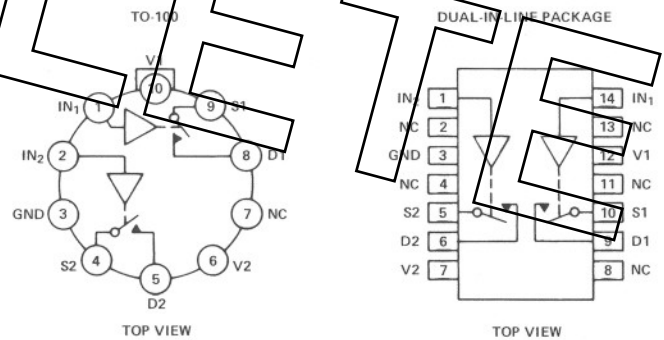
OBSOLETE

GENERAL DESCRIPTION

The ADG200 is a dual single-pole-single-throw analog switch. In the ON condition, the switch conducts current in either direction, maintaining nearly constant ON resistance over the entire analog signal range. In the OFF condition, the switch blocks voltages of peak values equal to the switch $V+$ and $V-$ supplies. Switch action is break-before-make. The digital inputs interface directly to TTL or CMOS logic over the full operating temperature range.

Fabricated using an advanced monolithic dielectrically-isolated CMOS process, the ADG200 is a superior plug-in replacement for the DG200. The ADG200 provides additional advantages (over the DG200) of: overvoltage protection to $\pm 25V$ beyond the power supplies, total latch-free operation, much lower power dissipation (30mW max) and faster switching time.

PIN CONFIGURATION



SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ORDERING INFORMATION

Commercial 0 to +70°C	Industrial -25°C to +85°C		Military -55°C to +125°C	
Plastic	Ceramic	TO-100	Ceramic	TO-100
ADG200CJ	ADG200BP	ADG200BA	ADG200AP	ADG200AA ADG200AA/883

Note: "/883" version is 100% screened to MIL-STD-883, class B as per note 7, page 2.

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SPECIFICATIONS

CHARACTERISTIC ¹	TYP ¹ +25°C	MAX LIMITS						UNITS	TEST CONDITIONS ⁸ Unless Noted V ₁ = +15V V ₂ = -15V, GND = 0V	
		AA, AP Suffix			BA, BP/CJ Suffix					
		-55°C ²	+25°C	+125°C	-25/0°C ²	+25°C	+85/70°C ²			
SWITCH										
r _{DS(ON)} Drain-Source ON Resistance	60	70	70	100	80	80	100	Ω	V _D = 10V V _D = -10V	V _{IN} = 0.8V I _S = 0.1mA
	40	70	70	100	80	80	100			
I _{S(OFF)} Source OFF Leakage Current	0.2	500	2	500	500	5	500	nA	V _S = 10V, V _D = -10V V _S = -10V, V _D = 10V V _D = 10V, V _S = -10V V _D = -10V, V _S = 10V V _D = V _S = 10V V _D = V _S = -10V	V _{IN} = 2.4V V _{IN} = 0.8V
I _{D(OFF)} Drain OFF Leakage Current	0.3	500	2	500	500	5	500			
I _{D(OFF)} Channel ON Leakage Current	-0.3	-500	-2	-500	-500	-5	-500			
I _{D(ON)} ³ Channel ON Leakage Current	0.1	500	2	500	500	2	500			
	-0.1	-500	-2	-500	-500	-2	-500			
INPUT										
I _{INH} Input Current Input Voltage High		-10	-1	-10	-10	-1	-10	μA	V _{IN} = 2.4V V _{IN} = 15V	
			10	1	10	10	1			10
I _{IN(PEAK)} ⁴ Peak Input Current Required for Transition		NOT APPLICABLE ⁴								
I _{INL} Input Current Input Voltage Low		-10	-1	-10	-10	-1	-10	μA	V _{IN} = 0V	
DYNAMIC										
t _{ON} Turn-ON Time ⁵	300		1000 ²			1000 ²		ns	V _{IN} = 3.5V to 0V V _{IN} = 0V to 3.5V	R _L = 1kΩ, C _L = 35pF V _S = ±5V
t _{OFF} Turn-OFF Time ⁵	20		500 ²			500 ²				
C _{S(OFF)} Source OFF Capacitance	11							pF	V _S = 0V, V _{IN} = 5V	
C _{D(OFF)} Drain OFF Capacitance	11							pF	V _D = 0V, V _{IN} = 5V	f = 140kHz
C _{D(ON)} - C _{S(ON)} Channel ON Capacitance	28							pF	V _D = V _S = 0V V _{IN} = 0V	
OFF Isolation ⁶	64							dB	V _{IN} = 5V, R _L = 1kΩ, C _L = 15pF V _S = 7V _{rms} , f = 500kHz	
SUPPLY										
I ₁ Positive Supply Current	0.02	2	1	2	2	1	2	mA	Both Channels ON; V _{IN} = 0V	
I ₂ Negative Supply Current	-0.02	-2	-1	-2	-2	-1	-2			
I ₁ Positive Supply Current	0.1	2	1	2	2	1	2	mA	Both Channels OFF; V _{IN} = 5V	
I ₂ Negative Supply Current	-0.02	-2	-1	-2	-2	-1	-2			
PRICES										
	1-24	25-99	100-499	500-999	1K					\$
ADG200CJ	3.50	3.00	2.50	2.25	2.00					
ADG200BP	11.00	8.50	7.00	7.00	6.50					
ADG200AP	13.00	10.00	8.50	8.50	7.75					
ADG200BA	3.50	3.00	2.50	2.25	2.00					
ADG200AA	11.00	9.00	7.75	7.75	7.00					
ADG200AA/883 ⁷	15.00	12.75	11.25	11.25	10.75					

NOTES:

¹ Typical values for information only, not guaranteed or production tested.

² Guaranteed, not subject to 100% production test.

³ I_{D(ON)} is leakage from driver gate into ON switch.

⁴ Digital inputs are MOS gates. Typical leakage (+25°C) is less than 1 nanoamp.

This is in contrast to other designs which require typically 150μA to switch.

⁵ Switch action is guaranteed break-before-make.

⁶ OFF isolation (dB) = 20 log V_S/V_D where V_S = input to OFF switch and V_D = output.

⁷ 100% screened to MIL-STD-883, method 5004, para. 3.1.1 through 3.1.12 for a class B device. Final electrical tests are:

r_{DS(ON)}, I_{S(OFF)}, I_{D(OFF)}, I_{INH}, I_{INL}, I₁, and I₂ at +25°C and +125°C (AA/883 version).

⁸ Functional operation is possible for supply voltages less than ±15V,

but the input logic switching threshold will shift (see page 4).

Specifications subject to change without notice.

CAUTION:

ESD (Electro-Static-Discharge) sensitive device. The digital control inputs are zener protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are removed.



ABSOLUTE MAXIMUM RATINGS

V _{IN} (Digital Input) to Ground	-.0.3V, V ₁
V _S or V _D to V ₁	
(1 second surge)	+25V, -40V
(continuous)	+20V, -35V
V _S or V _D to V ₂	
(1 second surge)	-25V, +40V
(continuous)	-20V, +35V
V ₁ to Ground	-.0.3V, +17V
V ₂ to Ground	+.0.3V, -17V
Current, Any Terminal Except S or D	30mA
Current, S or D	50mA
Current, S or D Pulsed	
(1ms, 10% duty cycle max)	.150mA

Operating Temperature

AA, AP Suffix	-55°C to +125°C
BA, BP Suffix	-25°C to +85°C
CJ Suffix	0°C to +70°C

Storage Temperature

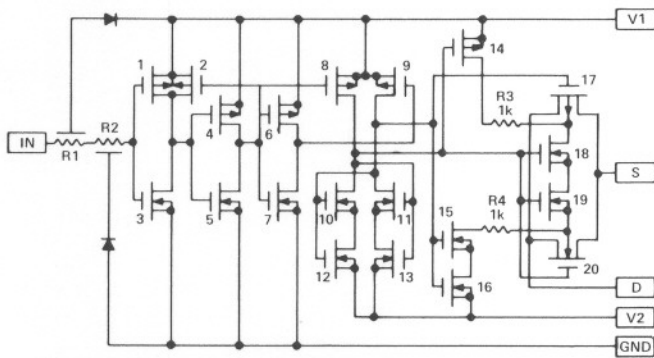
CJ Suffix	-65°C to +125°C
All Others	-65°C to +150°C

Power Dissipation (Package)*

Metal Can**	450mW
14 Pin Ceramic DIP***	825mW
14 Pin Plastic DIP****	470mW

- * Devices with all leads welded or soldered to printed circuit board
- ** Derate 6mW/°C above +75°C
- *** Derate 11mW/°C above +75°C
- **** Derate 6.5mW/°C above +25°C

CIRCUIT DESCRIPTION



NOTE: LOGIC "0" ON IN TERMINAL CLOSSES SWITCH BETWEEN S AND D.

Figure 1. Schematic Diagram (1 of 2 channels)

CMOS devices make excellent analog switches, however, problems with overvoltage and latch-up phenomenon necessitate protection circuitry. However, these protection circuits either cause degradation of important switch parameters such as R_{ON} or leakage, or provide only limited protection in the event of overvoltage.

The ADG200 switch utilizes a dielectrically-isolated CMOS fabrication process to eliminate the four-layer structure found in junction-isolated CMOS, thus providing latch-free operation.

A typical switch channel is shown in Figure 1. The output switching element consists of device numbers 17 and 20. Operation is as follows: for an "ON" switch, the gate of device 20 is V_1 and the gate of device 17 is V_2 from the driver circuits. Device numbers 14, 15, and 16 are "OFF" and numbers 18 and 19 are "ON". Hence, the back-gates of the P- and N-channel output devices (numbers 17 and 20) are tied together and floating. Floating the output switch back-gates with the signal input provides a flatter R_{ON} versus V_S response.

For an "OFF" switch, device numbers 18 and 19 are "OFF", and the back-gates of devices 17 and 20 are tied through 1kΩ resistors R_3 and R_4 to the respective supply voltages through the "ON" devices 14, 15, and 16.

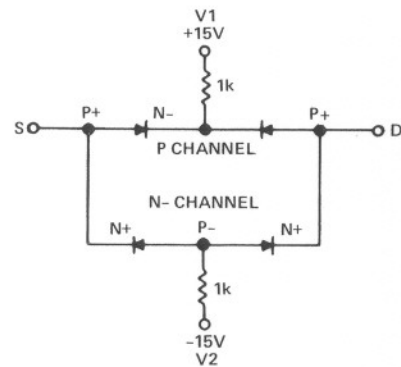


Figure 2. ADG200 Output Switch Diode Equivalent Circuit

If a voltage is applied to the S or D terminals which exceeds V_1 or V_2 , the S- or D-to-back-gate diode is forward biased; however, R_3 and R_4 provide current limiting action (Fig. 2).

Consequently, without external current limiting resistance (or increased R_{ON}), the ADG200 series switches provide:

1. Latch-proof operation.
2. Overvoltage protection 25V beyond the V_1 or V_2 supply voltage.

An equivalent circuit of the output switch element in Figure 2 shows that, indeed, the 1kΩ limiting resistors are in series with the back-gates of the P- and N-channel output devices — not in series with the signal path between the S & D terminals.

In some applications it is possible to run on a parasitic NPN (drain to back-gate to source of the N-channel) transistor which causes device destruction under certain conditions. This case will only manifest itself when a negative overvoltage (and not a positive overvoltage) exists with another voltage source on the other side of the switch. Current limitation through external resistors (200Ω) or the output of op amps will prevent damage to the device.

TYPICAL PERFORMANCE CHARACTERISTICS

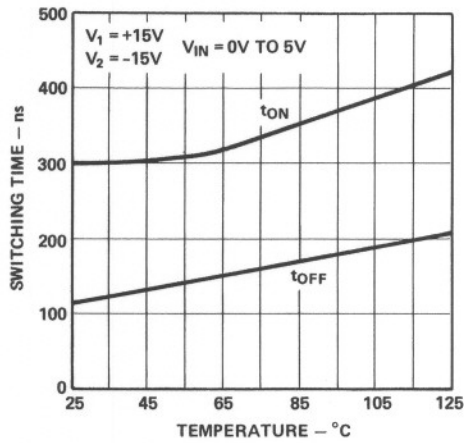


Figure 3. Switching Time vs. Temperature

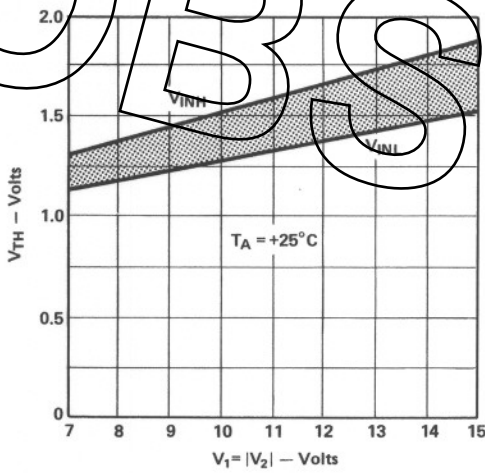
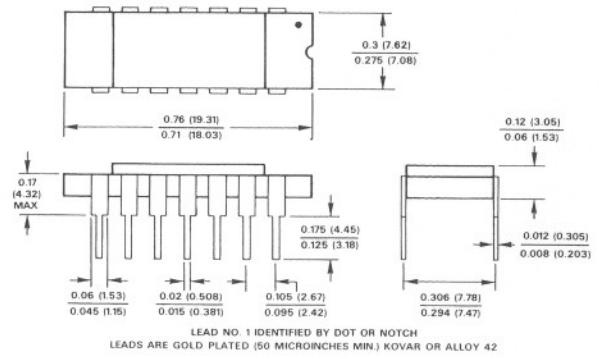


Figure 4. Input Logic Threshold vs. Power Supply Voltage

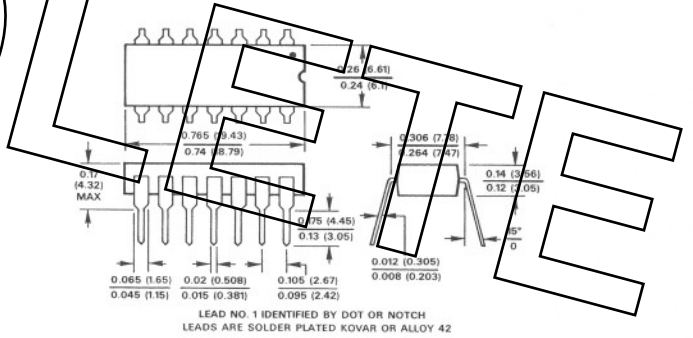
MECHANICAL INFORMATION

Dimensions shown in inches and (mm).

14-PIN CERAMIC DIP

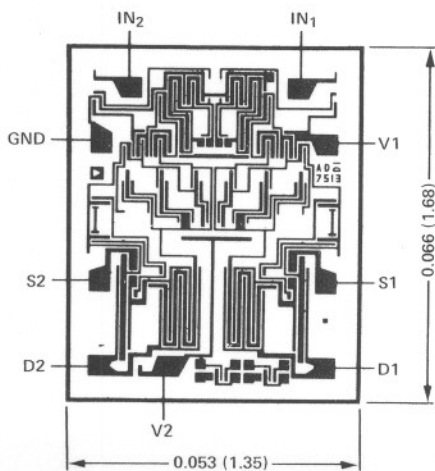


14-PIN PLASTIC DIP



BONDING DIAGRAM

Dimensions shown in inches and (mm).



- NOTES:
 1. BOND GND PIN FIRST TO MINIMIZE ESD HAZARD.
 2. BONDING PADS ARE 0.004 X 0.004 INCHES (0.102 X 0.102mm).

TO-100

