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MTM20P10

TMOS POWER FET
20 AMPERES
$R_{DS(on)}$ = 0.15 OHM
100 VOLTS

Designer's Data Sheet

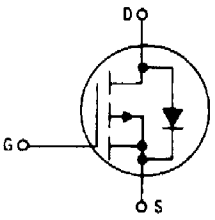
Power Field Effect Transistor

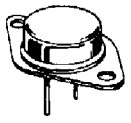
P-Channel Enhancement-Mode Silicon Gate

TMOS®

This TMOS Power FET is designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — I_{DSS}, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads





TO-204AA

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	100	Vdc
Drain-Gate Voltage (R_{GS} = 1 MΩ)	V_{DGR}	100	Vdc
Gate-Source Voltage Continuous Non-repetitive ($t_p \leq 50\ \mu s$)	 V_{GS} V_{GSM}	 ±20 ±40	 Vdc Vpk
Drain Current Continuous Pulsed	 I_D I_{DM}	 20 80	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	125 1	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance Junction to Case Junction to Ambient	 $R_{\theta JC}$ $R_{\theta JA}$	 1 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	300	°C

NJ Semi-Conductors reserves the right to change test conditions, parameter limits and package dimensions without notice. Information furnished by NJ Semi-Conductors is believed to be both accurate and reliable at the time of going to press. However, NJ Semi-Conductors assumes no responsibility for any errors or omissions discovered in its use. NJ Semi-Conductors encourages customers to verify that datasheets are current before placing orders.

Quality Semi-Conductors

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Max	Unit
OFF CHARACTERISTICS					
Drain-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	100	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = Rated V_{DSS}, V_{GS} = 0) (V_{DS} = Rated V_{DSS}, V_{GS} = 0, T_J = 125°C)		I_{DSS}	 — —	 10 100	μAdc
Gate-Body Leakage Current, Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	100	nAdc
Gate-Body Leakage Current, Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1 mA) T_J = 100°C		$V_{GS(th)}$	 2 1.5	 4.5 4	Vdc
Static Drain-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 10 Adc)		$R_{DS(on)}$	—	0.15	Ohm
Drain-Source On-Voltage (V_{GS} = 10 V) (I_D = 20 Adc) (I_D = 10 Adc, T_J = 100°C)		$V_{DS(on)}$	 — —	 3.2 3	Vdc
Forward Transconductance (V_{DS} = 10 V, I_D = 10 A)		g_{FS}	5	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1 MHz) See Figure 10	C_{iss}	—	2000	pF
Output Capacitance		C_{oss}	—	950	
Reverse Transfer Capacitance		C_{rss}	—	400	
SWITCHING CHARACTERISTICS* (T_J = 100°C)					
Turn-On Delay Time	(V_{DD} = 25 V, I_D = 0.5 Rated I_D, R_{gen} = 50 ohms) See Figures 12 and 13	$t_{d(on)}$	—	45	ns
Rise Time		t_r	—	200	
Turn-Off Delay Time		$t_{d(off)}$	—	150	
Fall Time		t_f	—	150	
Total Gate Charge	(V_{DS} = 0.8 Rated V_{DSS}, I_D = Rated I_D, V_{GS} = 10 V) See Figure 11	Q_g	52 (Typ)	75	nC
Gate-Source Charge		Q_{gs}	22 (Typ)	—	
Gate-Drain Charge		Q_{gd}	30 (Typ)	—	
SOURCE DRAIN DIODE CHARACTERISTICS*					
Forward On-Voltage	(I_S = Rated I_D, V_{GS} = 0)	V_{SD}	2.8 (Typ)	4	Vdc
Forward Turn-On Time		t_{on}	100 (Typ)	—	ns
Reverse Recovery Time		t_{rr}	350 (Typ)	—	ns

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.