Supervisory Circuits with Watchdog and Manual Reset in 5-Lead SOT-23

Data Sheet **ADM8316/ADM8318/ADM8319/ADM8320/ADM8321/ADM8322**

FEATURES

- 26 reset threshold options
  - 2.5 V to 5 V in 100 mV increments
- 4 reset timeout options
  - 1 ms, 20 ms, 140 ms, and 1120 ms (minimum)
- 4 watchdog timeout options
  - 6.3 ms, 102 ms, 1.6 sec, and 25.6 sec (typical)
- Manual reset input
- Multiple reset output options
- Low power consumption
- Specified over wide temperature range (−40°C to +125°C)
- Qualified for automotive applications
- 5-lead SOT-23 package

APPLICATIONS

- Automotive infotainment
- Microprocessor systems
- Computers
- Controllers
- Intelligent instruments
- Portable equipment

FUNCTIONAL BLOCK DIAGRAMS

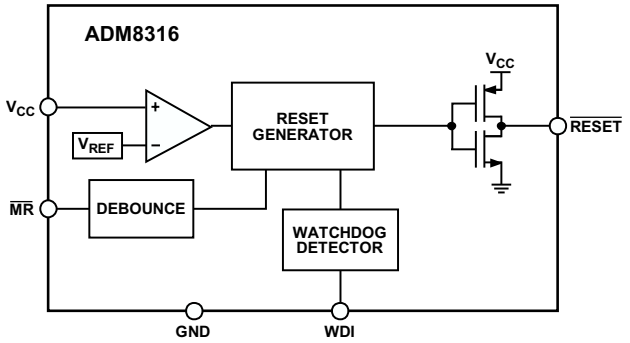

Figure 1. ADM8316

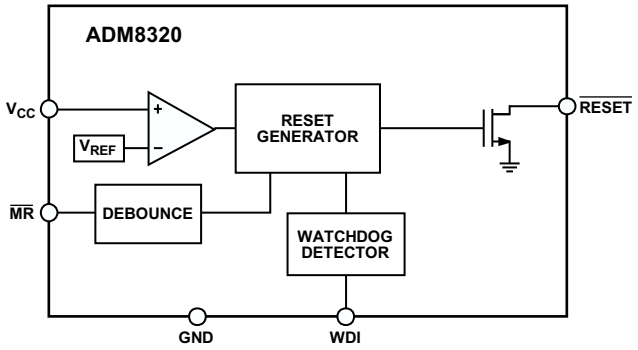

Figure 2. ADM8320

GENERAL DESCRIPTION

The ADM8316/ADM8318/ADM8319/ADM8320/ADM8321/ADM8322 are supervisory circuits that monitor power supply voltage levels and code execution integrity in microprocessor-based systems. As well as providing power-on reset signals, an on-chip watchdog timer can reset the microprocessor if it fails to strobe within a preset timeout period. A reset signal can also be asserted by an external push-button switch through a manual reset input. The six devices feature different combinations of watchdog input, manual reset input, and output stage configuration, as shown in Table 6.

Each device is available in a choice of 26 reset threshold options ranging from 2.5 V to 5 V in 100 mV increments. There are also four reset timeout options of 1 ms, 20 ms, 140 ms, and 1120 ms (minimum) and four watchdog timeout options of 6.3 ms, 102 ms, 1.6 sec, and 25.6 sec (typical).

The ADM8316/ADM8318/ADM8319/ADM8320/ADM8321/ADM8322 are available in 5-lead SOT-23 packages and typically consume only 10 µA, making them suitable for use in low power, portable applications.

Rev. 0 Document Feedback

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REVISION HISTORY

10/13—Revision 0: Initial Version

SPECIFICATIONS

V_{CC} = (V_{TH} + 1.5%) to 5.5 V, T_A = −40°C to +125°C, unless otherwise noted. Typical values are at T_A = 25°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY					
V_{CC} Operating Voltage Range[1]	0.9		5.5	V	
V_{CC} that Guarantees Valid Output	0.9			V	
Supply Current (WDI Floating)		10	20	µA	V_{CC} = 5.5 V
		10	18	µA	V_{CC} = 3.6 V
RESET THRESHOLD VOLTAGE[2]	V_{TH} − 1%	V_{TH}	V_{TH} + 1%	V	T_A = 25°C
	V_{TH} − 1.5%	V_{TH}	V_{TH} + 1.5%	V	T_A = −40°C to +125°C
RESET THRESHOLD TEMPERATURE COEFFICIENT		20		ppm/°C	
RESET THRESHOLD HYSTERESIS		2.5 × V_{TH}		mV	
RESET TIMEOUT PERIOD					See Table 7
Reset Timeout Option A	1	1.4	1.8	ms	
Reset Timeout Option B	20	28	36	ms	
Reset Timeout Option C	140	200	260	ms	
Reset Timeout Option D	1120	1600	2080	ms	
V_{CC} TO RESET DELAY, t_{RD}		90		µs	V_{CC} falling at 1 mV/µs
PUSH-PULL OUTPUT (ADM8316, ADM8318, ADM8319, ADM8321, ADM8322)					
$\overline{\text{RESET}}$ Output Voltage			0.2	V	V_{CC} ≥ 0.9 V, I_{SINK} = 25 µA
			0.2	V	V_{CC} ≥ 1.2 V, I_{SINK} = 100 µA
			0.2	V	V_{CC} ≥ 2.7 V, I_{SINK} = 1.2 mA
			0.3	V	V_{CC} ≥ 4.5 V, I_{SINK} = 3.2 mA
	0.9 × V_{CC}			V	V_{CC} ≥ 2.7 V, I_{SOURCE} = 500 µA
	0.9 × V_{CC}			V	V_{CC} ≥ 4.5 V, I_{SOURCE} = 800 µA
$\overline{\text{RESET}}$ Rise Time		50	100	ns	From 10% to 90% V_{CC}, C_L = 5 pF, V_{CC} = 3.3 V
RESET Output Voltage			0.2	V	V_{CC} ≥ 2.7 V, I_{SINK} = 1.2 mA
			0.3	V	V_{CC} ≥ 4.5 V, I_{SINK} = 3.2 mA
	0.9 × V_{CC}			V	V_{CC} ≥ 2.7 V, I_{SOURCE} = 500 µA
	0.9 × V_{CC}			V	V_{CC} ≥ 4.5 V, I_{SOURCE} = 800 µA
OPEN-DRAIN OUTPUT (ADM8320, ADM8321, ADM8322)					
$\overline{\text{RESET}}$ Output Voltage			0.2	V	V_{CC} ≥ 0.9 V, I_{SINK} = 25 µA
			0.2	V	V_{CC} ≥ 1.2 V, I_{SINK} = 100 µA
			0.2	V	V_{CC} ≥ 2.7 V, I_{SINK} = 1.2 mA
			0.3	V	V_{CC} ≥ 4.5 V, I_{SINK} = 3.2 mA
Open-Drain Reset Output Leakage Current			1	µA	
WATCHDOG INPUT (ADM8316, ADM8318, ADM8320, ADM8321)					
Watchdog Timeout Period, t_{WD}					See Table 8
Watchdog Timeout Option W	4.5	6.3	8.1	ms	
Watchdog Timeout Option X	72	102	132	ms	
Watchdog Timeout Option Y	1.12	1.6	2.24	sec	
Watchdog Timeout Option Z	18.0	25.6	33.2	sec	
WDI Pulse Width	50			ns	V_{IL} = 0.3 × V_{CC}, V_{IH} = 0.7 × V_{CC}
WDI Input Threshold	0.3 × V_{CC}		0.7 × V_{CC}	V	
WDI Input Current		35	100	µA	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
MANUAL RESET INPUT (ADM8316, ADM8319, ADM8320, ADM8322)					
V_{IL}			0.8	V	
V_{IH}	2.0			V	
$\overline{MR}$ Input Pulse Width	1			µs	
$\overline{MR}$ Glitch Rejection		100		ns	
$\overline{MR}$ Pull-Up Resistance	35	75	125	kΩ	
$\overline{MR}$ to Reset Delay		350		ns	V_{CC} = 5 V

[1] The device switches from undervoltage reset to normal operation when 1.5 V < V_{CC} < 2.5 V.
[2] The device monitors V_{CC} through an internal factory trimmed voltage divider that programs the nominal reset threshold. Factory-trimmed reset thresholds are available in approximately 100 mV increments from 2.5 V to 5 V.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 2.

Parameter	Rating
V_{CC}	−0.3 V to +6 V
All Other Pins	−0.3 V to (V_{CC} + 0.3 V)
Output Current (RESET, $\overline{\text{RESET}}$)	20 mA
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
θ_{JA} Thermal Impedance, SOT-23	270°C/W
Lead Temperature	
Soldering (10 sec)	300°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

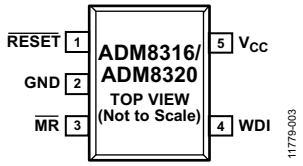

Figure 3. ADM8316/ADM8320 Pin Configuration

Table 3. ADM8316/ADM8320 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Active Low Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH}. This pin is a push-pull output stage for the ADM8316 and an open-drain output stage for the ADM8320.
2	GND	Ground.
3	$\overline{\text{MR}}$	Manual Reset Input. This is an active low input that, when forced low for greater than the glitch filter time, generates a reset. It features a 75 kΩ internal pull-up resistor.
4	WDI	Watchdog Input. Generates a reset if the logic level on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated. Leave this pin floating to disable the watchdog timer.
5	V_{CC}	Power Supply Voltage Being Monitored.

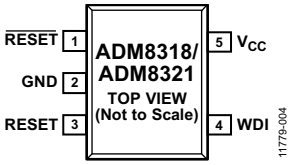

Figure 4. ADM8318/ADM8321 Pin Configuration

Table 4. ADM8318/ADM8321 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Active Low Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH}. This pin is a push-pull output stage for the ADM8318 and an open-drain output stage for the ADM8321.
2	GND	Ground.
3	RESET	Active High Push-Pull Reset Output.
4	WDI	Watchdog Input. Generates a reset if the logic level on the pin remains low or high for the duration of the watchdog timeout. The timer is cleared if a logic transition occurs on this pin or if a reset is generated. Leave this pin floating to disable the watchdog timer.
5	V_{CC}	Power Supply Voltage Being Monitored.

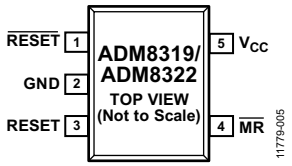

Figure 5. ADM8319/ADM8322 Pin Configuration

Table 5. ADM8319/ADM8322 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{RESET}}$	Active low Reset Output. Asserted whenever V_{CC} is below the reset threshold, V_{TH}. This pin is a push-pull output stage for the ADM8319 and an open-drain output stage for the ADM8322.
2	GND	Ground.
3	RESET	Active High Push-Pull Reset Output.
4	$\overline{\text{MR}}$	Manual Reset Input. This is an active low input that, when forced low for greater than the glitch filter time, generates a reset. It features a 75 kΩ internal pull-up resistor.
5	V_{CC}	Power Supply Voltage Being Monitored.

TYPICAL PERFORMANCE CHARACTERISTICS

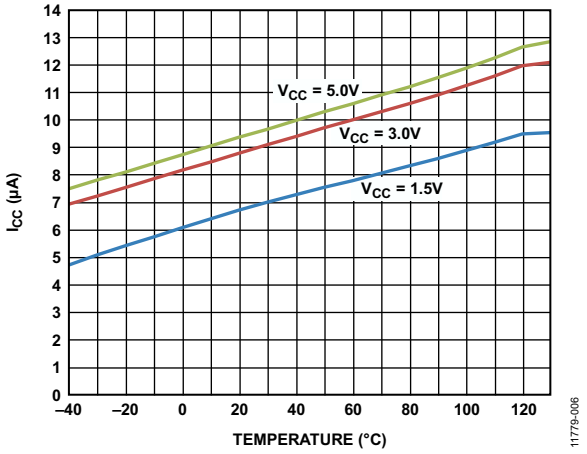

Figure 6. Supply Current (I_{CC}) vs. Temperature

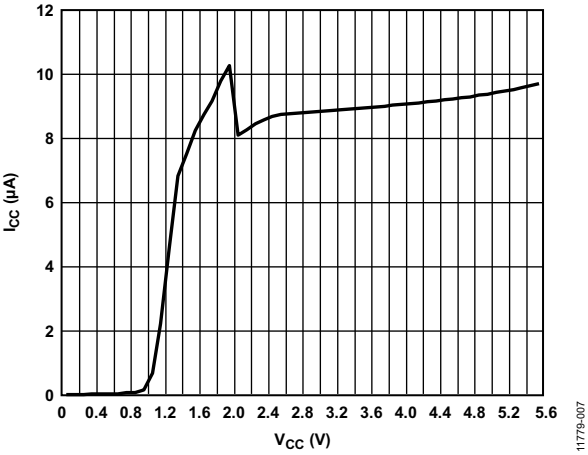

Figure 7. Supply Current (I_{CC}) vs. Supply Voltage (V_{CC})

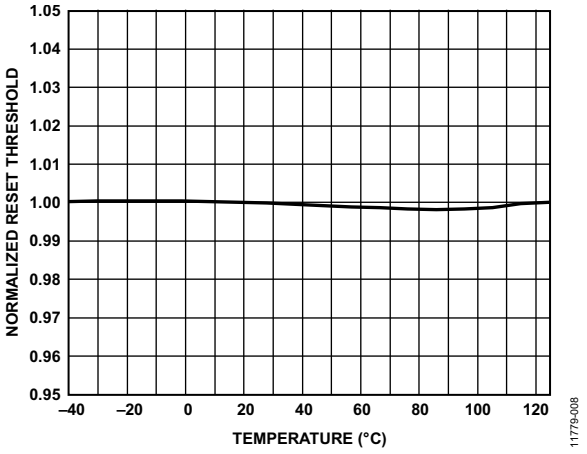

Figure 8. Normalized Reset Threshold vs. Temperature

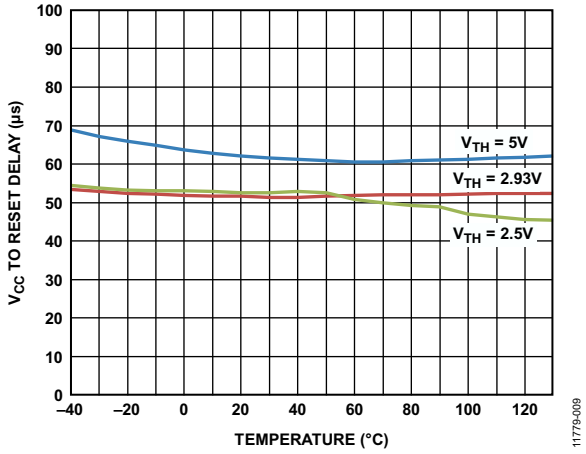

Figure 9. V_{CC} to Reset Delay vs. Temperature

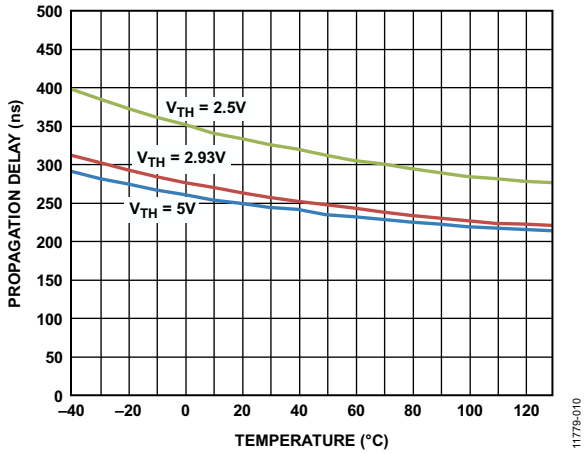

Figure 10. Manual Reset to Reset Propagation Delay vs. Temperature

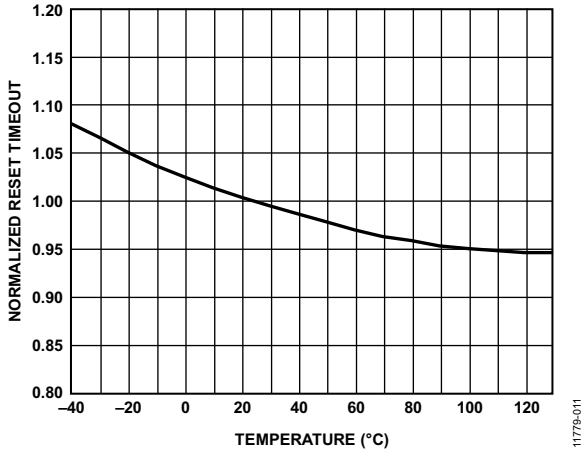

Figure 11. Normalized Reset Timeout vs. Temperature

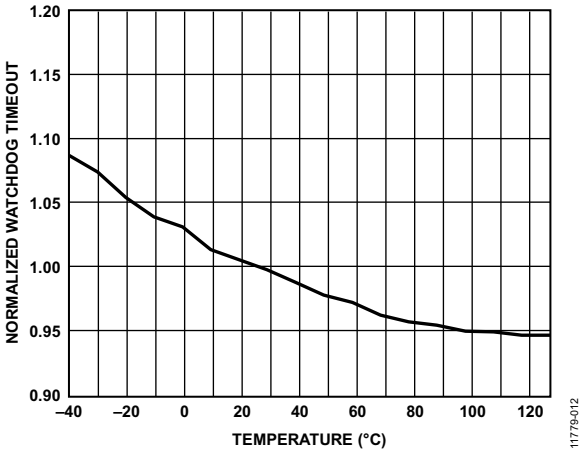

Figure 12. Normalized Watchdog Timeout vs. Temperature

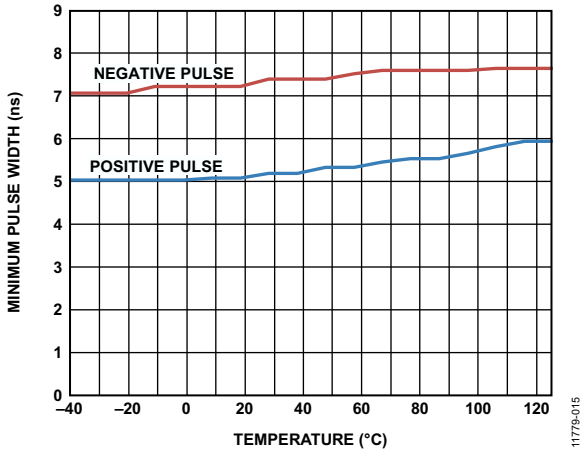

Figure 15. Watchdog Input Minimum Pulse Width vs. Temperature

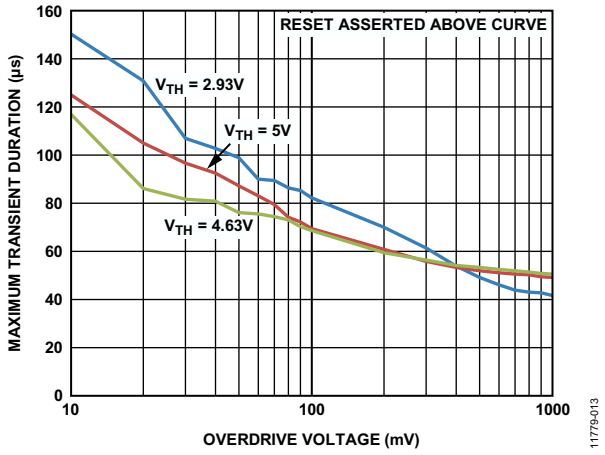

Figure 13. Maximum V_{CC} Transient Duration vs. $\overline{RESET}$ Threshold Overdrive

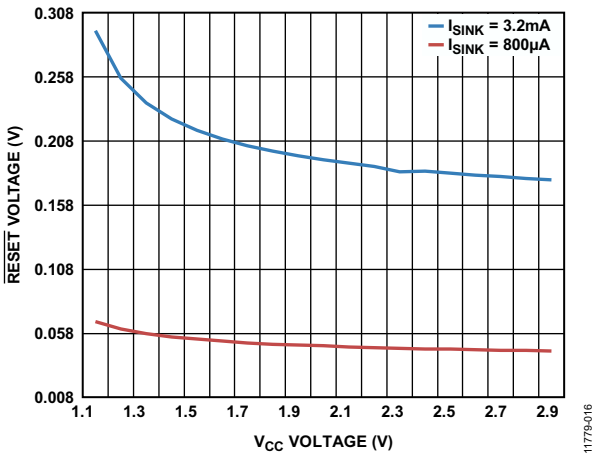

Figure 16. $\overline{RESET}$ Open-Drain V_{OL} Voltage vs. V_{CC} Voltage (V_{TH} = 3 V)

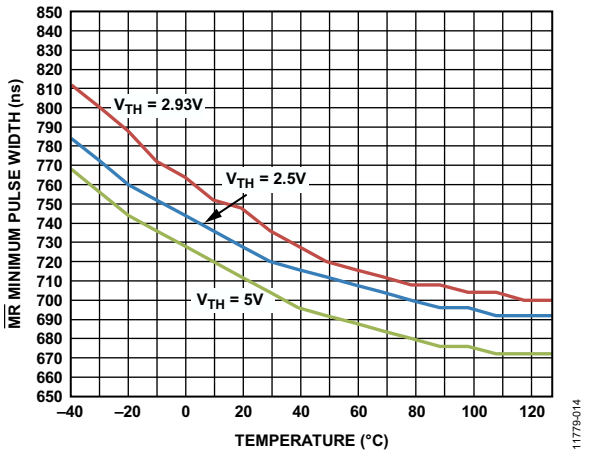

Figure 14. Manual Reset ($\overline{MR}$) Minimum Pulse Width vs. Temperature

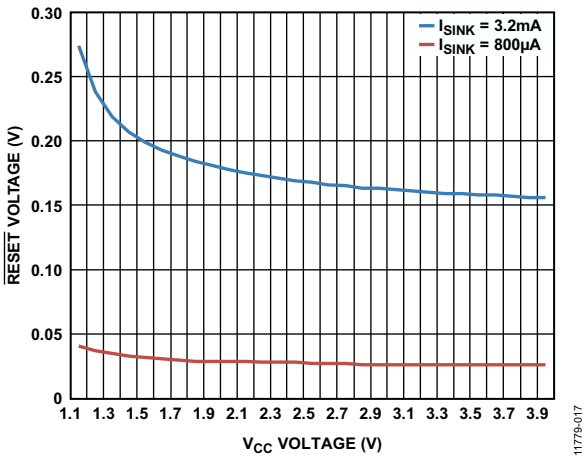

Figure 17. $\overline{RESET}$ Push-Pull V_{OL} Voltage vs. V_{CC} Voltage (V_{TH} = 4 V)

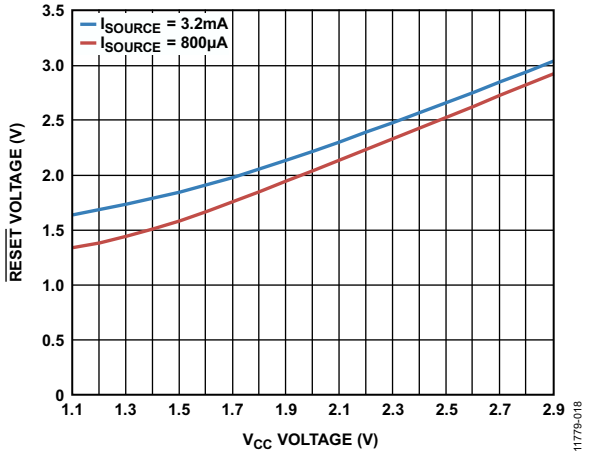

Figure 18. $\overline{RESET}$ Push-Pull V_{OH} Voltage vs. V_{CC} Voltage (V_{TH} = 3 V)

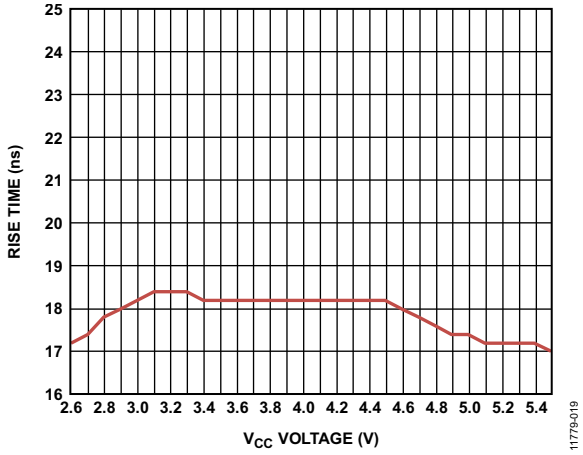

Figure 19. $\overline{RESET}$ Push-Pull Rise Time vs. V_{CC} Voltage

THEORY OF OPERATION

CIRCUIT DESCRIPTION

The ADM8316/ADM8318/ADM8319/ADM8320/ADM8321/ADM8322 provide microprocessor supply voltage supervision by controlling the microprocessor reset input. Code execution errors are avoided during power-up, power-down, and brownout conditions by asserting a reset signal when the supply voltage is below a preset threshold and by allowing supply voltage stabilization with a fixed timeout reset delay after the supply voltage rises above the threshold. In addition, problems with microprocessor code execution can be monitored and corrected with a watchdog timer (ADM8316/ADM8318/ADM8320/ADM8321). If the user detects a problem with system operation, a manual reset input is available (ADM8316/ADM8319/ADM8320/ADM8322) to reset the microprocessor, for example, by means of an external push-button switch.

PUSH-PULL RESET OUTPUT

The ADM8316 features an active low push-pull reset output, whereas the ADM8321/ADM8322 have active high push-pull reset outputs. The ADM8318/ADM8319 feature dual active low and active high push-pull reset outputs. For active low and active high outputs, the reset signal is guaranteed to be valid for V_{CC} down to 0.9 V.

The reset output is asserted when V_{CC} is below the reset threshold (V_{TH}), when $\overline{MR}$ is driven low, or when WDI is not serviced within the watchdog timeout period (t_{WD}). The reset output remains asserted for the duration of the reset active timeout period (t_{RP}) after V_{CC} rises above the reset threshold, after $\overline{MR}$ transitions from low to high, or after the watchdog timer times out. Figure 20 illustrates the behavior of the reset outputs.

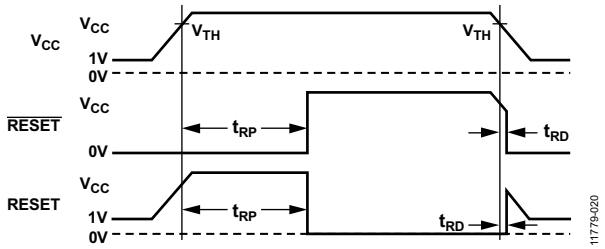

Figure 20. Reset Timing Diagram

OPEN-DRAIN $\overline{RESET}$ OUTPUT

The ADM8320/ADM8321/ADM8322 have an active low, open-drain reset output. This output structure requires an external pull-up resistor to connect the reset output to a voltage rail no higher than V_{CC}. A resistor that complies with the logic low and logic high voltage level requirements of the microprocessor while supplying input current and leakage paths on the $\overline{RESET}$ line is recommended. A 10 kΩ resistor is adequate in most situations.

MANUAL RESET INPUT

The ADM8316/ADM8319/ADM8320/ADM8322 feature a manual reset input ($\overline{MR}$), which when driven low, asserts the reset output. When $\overline{MR}$ transitions from low to high, the reset remains asserted for the duration of the reset active timeout period before deasserting. The $\overline{MR}$ input has a 75 kΩ, internal pull-up resistor so that the input is always high when unconnected. An external push-button switch can be connected between $\overline{MR}$ and ground so that the user can generate a reset. Debounce circuitry for this purpose is integrated on chip. Noise immunity is provided on the $\overline{MR}$ input, and fast, negative going transients of up to 100 ns (typical) are ignored. A 0.1 µF capacitor between $\overline{MR}$ and ground provides additional noise immunity.

WATCHDOG INPUT

The ADM8316/ADM8318/ADM8320/ADM8321 feature a watchdog timer that monitors microprocessor activity. A timer circuit is cleared with every low-to-high or high-to-low logic transition on the watchdog input pin (WDI), which detects pulses as short as 50 ns. If the timer counts through the preset watchdog timeout period (t_{WD}), a reset is asserted. The microprocessor is required to toggle the WDI pin to avoid asserting the reset pin. Failure of the microprocessor to toggle WDI within the timeout period, therefore, indicates a code execution error, and the reset pulse generated restarts the microprocessor in a known state.

As well as logic transitions on WDI, the watchdog timer is also cleared by a reset assertion due to an undervoltage condition on V_{CC} or due to $\overline{MR}$ being pulled low. When a reset asserts, the watchdog timer clears and does not begin counting again until the reset deassserts. The watchdog timer can be disabled by leaving WDI floating or by tristating the WDI driver.

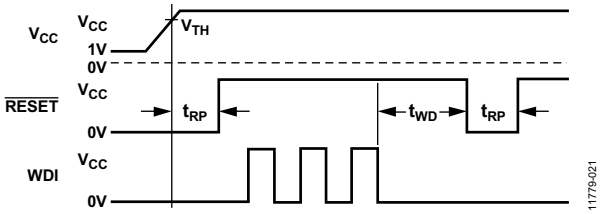

Figure 21. Watchdog Timing Diagram

APPLICATIONS INFORMATION

WATCHDOG INPUT CURRENT

To minimize the watchdog input current, leave WDI low for the majority of the watchdog timeout period. When driven high, WDI can draw as much as 100 µA. Pulsing WDI low to high to low at a low duty cycle reduces the effect of the large input current. When WDI is unconnected, a window comparator disconnects the watchdog timer from the reset output circuitry so that a reset is not asserted when the watchdog timer times out.

NEGATIVE GOING V_{CC} TRANSIENTS

To avoid unnecessary resets caused by fast power supply transients, the ADM8316/ADM8318/ADM8319/ADM8320/ADM8321/ADM8322 are equipped with glitch rejection circuitry. The typical performance characteristic in Figure 13 plots V_{CC} transient duration vs. reset threshold overdrive. The curves show combinations of reset threshold overdrive and duration for which a reset is not generated for 5 V, 4.63 V, and 2.93 V reset threshold devices. For example, with the 2.93 V threshold, a transient that goes 100 mV below the threshold and lasts 80 µs typically does not cause a reset, but if the transient is any larger in reset threshold overdrive or duration, a reset generates. An optional 0.1 µF bypass capacitor mounted near V_{CC} provides additional glitch rejection.

ENSURING RESET VALID TO V_{CC} = 0 V

Both active low and active high reset outputs are guaranteed to be valid for V_{CC} as low as 0.9 V. However, by using an external resistor with push-pull configured reset outputs, valid outputs for V_{CC} as low as 0 V are possible. For an active low reset output, a resistor connected between $\overline{\text{RESET}}$ and ground pulls the output low when it is unable to sink current. For an active high reset output, a resistor connected between RESET and V_{CC} pulls the output high when it is unable to source current. Use a large resistance, such as 100 kΩ, so that it does not overload the reset output when V_{CC} is greater than 0.9 V.

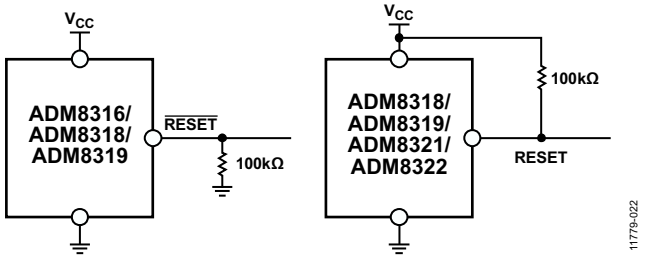

Figure 22. Ensuring Reset Valid to V_{CC} = 0 V

WATCHDOG SOFTWARE CONSIDERATIONS

In implementing the microprocessor watchdog strobe code, quickly switching WDI low to high and then high to low (minimizing WDI high time) is desirable for current consumption reasons. However, a more effective way of using the watchdog function can be considered.

A low to high to low WDI pulse within a given subroutine prevents the watchdog from timing out. However, if the subroutine becomes stuck in an infinite loop, the watchdog cannot detect this because the subroutine continues to toggle WDI. A more effective coding scheme for detecting this error involves using a slightly longer watchdog timeout. In the program that calls the subroutine, WDI is set high. The subroutine sets WDI low when it is called. If the program executes without error, WDI is toggled high and low with every loop of the program. If the subroutine enters an infinite loop, WDI is kept low, the watchdog times out, and the microprocessor is reset (see Figure 23).

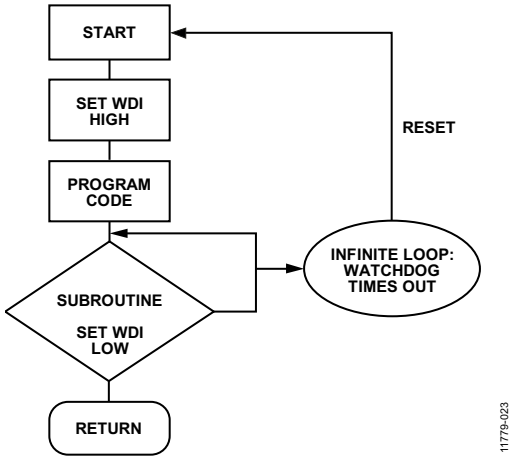

Figure 23. Watchdog Flow Diagram

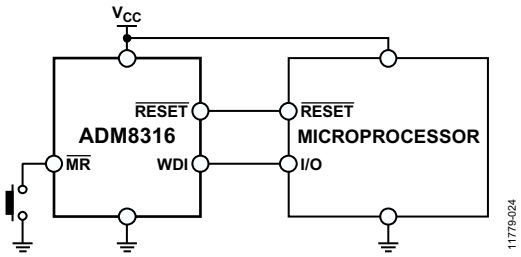

Figure 24. Typical Application Circuit

OPTIONS

Table 6. Selection Table

Device No.	Watchdog	Manual Reset	Output Stage	
			$\overline{\text{RESET}}$	RESET
ADM8316	Yes	Yes	Push-pull	No
ADM8318	Yes	No	Push-pull	Push-pull
ADM8319	No	Yes	Push-pull	Push-pull
ADM8320	Yes	Yes	Open-drain	No
ADM8321	Yes	No	Open-drain	Push-pull
ADM8322	No	Yes	Open-drain	Push-pull

Table 7. Reset Timeout Options

Suffix	Minimum	Typical	Maximum	Unit
A	1	1.4	1.8	ms
B	20	28	36	ms
C	140	200	260	ms
D	1120	1600	2080	ms

Table 8. Watchdog Timeout Options

Suffix	Minimum	Typical	Maximum	Unit
W	4.5	6.3	8.1	ms
X	72	102	132	ms
Y	1.12	1.6	2.24	sec
Z	18.0	25.6	33.2	sec

Table 9. Reset Voltage Threshold Options

Reset Threshold Number	T_A = 25°C			T_A = −40°C to +125°C		Unit
	Minimum	Typical	Maximum	Minimum	Maximum	
50	4.950	5.000	5.050	4.925	5.075	V
49	4.851	4.900	4.949	4.826	4.974	V
48	4.752	4.800	4.848	4.728	4.872	V
47	4.653	4.700	4.747	4.629	4.771	V
46	4.584	4.630	4.676	4.560	4.700	V
45	4.455	4.500	4.545	4.432	4.568	V
44	4.346	4.390	4.434	4.324	4.456	V
43	4.257	4.300	4.343	4.235	4.365	V
42	4.158	4.200	4.242	4.137	4.263	V
41	4.059	4.100	4.141	4.038	4.162	V
40	3.960	4.00	4.040	3.940	4.060	V
39	3.861	3.900	3.939	3.841	3.959	V
38	3.762	3.800	3.838	3.743	3.857	V
37	3.663	3.700	3.737	3.644	3.756	V
36	3.564	3.600	3.636	3.546	3.654	V
35	3.465	3.500	3.535	3.447	3.553	V
34	3.366	3.400	3.434	3.349	3.451	V
33	3.267	3.300	3.333	3.250	3.350	V
32	3.168	3.200	3.232	3.152	3.248	V
31	3.049	3.080	3.111	3.033	3.127	V
30	2.970	3.000	3.030	2.955	3.045	V
29	2.901	2.930	2.959	2.886	2.974	V
28	2.772	2.800	2.828	2.758	2.842	V
27	2.673	2.700	2.727	2.659	2.741	V
26	2.604	2.630	2.656	2.590	2.670	V
25	2.475	2.500	2.525	2.462	2.538	V

Table 10. Standard Models

Model	Reset Threshold (V)	Minimum Reset Timeout (ms)	Typical Watchdog Timeout (sec)
ADM8316WBX30ARJZR7	3	20	0.102
ADM8316WBX46ARJZR7	4.63	20	0.102
ADM8318WCY46ARJZR7	4.63	140	1.6
ADM8319WB31ARJZR7	3.08	20	Not applicable
ADM8320WCY29ARJZR7	2.93	140	1.6
ADM8321WAY30ARJZR7	3	1	1.6
ADM8321WCY46ARJZR7	4.63	140	1.6
ADM8322WC46ARJZR7	4.63	140	Not applicable

OUTLINE DIMENSIONS

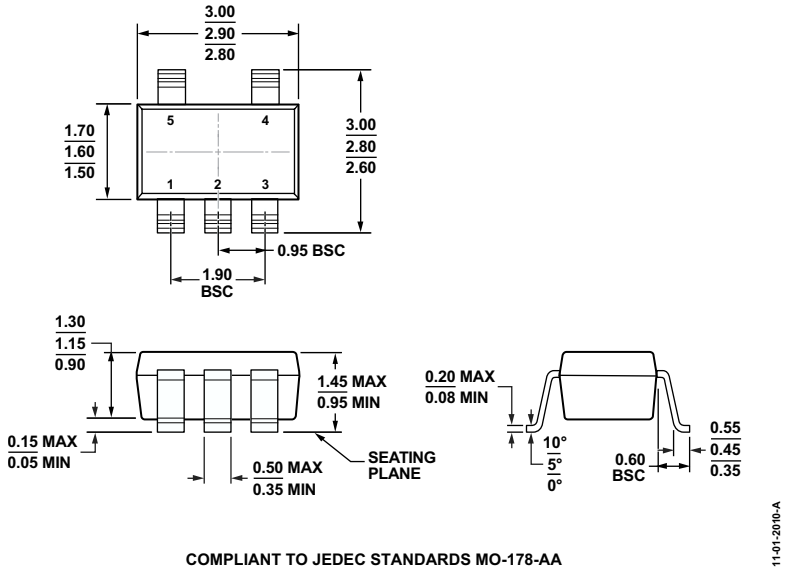

Figure 25. 5-Lead Small Outline Transistor Package [SOT-23]
(RJ-5)
Dimensions shown in millimeters

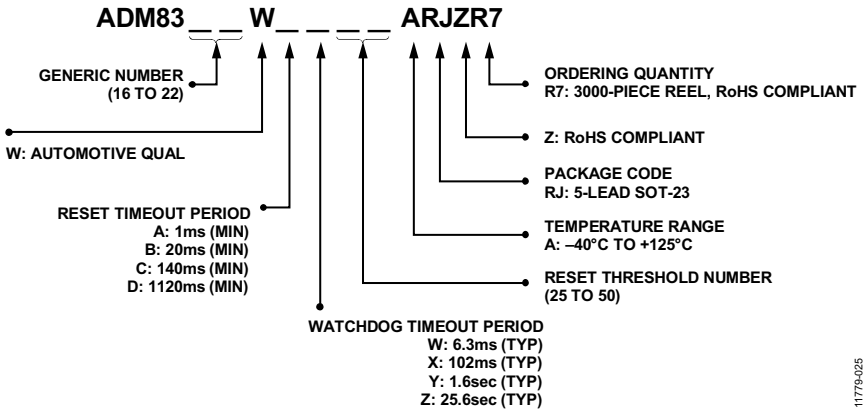

Figure 26. Ordering Code Structure

ORDERING GUIDE

Model[1, 2, 3, 4]	Temperature Range	Ordering Quantity[5]	Package Description	Package Option	Branding
ADM8316WxxxxARJZR7	−40°C to +125°C	3,000	5-Lead SOT-23	RJ-5	LMT
ADM8318WxxxxARJZR7	−40°C to +125°C	3,000	5-Lead SOT-23	RJ-5	LMW
ADM8319WxxxARJZR7	−40°C to +125°C	3,000	5-Lead SOT-23	RJ-5	LMV
ADM8320WxxxxARJZR7	−40°C to +125°C	3,000	5-Lead SOT-23	RJ-5	LMX
ADM8321WxxxxARJZR7	−40°C to +125°C	3,000	5-Lead SOT-23	RJ-5	LMY
ADM8322WxxxARJZR7	−40°C to +125°C	3,000	5-Lead SOT-23	RJ-5	LMZ

[1] Complete the ordering code by inserting the reset timeout, watchdog timeout, and reset threshold (ADM8316/ADM8318/ADM8320/ADM8321) suffixes from Table 7 to Table 9. No watchdog timeout is available for ADM8319/ADM8322.
[2] Contact sales for the availability of nonstandard models. See Table 10 for a list of standard models.
[3] Z = RoHS Compliant Part.
[4] W = Qualified for Automotive Applications.
[5] A minimum of 12,000 (four reels) must be ordered for nonstandard models.

AUTOMOTIVE PRODUCTS

The ADM8316W/ADM8318W/ADM8319W/ADM8320W/ADM8321W/ADM8322W models are available with controlled manufacturing to support the quality and reliability requirements of automotive applications. Note that these automotive models may have specifications that differ from the commercial models; therefore, designers should review the Specifications section of this data sheet carefully. Only the automotive grade products shown are available for use in automotive applications. Contact your local Analog Devices account representative for specific product ordering information and to obtain the specific Automotive Reliability reports for these models.

NOTES

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