

December 1996

## Fast CMOS Multilevel Pipeline Register

### Features

- Advanced 0.8 micron CMOS Technology
- These Devices are Pinout and Function Compatible with IDT29FCT520, QS29FCT520 and AMD's Am29520
- Four 8-bit High-Speed Registers
- Hold, Transfer, and Load Instructions
- Dual Two-Level or Single Four-Level Pipeline Operation
- TTL Input and Output Levels, Reducing Problematic Ground Bounce
- High Output Drive .....  $I_{OL} = 48\text{mA}$
- Extremely Low Static Power .....  $1\text{mW}$  (Typ)

### Description

These devices are multilevel pipeline registers containing four 8-bit positive triggered registers which can be configured as a dual 2-level or a single 4-level pipeline. These products are designed for use as temporary storage or for storage delays in pipelined systems. When data is entered into the first level ( $l = 2$  or  $l = 1$ ) of the CD29FCT520T, the existing data in the first level is moved to the second level. The  $l = 3$  shift instruction puts the registers on hold.

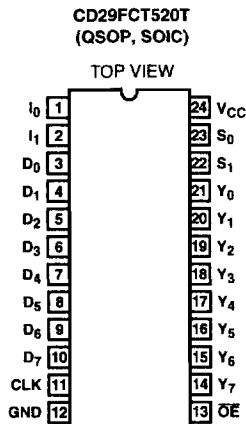
### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
CD29FCT520ATM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT520ATQM	-40 to 85	24 Ld QSOP	M24.15-P
CD29FCT520BTM	-40 to 85	24 Ld SOIC	M24.3-P
CD29FCT520BTQM	-40 to 85	24 Ld QSOP	M24.15-P

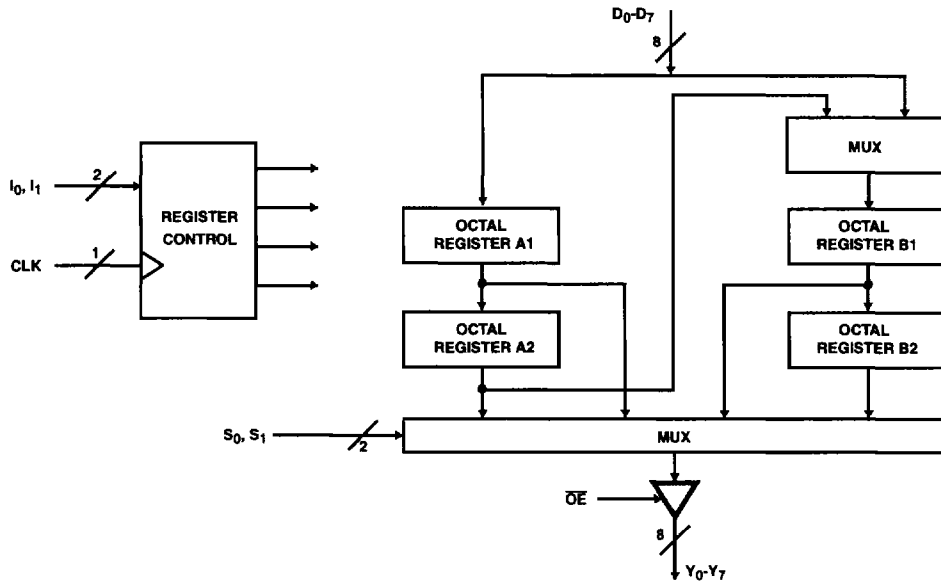
NOTE: QSOP is commonly known as SSOP.

When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.

### Pinout



**Functional Block Diagram**



**Register Selection**

S1	S0	REGISTER
0	0	B <sub>2</sub>
0	1	B <sub>1</sub>
1	0	A <sub>2</sub>
1	1	A <sub>1</sub>

**Pin Descriptions**

PIN NAME	DESCRIPTION
$\overline{OE}$	Output Enable Input (Active LOW) for Three-State Output Port
CLK	Clock Input. Enter Data into Registers on LOW-to-HIGH Transitions
I <sub>0</sub> , I <sub>1</sub>	Instruction Inputs
S <sub>0</sub> , S <sub>1</sub>	Multiplexer Select. Inputs Either Register A <sub>1</sub> , A <sub>2</sub> , B <sub>1</sub> , or B <sub>2</sub> Data to be Available at the Output Ports
D <sub>X</sub>	Register Inputs
Y <sub>X</sub>	Register Outputs
GND	Ground
VCC	Power

**CD29FCT520T Data Loading** (Note 1)

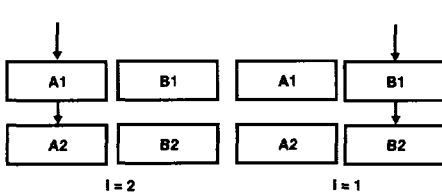


FIGURE 1. DUAL 2-LEVEL

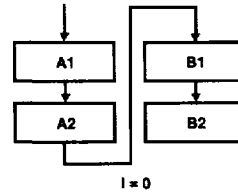


FIGURE 2. SINGLE 4-LEVEL

NOTE: I = 3 for hold.

# CD29FCT520T

## Absolute Maximum Ratings

DC Input Voltage	-0.5V to 7.0V
DC Output Current	120mA

## Operating Conditions

Operating Temperature Range	-40°C to 85°C
Supply Voltage to Ground Potential	
Inputs and V <sub>CC</sub> Only	-0.5V to 7.0V
Supply Voltage to Ground Potential	
Outputs and D/O Only	-0.5V to 7.0V

## Thermal Information

Thermal Resistance (Typical, Note 1)	$\theta_{JA}$ (°C/W)
SOIC Package	75
QSOP Package	100
Maximum Junction Temperature	150°C
Maximum Storage Temperature Range	-65°C to 150°C
Maximum Lead Temperature (Soldering 10s)	300°C (Lead Tips Only)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## Electrical Specifications

PARAMETER	SYMBOL	(NOTE 3) TEST CONDITIONS	MIN	(NOTE 4) TYP	MAX	UNITS	
<b>DC ELECTRICAL SPECIFICATIONS</b> Over the Operating Range, $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$ , $V_{CC} = 5.0\text{V} \pm 5\%$							
Output HIGH Voltage	$V_{OH}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -15.0\text{mA}$	2.4	3.0	V	
Output LOW Voltage	$V_{OL}$	$V_{CC} = \text{Min}$ , $V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 48\text{mA}$	-	0.3	V	
Input HIGH Voltage	$V_{IH}$	Guaranteed Logic HIGH Level		2.0	-	V	
Input LOW Voltage	$V_{IL}$	Guaranteed Logic LOW Level		-	0.8	V	
Input HIGH Current	$I_{IH}$	$V_{CC} = \text{Max}$	$V_{IN} = V_{CC}$	-	1	$\mu\text{A}$	
Input LOW Current	$I_{IL}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$	-	-1	$\mu\text{A}$	
High Impedance Output Current	$I_{OZH}$	$V_{CC} = \text{Max}$	$V_{OUT} = 2.7\text{V}$	-	1	$\mu\text{A}$	
	$I_{OZL}$		$V_{OUT} = 0.5\text{V}$	-	-1	$\mu\text{A}$	
Clamp Diode Voltage	$V_{IK}$	$V_{CC} = \text{Min}$ , $I_{IN} = -18\text{mA}$		-	-0.7	V	
Short Circuit Current	$I_{OS}$	$V_{CC} = \text{Max}$ (Note 5), $V_{OUT} = \text{GND}$		-60	-120	mA	
Power Down Disable	$I_{OFF}$	$V_{CC} = \text{GND}$ , $V_{OUT} = 4.5\text{V}$		-	100	$\mu\text{A}$	
Input Hysteresis	$V_H$			-	200	mV	
<b>CAPACITANCE</b> $T_A = 25^\circ\text{C}$ , $f = 1\text{MHz}$							
Input Capacitance (Note 6)	$C_{IN}$	$V_{IN} = 0\text{V}$		-	6	pF	
Output Capacitance (Note 6)	$C_{OUT}$	$V_{OUT} = 0\text{V}$		-	8	pF	
<b>POWER SUPPLY SPECIFICATIONS</b>							
Quiescent Power Supply Current	$I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = \text{GND}$ or $V_{CC}$	-	0.1	10	$\mu\text{A}$
Supply Current per Input at TTL HIGH	$\Delta I_{CC}$	$V_{CC} = \text{Max}$	$V_{IN} = 3.4\text{V}$ (Note 7)	-	0.5	2.0	mA
Supply Current per Input per MHz (Note 8)	$I_{CCD}$	$V_{CC} = \text{Max}$ , Outputs Open $\overline{OE} = \text{GND}$ One Input Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	0.15	0.25	mA/MHz
Total Power Supply Current (Note 10)	$I_C$	$V_{CC} = \text{Max}$ , Outputs Open $f_{cp} = 10\text{MHz}$ , 50% Duty Cycle $\overline{OE} = \text{GND}$ One Bit Toggling $f_1 = 5\text{MHz}$ , 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	1.5	3.5 (Note 9)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	2.0	5.5 (Note 9)	mA
		$V_{CC} = \text{Max}$ , Outputs Open $f_{cp} = 10\text{MHz}$ , 50% Duty Cycle $\overline{OE} = \text{GND}$ Eight Bits Toggling $f_1 = 5\text{MHz}$ , 50% Duty Cycle	$V_{IN} = V_{CC}$ $V_{IN} = \text{GND}$	-	3.8	7.3 (Note 9)	mA
			$V_{IN} = 3.4\text{V}$ $V_{IN} = \text{GND}$	-	6.0	16.3 (Note 9)	mA

4

OCTAL 5V FCT  
5V FCT 25Ω

## CD29FCT520T

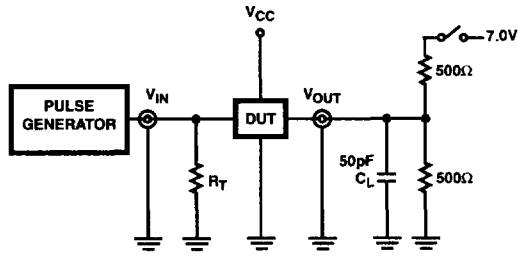
### Switching Specifications Over Operating Range

PARAMETER	SYMBOL	(NOTE 11) TEST CONDITIONS	AT		BT		UNITS
			(NOTE 12) MIN	MAX	(NOTE 12) MIN	MAX	
Propagation Delay CLK to Y <sub>X</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50 pF R <sub>L</sub> = 500Ω	2.0	14.0	2.0	7.5	ns
Propagation Delay S <sub>0</sub> or S <sub>1</sub> to Y <sub>X</sub>	t <sub>PLH</sub> , t <sub>PHL</sub>		2.0	13.0	2.0	7.5	ns
Setup Time HIGH or LOW D <sub>X</sub> to CLK	t <sub>SU</sub>		5.0	-	2.5	-	ns
Hold Time HIGH or LOW D <sub>X</sub> to CLK	t <sub>H</sub>		2.0	-	2.0	-	ns
Setup Time HIGH or LOW I <sub>0</sub> or I <sub>1</sub> to CLK	t <sub>SU</sub>		5.0	-	4.0	-	ns
Hold Time HIGH or LOW I <sub>0</sub> or I <sub>1</sub> to CLK	t <sub>H</sub>		2.0	-	2.0	-	ns
Output Enable Time OE to Y <sub>X</sub>	t <sub>PZH</sub> , t <sub>PZL</sub>		1.5	12.0	1.5	7.0	ns
Output Disable Time OE to Y <sub>X</sub> (Note 13)	t <sub>PHZ</sub> , t <sub>PLZ</sub>		1.5	15.0	1.5	7.5	ns
Clock Pulse Width HIGH or LOW (Note 13)	t <sub>W</sub>		7.0	-	5.5	-	ns

**NOTES:**

2. For conditions shown as Max or Min, use appropriate value specified under Electrical Specifications for the applicable device type.
3. Typical values are at V<sub>CC</sub> = 5.0V, 25°C ambient and maximum loading.
4. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
5. This parameter is determined by device characterization but is not production tested.
6. Per TTL driven input (V<sub>IN</sub> = 3.4V, control inputs only); all other inputs at V<sub>CC</sub> or GND.
7. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
8. Values for these conditions are examples of the I<sub>CC</sub> formula. These limits are guaranteed but not tested.
9. I<sub>C</sub> = I<sub>QUIESCENT</sub> + I<sub>INPUTS</sub> + I<sub>DYNAMIC</sub>  
 $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (t_{CP}/2 + f_i N_i)$   
 I<sub>CC</sub> = Quiescent Current  
 ΔI<sub>CC</sub> = Power Supply Current for a TTL High Input (V<sub>IN</sub> = 3.4V)  
 D<sub>H</sub> = Duty Cycle for TTL Inputs High  
 N<sub>T</sub> = Number of TTL Inputs at D<sub>H</sub>  
 I<sub>CCD</sub> = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)  
 f<sub>CP</sub> = Clock Frequency for Register Devices (Zero for Non-Register Devices)  
 f<sub>i</sub> = Input Frequency  
 N<sub>i</sub> = Number of Inputs at f<sub>i</sub>  
 All currents are in milliamps and all frequencies are in megahertz.
10. See test circuit and wave forms.
11. Minimum limits are guaranteed but not tested on Propagation Delays.
12. This parameter is guaranteed but not production tested.

Test Circuits and Waveforms



NOTE:

13. Pulse Generator for All Pulses: Rate  $\leq$  1.0MHz;  $Z_{OUT} \leq 50\Omega$ ;  
 $t_r, t_f \leq 2.5ns$ .

FIGURE 3. TEST CIRCUIT

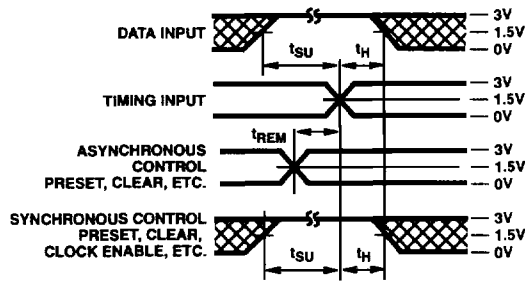


FIGURE 4. SETUP, HOLD, AND RELEASE TIMING

SWITCH POSITION	
TEST	SWITCH
$t_{PLZ}, t_{PZL}$	Closed
$t_{PHZ}, t_{PZH}, t_{PLH}, t_{PHL}$	Open

DEFINITIONS:

$C_L$  = Load capacitance, includes jig and probe capacitance.

$R_T$  = Termination resistance, should be equal to  $Z_{OUT}$  of the Pulse Generator.

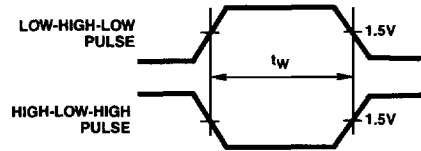


FIGURE 5. PULSE WIDTH

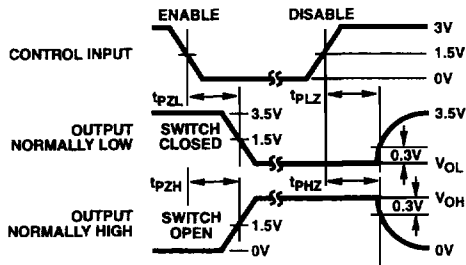


FIGURE 6. ENABLE AND DISABLE TIMING

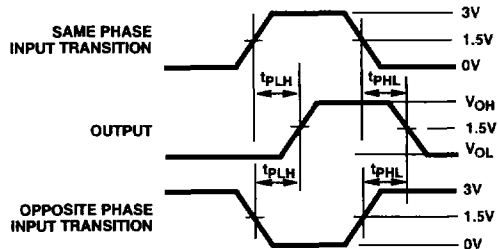


FIGURE 7. PROPAGATION DELAY