Data Sheet | May 9, 2008 | FN6570.0

8-Channel LED Driver

The ISL97636 is an integrated power LED driver that controls 8 channels of LED current for LCD backlight applications. The ISL97636 is capable of driving typically 72 (8x9) pieces of 3.5V/30mA or 80 (8x10) pieces of 3.2V/20mA LEDs. The ISL97636's contains 8 channels of voltage controlled current sources with typical currents matching of ±1%, which compensate for the non-uniformity effect of forward voltages variance in the LED stacks. To minimize the voltage headroom and power loss in the typical multi-strings operation, the ISL97636 features a dynamic headroom control that monitors the highest LED forward voltage string and uses its feedback signal for output regulation.

The LED brightness can be pulse width modulated with an applied PWM signal from DC to audio noise free 20kHz.

The ISL97636 features extensive protection functions that include string open and short circuit detections, OVP, OTP, thermal shutdown and an optional input overcurrent protection with master fault disconnect switch.

Available in the 24 Ld 4mmx4mm QFN, the ISL97636 operates from -40°C to +85°C with input voltage ranges from 6V to 24V for high LEDs count applications.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-Free)	PKG. DWG. #
ISL97636IRZ*	976 36IRZ	24 Ld 4x4 QFN	L24.4x4D

*Add "-T" or "-TK" suffix for tape and reel. Please refer to TB347 for details on reel specifications

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

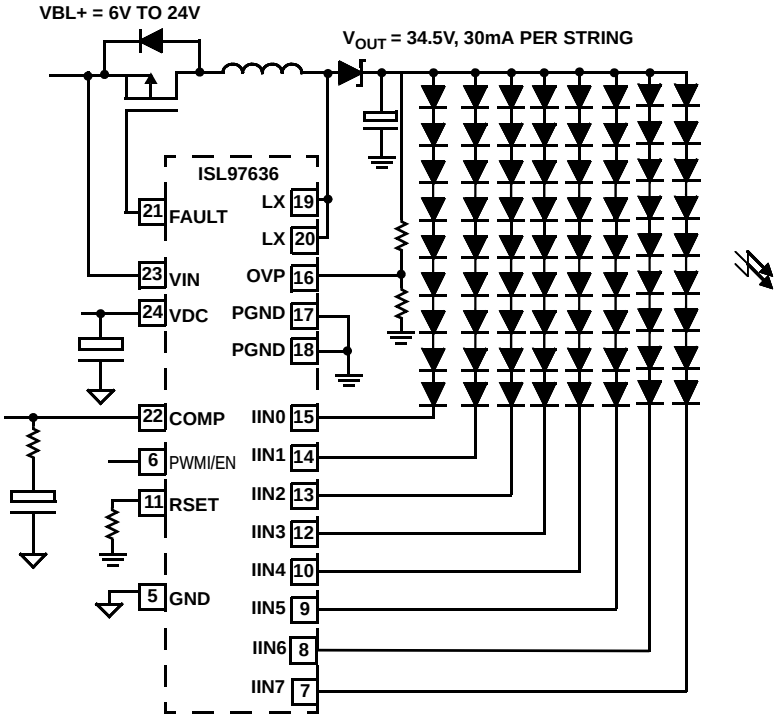
Features

- 8 Channels
- 6V to 24V Input
- 34.5V Output Max
- Drive Maximally 72 (3.5V/30mA each) or 80 (3.2V/20mA each) LEDs
- Current Matching ±1% Typ
- Dynamic Headroom Control
- PWM Signal up to 20kHz Dimming
- Protections
  - String Open Circuit Detection
  - String Short Circuit Detection with Selectable Thresholds
  - Over-Temperature Protection
  - Overvoltage Protection
  - Optional Input Overcurrent Protection w/Disconnect SW
- 1.2MHz Switching Frequency
- 24 Ld 4mmx4mm QFN Package
- Pb-Free (RoHS compliant)

Applications

- Notebook Displays LED Backlighting
- LCD Monitor LED Backlighting
- Automotive Displays LED Backlighting
- Automotive or Traffic Lighting

Typical Application Circuit



Block Diagram

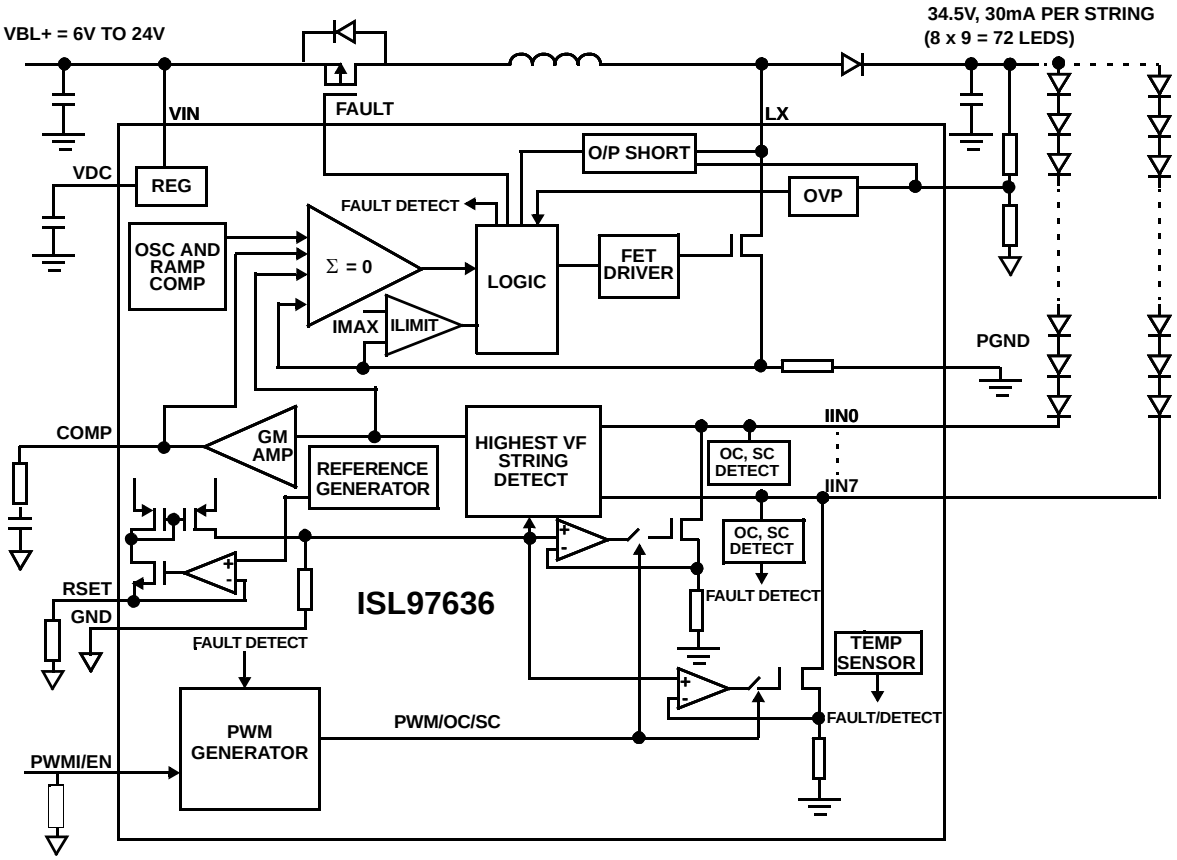


FIGURE 1. ISL97636 BLOCK DIAGRAM

Absolute Maximum Ratings (T_A = +25°C)

VIN, FAULT . . . . . -0.3V to 24V
VDC, COMP, RSET, EN/PWM . . . . . -0.3V to 6.5V
OVP, IIN0 - IIN7 . . . . . -0.3V to 28V
LX. . . . . -0.3V to 36V
PGND. . . . . -0.3V to +0.3V
Above voltage ratings are all with respect to GND pin

Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
24 Ld QFN	39	2

Thermal Characterization (Typical, Note 3)	PSI_{JT} (°C/W)
24 Ld QFN	~0.7

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside assumed under ideal case temperature.
3. PSI_{JT} is the junction-to-top thermal resistance. If the package top temperature can be measured, with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.
4. Limits established by characterization and are not production tested.

Electrical Specifications

All specifications below are tested at T_A = -40°C to +85°C; V_{IN} = 12V, EN = 5V, R_{SET} = 36.6kΩ; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
GENERAL						
VIN	Backlight Supply Voltage	≤ 9 LEDs per channel (3.5V/30mA type)	6		24	V
IVIN_STBY	VIN Shutdown Current				5	µA
V_{OUT}	Output Voltage				34.5	V
Vuvlo	Undervoltage Lockout Threshold		2.45		2.8	V
Vuvlo_hys	Undervoltage Lockout Hysteresis			300		mV
SS	Soft-start			1		ms
PWM GENERATOR						
EN/PWM	EN/PWM Voltage Range		2.7		5.5	V
ENmin	Minimum Enable Signal			40		µs
tMAX_PWM_OFF	Maximum PWMI Off Time Before Shutdown	EN/PWMI toggles		28		ms
REGULATOR						
VDC	LDO Output Voltage	V_{IN} > 6V	5.0		5.5	V
IVDC_STBY	Standby Current	EN/PWM = 0V			20	µA
IVDC	Active Current	EN/PWM = 5V		10		mA
VLDO	VDC LDO Dropout Voltage	V_{IN} > 5.5V, 30mA		30	200	mV
BOOST						
SWILimit	Boost FET Current Limit	T_A = +25°C	2.3		3.2	A
		T_A = -40°C, +85°C	2.2			A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance			130	260	mΩ

Electrical Specifications All specifications below are tested at T_A = -40°C to +85°C; V_{IN} = 12V, EN = 5V, R_{SET} = 36.6kΩ; Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. **(Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN	TYP	MAX	UNIT
Eff_peak	Peak Efficiency	VIN = 18V, 72 LEDs, 20mA each, L = 8.2µH with DCR 106mΩ, T_A = +25°C		91		%
		VIN = 12V, 72 LEDs, 20mA each, L = 8.2µH with DCR 106mΩ, T_A = +25°C		90		%
		VIN = 6V, 72 LEDs, 20mA each, L = 8.2µH with DCR 106mΩ, T_A = +25°C		86		%
$\Delta I_{OUT}/\Delta V_{IN}$	Line Regulation			0.1		%
Dmax	Boost Maximum Duty Cycle		82			%
Dmin	Boost Minimum Duty Cycle			7		%
f_S	Switching Frequency		1.0	1.2	1.3	MHz
ILX_leakage	LX Leakage Current	VLX = 36V, EN = 0			10	µA
REFERENCE						
Imatch	Channel-to-Channel Current Matching	I_{OUT} = 30mA	-3.5	±1	+3.5	%
I_{ACC}	Current Accuracy			±3		%
FAULT DETECTION						
VSC	Short Circuit Threshold	PWM Dimming = 100%	7.8	8	8.8	V
Vtemp_acc	Over-Temperature Threshold Accuracy			5		°C
VOVPlo	Overvoltage Limit on OVP Pin		1.17	1.2	1.23	V
OVPhys	OVP Hysteresis			20		mV
OVPfault	OVP Short Detection Fault Level			300		mV
CURRENT SOURCES						
$V_{headroom}$	Dominant Channel Current Source Headroom at IIN Pin	I_{LED} = 20mA T_A = +25°C		100		mV
V_{RSET}	Voltage at RSET Pin	R_{SET} = 36.6kΩ	680	700	720	mV
ILEDmax	Maximum LED Current Per Channel	R_{SET} = 20.9kΩ		35		mA
FAULT PIN						
Ifault	Fault Pull-down Current	V_{IN} = 12V	10	18	30	µA
Vfault	FAULT Clamp Voltage with Respect to V_{IN}	V_{IN} = 12, V_{IN} - Vfault		7.5		V
IlxStartup	LX Start-up Current	VDC = 5.2V	1	2.7	7	mA

Typical Performance Curves

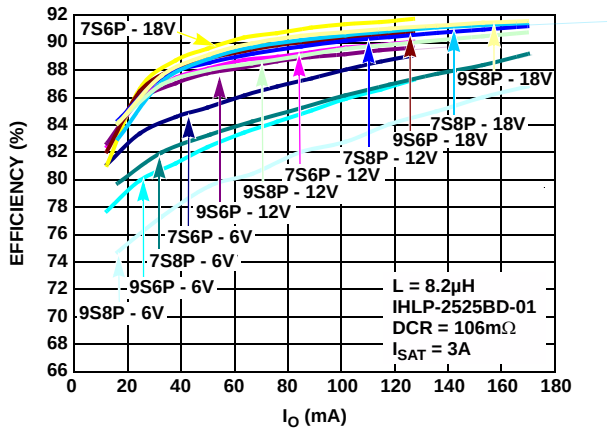


FIGURE 2. EFFICIENCY, L = 8.2µH WITH DCR = 106mΩ, C_O = 4x4.7µF/50V

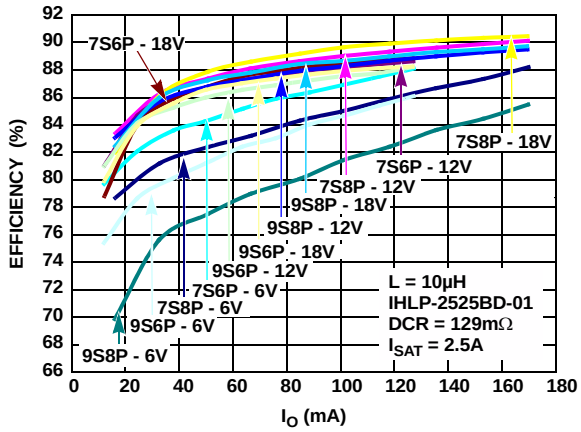


FIGURE 3. EFFICIENCY, L = 10µH WITH DCR = 129mΩ, C_O = 4x4.7µF/50V

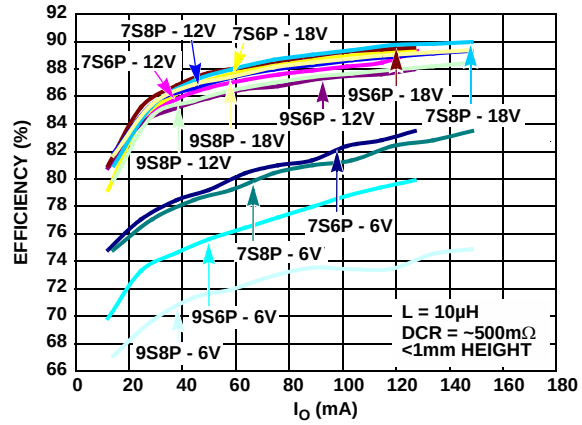


FIGURE 4. 3 EFFICIENCY, L = 10µH WITH DCR = 500mΩ, 1mm, C_O = 4x4.7µF/50V

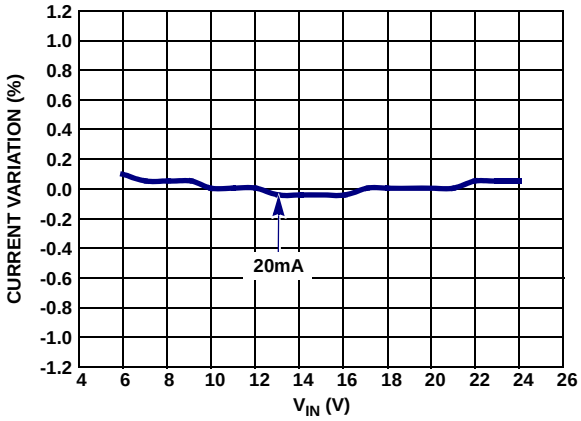


FIGURE 5. CURRENT REGULATION

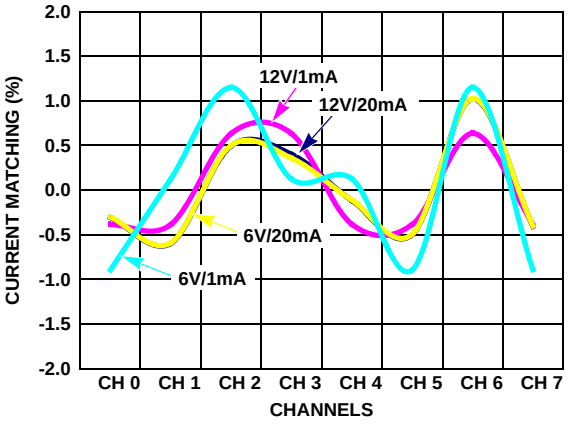


FIGURE 6. CHANNEL-TO-CHANNEL CURRENT MATCHING

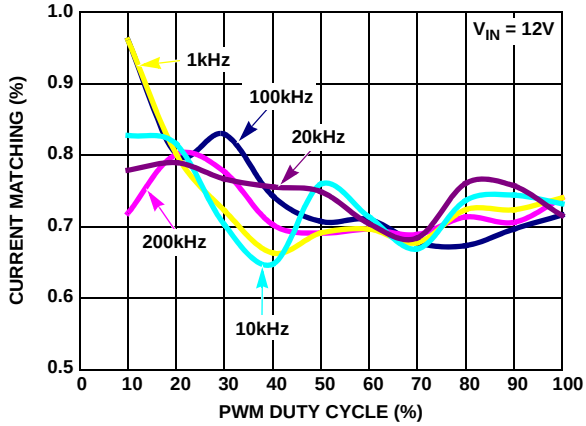


FIGURE 7. CURRENT MATCHING vs DUTY CYCLE vs DIMMING FREQUENCY

Typical Performance Curves (Continued)

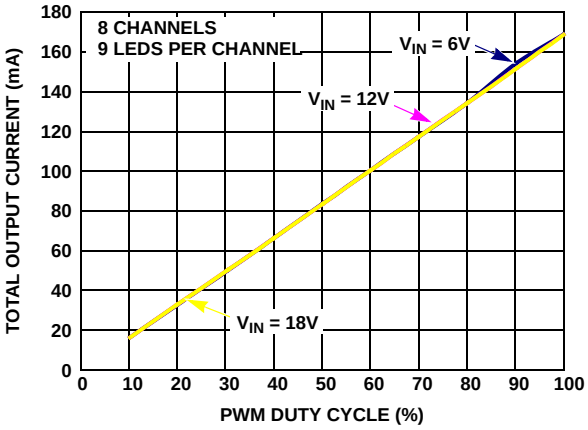


FIGURE 8. PWM DIMMING LINEARITY

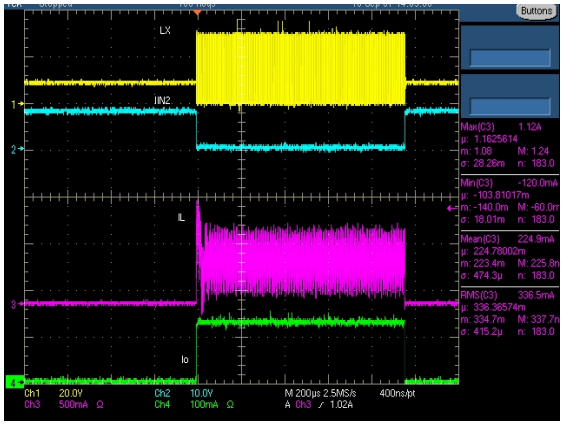


FIGURE 9. LX, VIIN, IL AND I_O AT PWM DIMMING (54 LEDS, 20mA, V_{IN} = 12V)

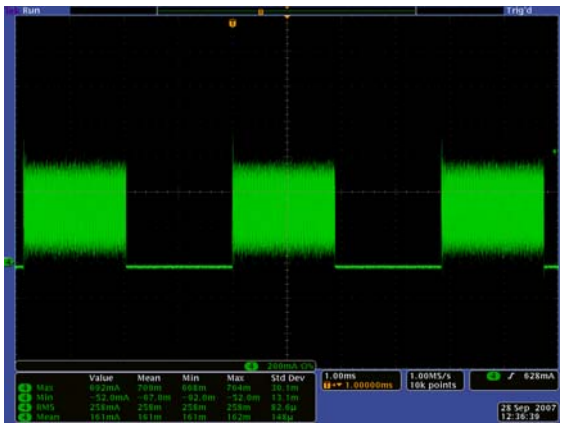


FIGURE 10. I_L AT 50% PWM DIMMING (54LEDs, 20mA, V_{IN} = 12V, L = 8.2µH)

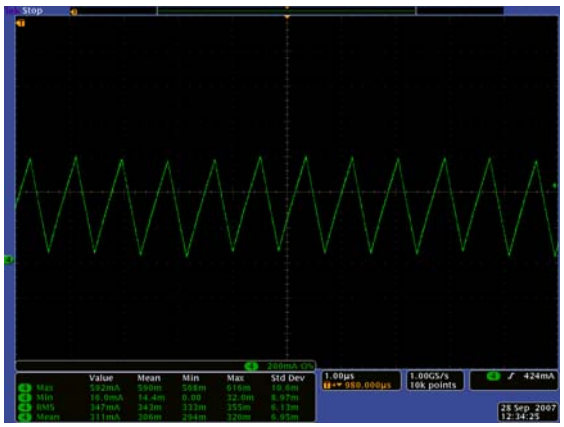


FIGURE 11. I_L ZOOM IN AT PWM DIMMING ZOOM IN (54 LEDs, 20mA, V_{IN} = 12V, L = 8.2µH)

FIGURE 12. I_{LED} AT 50% PWM DIMMING (54 LEDs, 20mA, V_{IN} = 12V)

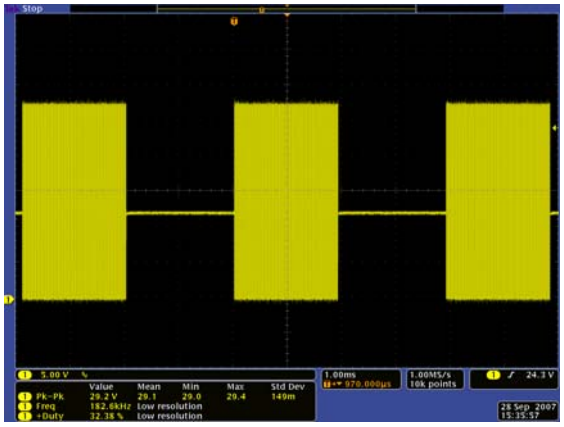


FIGURE 13. LX AT 50% PWM DIMMING (54 LEDs, 20mA, V_{IN} = 12V)

Typical Performance Curves (Continued)

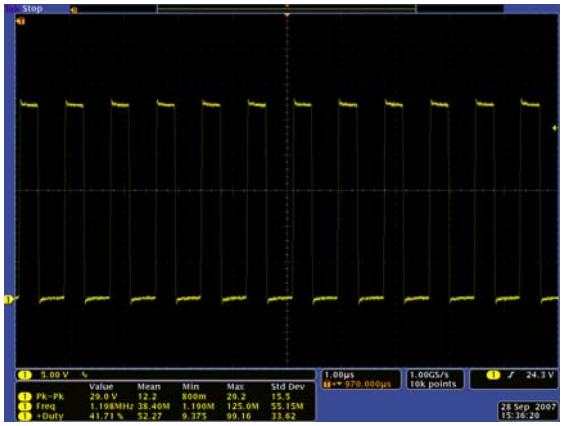


FIGURE 14. LX ZOOM IN AT 50% DIMMING (54 LEDs, 20mA, V_{IN} = 12V)

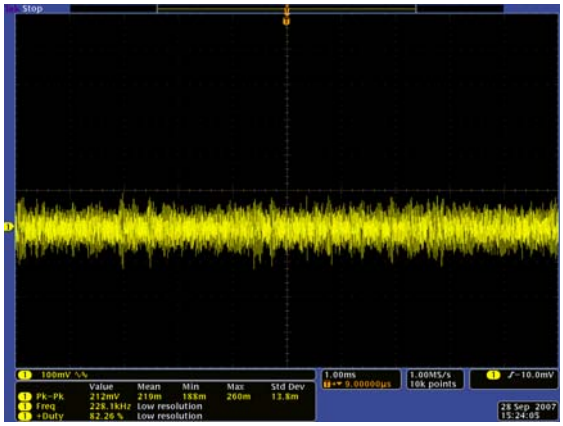


FIGURE 15. RIPPLE VOLTAGE (54 LEDs, V_{IN} = 12V, 20mA EACH, C_{OUT} = 4x4.7µF/50V)

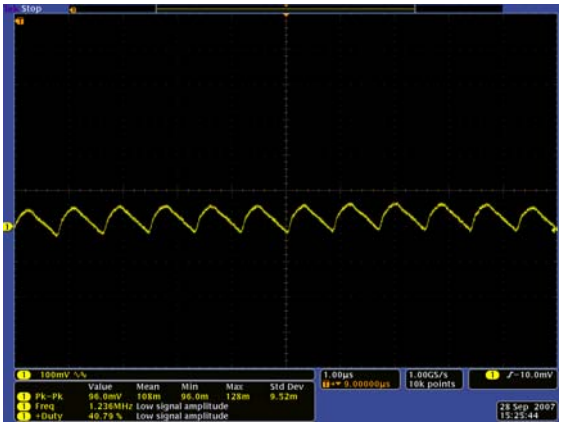
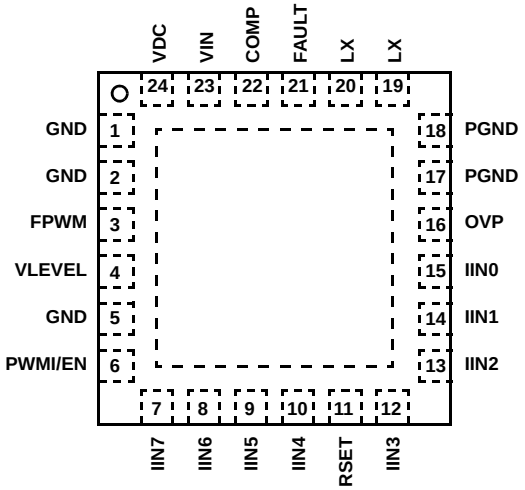


FIGURE 16. RIPPLE VOLTAGE ZOOM IN (54 LEDs, V_{IN} = 12V, 20mA EACH, C_{OUT} = 4x4.7µF/50V)

Pinout

ISL97636
(24 LD QFN)
TOP VIEW



Pin Descriptions (I = Input, O = Output, S = Supply)

PIN	NAME	TYPE	DESCRIPTION
1, 2	GND	S	Analog GND
3	FPWM	-	Not used. Leave floating and connect anything will have no effect on operation.
4	VLEVEL	-	Not used. Leave floating and connect anything will have no effect on operation.
5	GND	S	Analog GND and LED power return
6	EN/PWMI	I	Dual Functions: Enable Pin and PWM brightness control pin. DO NOT leave EN/PWMI floating. The device needs 40µs for initial power-up Enable, then this pin can be applied with a PWM signal with off time no longer than 28ms.
7	IIN7	I	Input 7 to current source, FB, and monitoring
8	IIN6	I	Input 6 to current source, FB, and monitoring
9	IIN5	I	Input 5 to current source, FB, and monitoring
10	IIN4	I	Input 4 to current source, FB, and monitoring
11	RSET	I	Resistor connection for setting LED current, (see Equation 1 for calculating the ILEDpeak)
12	IIN3	I	Input 3 to current source, FB, and monitoring
13	IIN2	I	Input 2 to current source, FB, and monitoring
14	IIN1	I	Input 1 to current source, FB, and monitoring
15	IIN0	I	Input 0 to current source, FB, and monitoring
16	OVP	I	Overvoltage protection input
17	PGND	S	Power ground (LX Power return)
18	PGND	S	Power ground (LX Power return)
19	LX	I	Input to boost switch
20	LX	I	Input to boost switch
21	FAULT	O	Fault disconnect switch
22	COMP	O	Boost compensation pin
23	VIN	S	Input voltage for the device and LED power
24	VDC	S	De-couple capacitor for internally generated supply rail. If 2.7V < VBL+ < 5.5V, apply VDC directly with a supply voltage of 2.7V to 5.5V

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED stack with the highest forward voltage drop to run at the programmed current. The ISL97636 employes current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the notebook backlight application where the power can be a series of drained batteries or instantly changed to an AC/DC adapter without rendering a noticeable visual nuisance. The number of LEDs that can be driven by ISL97636 depends on the type of LED chosen in the application. The ISL97636 is capable of boosting up to 34.5V and typically driving 9 LEDs in series for each of the 8 channels, enabling a total of 72 pieces of the 3.5V/30mA type of LEDs.

Enable and PWMI

The EN/PWMI pin serves dual purposes; it is used as an enable signal and can be used for PWM input signal for dimming. If a PWM signal is applied to this pin, the first pulse of minimum 40µs will be used as an Enable signal. If there is no signal for longer than 28ms, the device will enter shutdown. The EN/PWMI pin cannot be floating, thus a 10kΩ pull-down resistor may need to be added.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 17.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $733/R_{SET}$. The source terminals of the current source MOSFETs are designed as 100mV to minimize the power loss. The sources of errors of the channel-to-channel current matching come from the op amp's offset, internal layout and reference and these parameters are optimized for current matching and absolute current accuracy. The absolute accuracy is also determined by the external R_{SET}, and therefore a 1% tolerance resistor should be used.

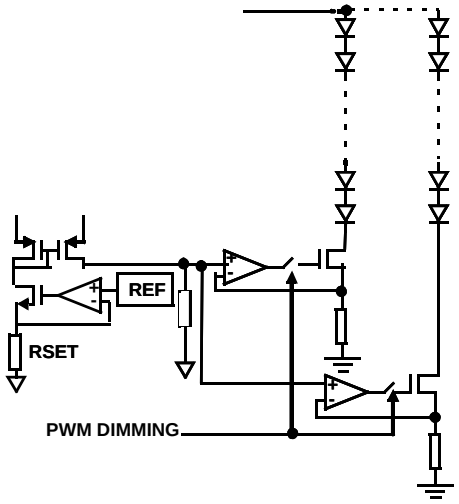


FIGURE 17. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97636 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the IIN pins. When this lowest I_{IN} voltage is lower than the short circuit threshold, V_{SC}, such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest IIN pin is at the target headroom voltage. Since all LED stacks are connected to the same output voltage, the other IIN pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same current. The output voltage will regulate cycle by cycle and it is always referenced to the highest forward voltage string in the architecture.

Dimming Controls

The ISL97636 allows two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

MAXIMUM DC CURRENT SETTING

The initial brightness should be set by choosing an appropriate value for R_{SET}. This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{733}{R_{SET}} \quad \text{(EQ. 1)}$$

DC CURRENT ADJUSTMENT

R_{SET} can be a DCP (Digitally Controlled Potentiometer) for DC current adjustment but minimum resistance should not be lower than 21kΩ for a maximum of 35mA.

For example, if the maximum required LED current ($I_{LED(max)}$) is 20mA, rearranging Equation 1 yields Equation 3:

$$R_{SET} = 733/0.02 = 36.6k\Omega \quad \text{(EQ. 2)}$$

PWM CURRENT CONTROL

The average LED current of each channel can be controlled by an external PWMI signal, as shown in Equation 3:

$$I_{LED(ave)} = I_{LED} \times PWMI \quad \text{(EQ. 3)}$$

The PWM dimming frequency can be, for example, 20kHz, but there are minimum on and off time requirements such that the dimming will be in the range of 10% to 99.5%. If the dimming frequency is below 5kHz, the dimming range can be 1% to 99.5%.

The PWM dimming off time cannot be longer than 28ms or else the driver will enter shutdown.

5V Low Dropout Regulator

A 5.2V LDO regulator is present at the VDC pin to develop the necessary low voltage supply which is used by the chips internal control circuitry. Because VDC is an LDO pin, it requires a bypass capacitor of 1µF or more for the regulation. For applications with an input voltage ≤ 5.5V, the VIN and VDC pins can be connected together. The VDC pin can be used as a coarse reference with few mA sourcing capability.

Inrush Control and Soft-start

The ISL97636 has separately built-in independent inrush control and soft-start functions. The inrush control function is built around the short circuit protection FET, and is only available in applications which include this device. At start-up, the fault protection FET is turned on slowly due to a 30µA pull-down current output from the FAULT pin. This discharges the fault FET's gate-source capacitance, turning on the FET in a controlled fashion. As this happens, the output capacitor is charged slowly through the weakly turned on FET before it becomes fully enhanced. This results in a low inrush current. This current can be further reduced by adding a capacitor (in the 1nF to 5nF range) across the gate source terminals of the FET.

Once the chip detects that the fault protection FET is turned on hard, it is assumed that inrush is complete. At this point, the boost regulator will begin to switch and the current in the inductor will ramp-up. The current in the boost power switch is monitored and the switching terminated in any cycle where the current exceeds the current limit. The ISL97636 includes a soft-start feature where this current limit starts at a low value (375mA). This is stepped up to the final 3A current limit in seven further steps of 375mA. These steps will happen over a 1ms total time, such that after 1ms the final limit will be reached. This allows the output capacitor to be charged to the required value at a low current limit and prevents high input current for systems that have only a low to medium output current requirement.

For systems with no master fault protection FET, the inrush current will flow towards C_{OUT} when VIN is applied and it is determined by the ramp rate of VIN and the values of C_{OUT} and L.

Fault Protection and Monitoring

The ISL97636 features extensive protection functions to cover all the perceivable failure conditions. The failure mode of a LED can be either open circuit or as a short. The behavior of an open circuited LED can additionally take the form of either infinite resistance or, for some LEDs, a zener diode, which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring.

Due to the lag in boost response to any load change at its output, certain transient events (such as LED current steps or significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97636 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED stacks to fault out. See Table 1 for more details.

A fault condition that results in an input current that exceeds the devices electrical limits will result in a shutdown of all output channels.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected above 8V (the action taken is described in Table 1.)

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97636 monitors the current in each channel such that any string which reaches at least 75% of the intended output current is considered “good”. Should the current subsequently fall below 50% of the target, the channel will be considered an “open circuit”. Furthermore, should the boost output of the ISL97636 reach the OVP limit or should the lower over-temperature threshold be reached, all channels which are not “good” will immediately be considered as “open circuit”. Detection of an “open circuit” channel will result in a time-out before disabling of the affected channel. This time-out is sped up when the device is above the lower over-temperature threshold in an attempt to prevent the upper over-temperature trip point from being reached.

Some users employ some special types of LEDs that have zener diode structure in parallel with the LED for ESD enhancement and enabling open circuit operation. When this type of LED is open circuited, the effect is as if the LED forward voltage has increased but no lighting. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, so as to make sure that multiple failures on one string do not cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channels look as if they have LED shorts. See Table 1 for details regarding responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as:

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER}) / R_{LOWER} \quad \text{(EQ. 4)}$$

These resistors should be large to minimize the power loss. For example, a 1MΩ R_{UPPER} and 39kΩ R_{LOWER} sets OVP to 32.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the PWM off time.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 2.45V, the device will stop switching and reset. Operation will restart when the voltage comes back into the operating range.

Input Overcurrent Protection

During normal switching operation, the current through the internal boost power FET is monitored. If the current exceeds the current limit, the internal switch will be turned off. This monitoring happens on a cycle-by-cycle basis in a self protecting way.

Additionally, the ISL97636 monitors the voltage at the LX and OVP pins. At start-up, a fixed current is injected out of the LX pins and into the output capacitor. The device will not start-up unless the voltage at LX exceeds 1.2V. Furthermore, should the voltage at LX not rise above this threshold during any subsequent period where the power FET is not switched on, it will immediately disable the input protection FET. The OVP pin is also monitored such that if it rises above and subsequently falls below 20% of the target OVP level, the input protection FET will also be switched off.

Over-Temperature Protection (OTP)

The ISL97636 includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel which is outputting current at a level significantly below the regulation target will be treated as “open circuit” and disabled after a time-out period. This time-out period is also reduced to 800µs when it is above the lower threshold. The intention of the lower threshold is to allow bad channels to be isolated and disabled before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off. Once the device has cooled to approximately +100°C, the device will restart with the DC LED current level reduced to 77% of the initial setting. If the dissipation problem persists, subsequent hitting of the limit will cause identical behavior, with the current reduced in steps to 53% and finally 30%. Unless disabled via the EN pin, the device stays in an active state throughout.

For the extensive fault protection conditions, please refer to Figure 18 and Table 1 for details.

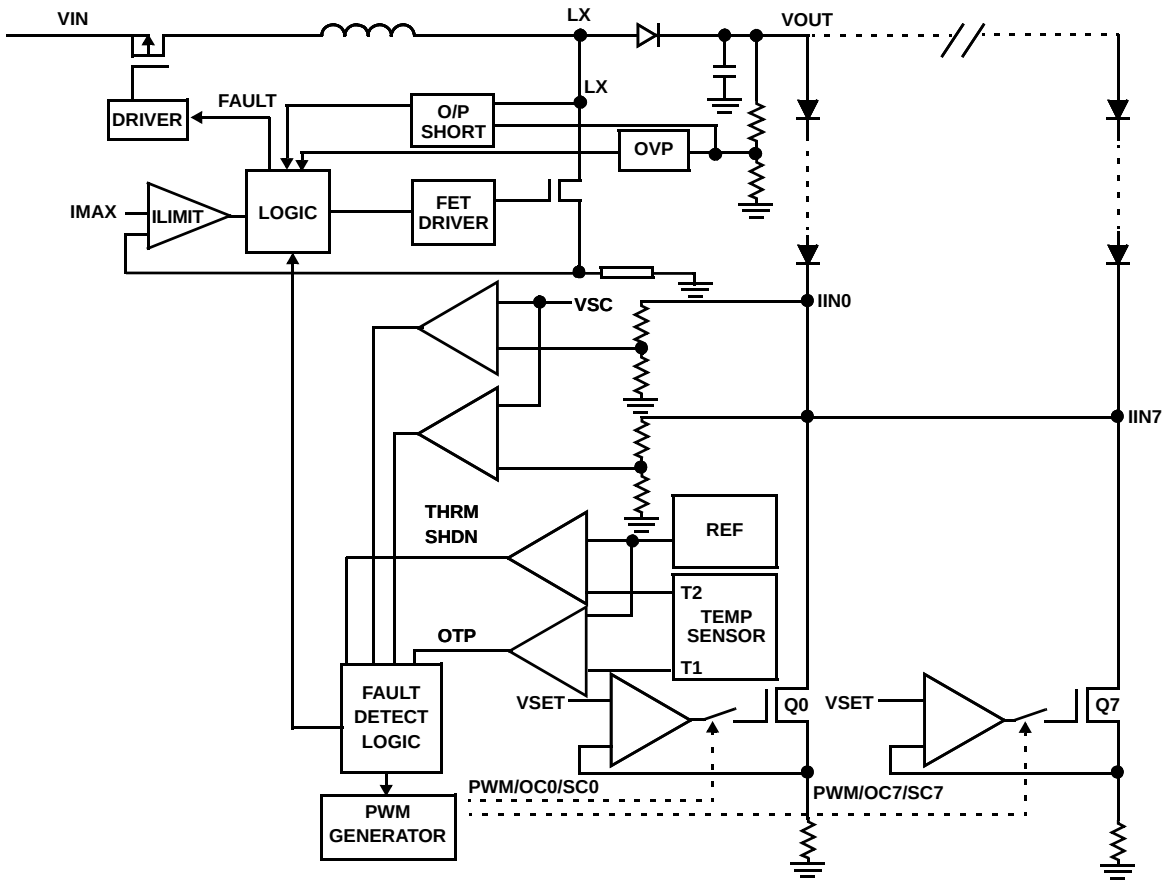


FIGURE 18. SIMPLIFIED FAULT PROTECTIONS

TABLE 1. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	VOUT REGULATED BY
1	CH0 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and VIIN0 < VSC	CH0 ON and burns power	CH1 through CH7 Normal	Highest VF of CH1 through CH7
2	CH0 Short Circuit	Upper OTP triggered but VIN0 < VSC	CH0 goes off until chip cooled and then comes back on with current reduced to 76%. Further OTP triggers result in reduction to 53%, then 30%.	Same as CH0	Highest VF of CH1 through CH7
3	CH0 Short Circuit	Upper OTP not triggered but VIIN0 > VSC	CH0 doubled after 6ms time-out. Time-out reduced to 420µs if above lower OTP limit	CH1 through CH7 Normal	Highest VF of CH1 through CH7
4	CH0 Open Circuit with infinite resistance	Upper OTP not triggered and VIIN0 < VSC	VOUT will ramp to OVP. CH0 will time-out after 6ms (800µs if above lower OTP limit) and switch off. VOUT will drop to normal level.	CH1 through CH7 Normal	Highest VF of CH1 through CH7
5	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered and VIIN0 < VSC	CH0 remains ON and has highest VF, thus VOUT increases	CH1 through CH7 ON, Q1 through Q7 burn power	VF of CH0

TABLE 1. PROTECTIONS TABLE (Continued)

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	VOUT REGULATED BY
6	CH0 LED Open Circuit but has paralleled Zener	Upper OTP triggered but VIIN0 < VSC	CH0 goes off until chip cooled and then comes back on with current reduced to 76%. Further OTP triggers result in reduction to 53%, then 30%.	Same as CH0	VF of CH0
7	CH0 LED Open Circuit but has paralleled Zener	Upper OTP not triggered but VIIN0 > VSC	CH0 OFF	CH1 through CH7 Normal	Highest VF of CH1 through CH7
		Upper OTP not triggered but VIINx > VSC	CH0 remains ON and has highest VF, thus VOUT increases.	VOUT increases then CH-X switches OFF. This is an unwanted shut off and the effect can be minimized by setting OVP at an appropriate level.	VF of CH0
8	Channel-to-Channel ΔVF too high	Lower OTP triggered but VIINx < VSC	Any channel at below 50% of the target current will fault out after 400µs. Remaining channels driven with normal current.		Highest VF of CH0 through CH7
9	Channel-to-Channel ΔVF too high	Upper OTP triggered but VIINx < VSC	All channels switched off until chip cooled and then comes back on with current reduced to 76%. Further OTP triggers result in reduction to 53%, then 30%.		Highest VF of CH0 through CH7
10	Output LED stack voltage too high	VOUT > VOVP	Driven with normal current. Any channel that is below 50% of the target current will time-out after 6ms.		Highest VF of CH0 through CH7
11	VOUT/LX shorted to GND	LX current and timing are monitored. OVP pin monitored for excursions below 20% of OVP threshold	Fault switch disabled and system shutdown until fault goes away, VOUT is checked at start-up with a low current from LX to check for presence of short before the fault switch is enabled.		

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On time is equal to the change of inductor current during the switching regulator Off time. Since the voltage across an inductor is:

$$V_L = L \times \Delta I_L / \Delta t \quad \text{(EQ. 5)}$$

and ΔI_L @ On = ΔI_L @ Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \quad \text{(EQ. 6)}$$

where D is the switching duty cycle defined by the turn-on time over the switching period. V_D is Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as:

$$V_O/V_I = 1/(1 - D) \quad \text{(EQ. 7)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 8)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

In boost mode, input current flows continuously into the inductor, with an AC ripple component proportional to the rate of inductor charging only and smaller value input capacitors may be used. It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability.

Its maximum current capability must be adequate to handle the peak current at the worst case condition. If an inductor core is chosen with too low a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the fact that the voltage across the inductor during the Off period can be shown as:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_S)] \quad \text{(EQ. 9)}$$

The choice of 85% is just an average term for the efficiency approximation. The first term is average current that is inversely proportional to the input voltage. The second term is inductor current change that is inversely proportional to L and f_S. As a result, for a given switching frequency and minimum input voltage the system operates, the inductor I_{SAT} must be chosen carefully. At a given inductor size, usually the larger the inductance, the higher the series resistance because of the extra winding of the coil. Thus the higher the inductance, the lower the peak current capability. The ISL97636 current limit may also have to be taken into account.

Output Capacitors

The output capacitor acts to smooth the output voltage and supplies load current directly during the conduction phase of the power switch. Output ripple voltage consists of the discharge of the output capacitor for I_{LPEAK} during FET On and the voltage drop due to flowing through the ESR of the output capacitor. The ripple voltage can be shown as:

$$\Delta V_{CO} = (I_O/C_O \times D/f_S) + ((I_O \times ESR) \quad \text{(EQ. 10)}$$

The conservation of charge principle in Equation 8 also brings up a fact that during the boost switch Off period, the output capacitor is charged with the inductor ripple current minus a relatively small output current in boost topology. As a result, the user needs to select an output capacitor with low ESD and with a enough input ripple current capability.

Output Ripple

ΔV_{Co} can be reduced by increasing C_O or f_S, or using small ESR capacitors. In general, ceramic capacitors are the best choice for output capacitors in small to medium sized LCD backlight applications due to their cost, form factor, and low ESR.

A larger output capacitor will also ease the driver response during PWM dimming Off period due to the longer sample and hold effect of the output drooping. The driver does not need to boost harder in the next On period that minimizes transient current. The output capacitor is also needed for compensation, and in general, 2x4.7µF/50V ceramic capacitors are suitable for the notebook display backlight applications.

Schottky Diode

A high speed rectifier diode is necessary to prevent excessive voltage overshoot, especially in the boost configuration. Low forward voltage and reverse leakage current will minimize losses, making Schottky diodes the preferred choice. Although the Schottky diode turns on only during the boost switch Off period, it carries the same peak current as the inductor's, and therefore, a suitable current rated Schottky diode must be used.

Applications

High Current Applications

Each channel of the ISL97636 can support up to 35mA. For applications that need higher current, multiple channels can be grouped to achieve the desirable current. For example, the cathode of the last LED can be connected to IIN0 to IIN2; this configuration can be treated as a single string with 105mA current driving capability.

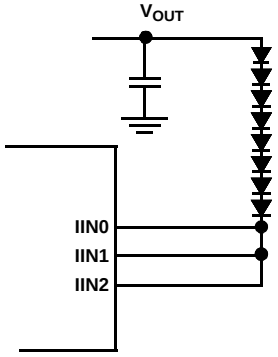
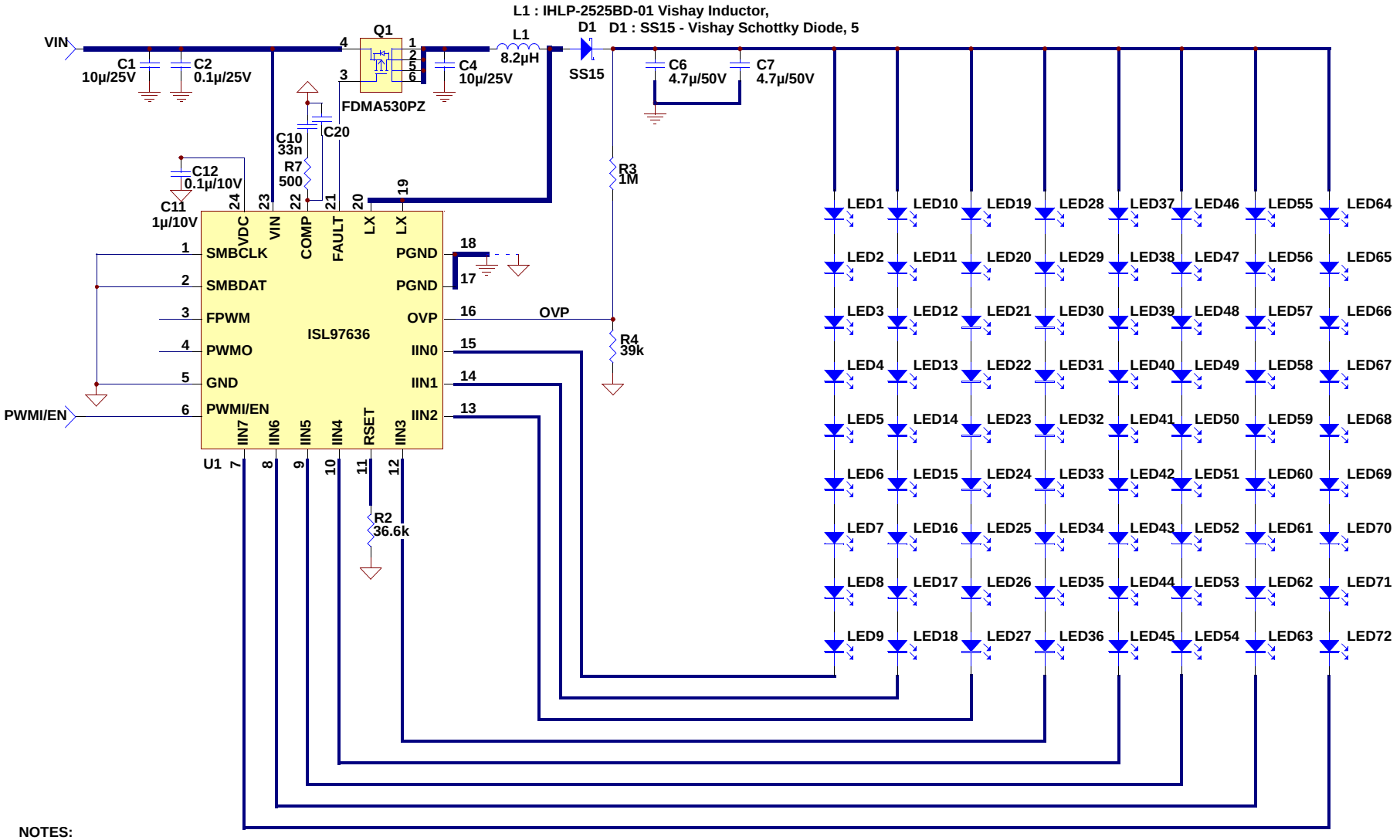


FIGURE 19. GROUPING MULTIPLE CHANNELS FOR HIGH CURRENT APPLICATIONS

Compensation

The ISL97636 has two main elements in the system; the Current Mode Boost Regulator and the op amp based multi-channel current sources. The ISL97636 incorporates a transconductance amplifier in its feedback path to allow the user some levels of adjustment on the transient response and better regulation. The ISL97636 uses current mode control architecture, which has a fast current sense loop and a slow voltage feedback loop. The fast current feedback loop does not require any compensation. The slow voltage loop must be compensated for stable operation. The

compensation network is a series Rc, Cc1 network from COMP pin to ground and an optional Cc2 capacitor connected to the COMP pin. The Rc sets the high frequency integrator gain for fast transient response and the Cc1 sets the integrator zero to ensure loop stability. For most applications, Rc is in the range of 200Ω to 3kΩ and Cc1 is in the range of 27nF to 37nF. Depending upon the PCB layout, a Cc2, in range of 100nF, may be needed to create a pole to cancel the output capacitor ESR's zero effect for stability. The ISL97636 evaluation board is configured with Rc1 of 500Ω, Cc1 of 33nF, and Cc2 of 0, which achieves stability. In the actual applications, these values may need to be tuned empirically but the recommended values are usually a good starting point.



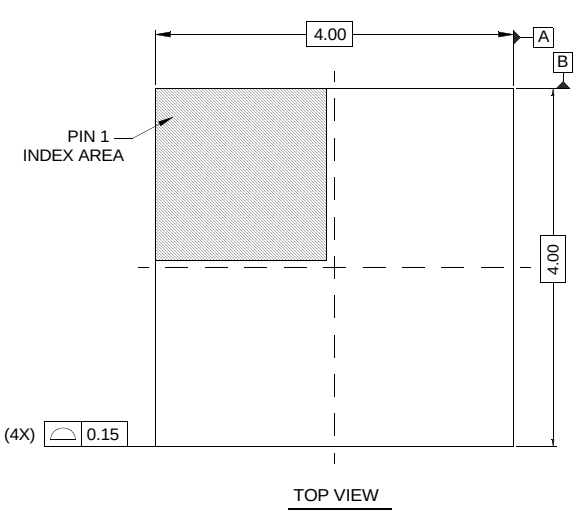
NOTES:
FOR 2 LAYERS BOARD, LAYOUT PGND (NOISY GROUND) ON TOP LAYER AND AGND (QUIET GROUND) ON BOTTOM LAYER. TIE PGND AND AGND ONLY AT ONE POINT BY DOING THIS: BRIDGE U1 PGND (PINS 18 AND 19) AND AGND (PIN 5) TO THE PACKAGE THERMAL PAD. PUT MULTIPLE VIAS ON THE THERMAL PAD THAT CONNECTS TO THE BOTTOM SIDE AGND.

FIGURE 20. TYPICAL APPLICATION CIRCUIT

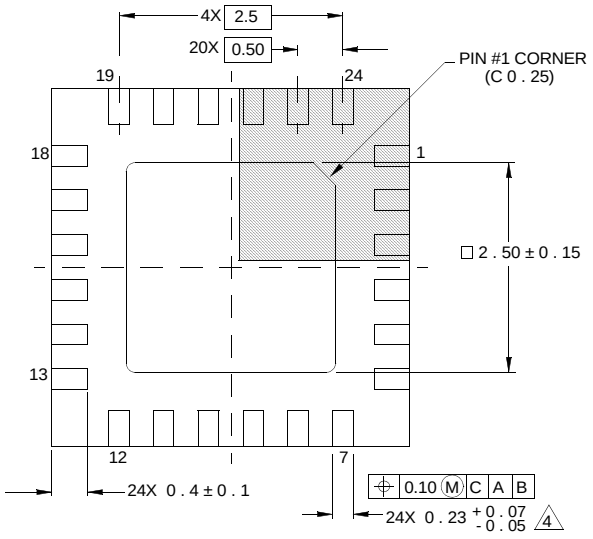
Package Outline Drawing

L24.4x4D

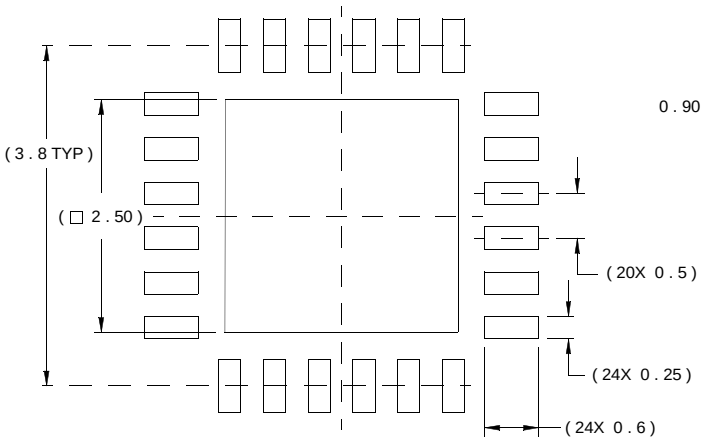
24 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 10/06



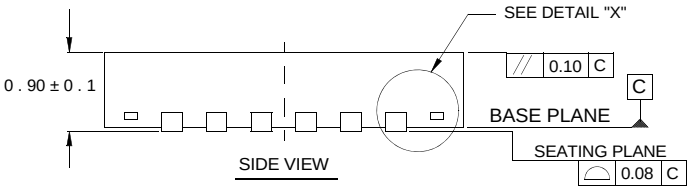
TOP VIEW



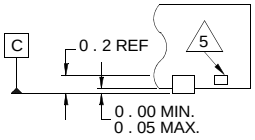
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.