QL3004E pASIC 3 FPGA Data Sheet

4,000 Usable PLD Gate pASIC 3 FPGA Combining High Performance and High Density

Device Highlights

High Performance & High Density

- 4,000 Usable PLD Gates with 82 I/Os
- 300 MHz 16-bit Counters, 400 MHz Datapaths
- 0.35 µm four-layer metal non-volatile CMOS process for smallest die sizes

Easy-to-Use / Fast Development Cycles

- 100% routable with 100% utilization and complete pin-out stability
- Variable-grain logic cells provide high performance and 100% utilization
- Comprehensive design tools include high quality Verilog/VHDL synthesis

Advanced I/O Capabilities

- Interfaces with both 3.3 V and 5.0 V devices
- PCI compliant with 3.3 V and 5.0 V buses for -1/-2/-3/-4 speed grades
- Full JTAG boundary scan
- I/O Cells with individually controlled Registered Input Path and Output Enables

Total of 82 I/O Pins

- 74 bidirectional input/output pins, PCI-compliant for 5.0 V and 3.3 V buses for -1/-2/-3/-4 speed grades
- Four High-Drive input-only pins
- Four High-Drive/distributed network pins

Four Low-Skew Distributed Networks

- Two array clock/control networks available to the logic cell flip-flop clock, set and reset inputs — each driven by an input-only pin
- Two global clock/control networks available to the logic cell; F1, clock, set and reset inputs and the data input, I/O register clock, reset and enable inputs as well as the output enable control — each driven by an input-only or I/O pin, or any logic cell output or I/O cell feedback

High Performance

- Input + logic cell + output total delays under 6 ns
- Data path speeds over 400 MHz
- Counter speeds over 300 MHz

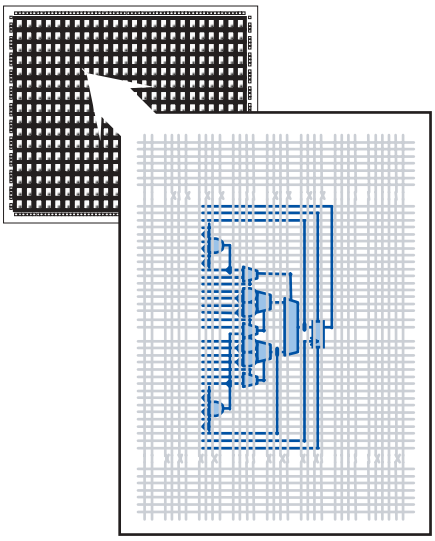


Figure 1: 160 pASIC 3 Logic Cells

Architecture Overview

The QL3004E is a 4,000 usable PLD gate member of the pASIC 3 family of FPGAs. pASIC 3 FPGAs are fabricated on a 0.35 µm four-layer metal process using QuickLogic®'s patented ViaLink® technology to provide a unique combination of high performance, high density, low cost, and extreme ease-of-use.

The QL3004E contains 96 logic cells. With a maximum of 74 I/Os, the QL3004E is available 68-pin PLCC, 84-pin PLCC, and 100-pin TQFP packages.

Software support for the complete pASIC 3 family, including the QL3004E, is available through three basic packages. The turnkey Quick*Works*® package provides the most complete FPGA software solution from design entry to logic synthesis, to place and route, to simulation. The QuickTools™ for Workstations package provides a solution for designers who use Cadence®, Exemplar™, Mentor®, Synopsys®, Synplicity®, Viewlogic™, Aldec™, or other third-party tools for design entry, synthesis, or simulation.

Electrical Specifications

AC Characteristics at V_{CC} = 3.3 V, TA = 25°C (K = 1.00)

To calculate delays, multiply the appropriate K factor from **Table 7** by the numbers provided in **Table 1** through **Table 5**.

Table 1: Logic Cells

Symbol	Parameter	Propagation Delays (ns) Fanout[a]				
		1	2	3	4	8
t_{PD}	Combinatorial Delay [b]	1.4	1.7	1.9	2.2	3.2
t_{SU}	Setup Time [b]	1.7	1.7	1.7	1.7	1.7
t_{H}	Hold Time	0.0	0.0	0.0	0.0	0.0
t_{CLK}	Clock to Q Delay	0.7	1.0	1.2	1.5	2.5
t_{CWHI}	Clock High Time	1.2	1.2	1.2	1.2	1.2
t_{CWLO}	Clock Low Time	1.2	1.2	1.2	1.2	1.2
t_{SET}	Set Delay	1.0	1.3	1.5	1.8	2.8
t_{RESET}	Reset Delay	0.8	1.1	1.3	1.6	2.6
t_{SW}	Set Width	1.9	1.9	1.9	1.9	1.9
t_{RW}	Reset Width	1.8	1.8	1.8	1.8	1.8

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.

b. These limits are derived from a representative selection of the slowest paths through the pASIC 3 logic cell including typical net delays. Worst case delay values for specific paths should be determined from timing analysis of your particular design.

Table 2: Input-Only/Clock Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]						
		1	2	3	4	8	12	24
t_{IN}	High Drive Input Delay	1.5	1.6	1.8	1.9	2.4	2.9	4.4
t_{INI}	High Drive Input, Inverting Delay	1.6	1.7	1.9	2.0	2.5	3.0	4.5
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0
t_{ICLK}	Input Register Clock To Q	0.7	0.8	1.0	1.1	1.6	2.1	3.6
t_{IRST}	Input Register Reset Delay	0.6	0.7	0.9	1.0	1.5	2.0	3.5
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.

Table 3: Clock Cells

Symbol	Parameter	Propagation Delays (ns) Loads per Half Column [a]						
		1	2	3	4	8	10	11
t_{ACK}	Array Clock Delay	1.2	1.2	1.3	1.3	1.5	1.6	1.7
t_{GCKP}	Global Clock Pin Delay	0.7	0.7	0.7	0.7	0.7	0.7	0.7
t_{GCKB}	Global Clock Buffer Delay	0.8	0.8	0.9	0.9	1.1	1.2	1.3

a. The array distributed networks consist of 24 half columns and the global distributed networks consist of 28 half columns, each driven by an independent buffer. The number of half columns used does not affect clock buffer delay. The array clock has up to eight loads per half column. The global clock has up to 7 loads per half column.

Table 4: Input-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Fanout [a]					
		1	2	3	4	8	10
$t_{I/O}$	Input Delay (bidirectional pad)	1.3	1.6	1.8	2.1	3.1	3.6
t_{ISU}	Input Register Set-Up Time	3.1	3.1	3.1	3.1	3.1	3.1
t_{IH}	Input Register Hold Time	0.0	0.0	0.0	0.0	0.0	0.0
t_{IOCLK}	Input Register Clock To Q	0.7	1.0	1.2	1.5	2.5	3.0
t_{IORST}	Input Register Reset Delay	0.6	0.9	1.1	1.4	2.4	2.9
t_{IESU}	Input Register clock Enable Set-Up Time	2.3	2.3	2.3	2.3	2.3	2.3
t_{IEH}	Input Register Clock Enable Hold Time	0.0	0.0	0.0	0.0	0.0	0.0

a. Stated timing for worst case Propagation Delay over process variation at V_{CC} = 3.3 V and TA = 25°C. Multiply by the appropriate Delay Factor, K, for speed grade, voltage, and temperature settings as specified in **Table 7**.

Table 5: Output-Only I/O Cells

Symbol	Parameter	Propagation Delays (ns) Output Load Capacitance (pF)				
		30	50	75	100	150
t_{OUTLH}	Output Delay Low to High	2.1	2.5	3.1	3.6	4.7
t_{OUTHL}	Output Delay High to Low	2.2	2.6	3.2	3.7	4.8
t_{PZH}	Output Delay Tri-state to High	1.2	1.7	2.2	2.8	3.9
t_{PZL}	Output Delay Tri-state to Low	1.6	2.0	2.6	3.1	4.2
t_{PHZ}	Output Delay High to Tri-State [a]	2.0	-	-	-	-
t_{PLZ}	Output Delay Low to Tri-State	1.2	-	-	-	-

a. The loads presented in **Figure 2** are used for t_{PXZ}:

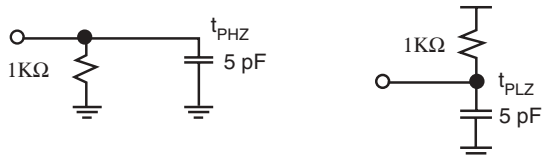


Figure 2: Loads used for t_{PXZ}

DC Characteristics

The DC specifications are provided in **Table 6** through **Table 8**.

Table 6: Absolute Maximum Ratings

Parameter	Value	Parameter	Value
V_{CC} Voltage	-0.5 V to 4.6 V	DC Input Current	±20 mA
V_{CCIO} Voltage	-0.5 V to 7.0 V	ESD Pad Protection	±2000 V
Input Voltage	-0.5 V to V_{CCIO} +0.5 V	Storage Temperature	-65°C to +150°C
Latch-up Immunity	±200 mA	Lead Temperature	300°C

Table 7: Operating Range

Symbol	Parameter		Military		Industrial		Commercial		Unit
			Min	Max	Min	Max	Min	Max	
V_{CC}	Supply Voltage		3.0	3.6	3.0	3.6	3.0	3.6	V
V_{CCIO}	I/O Input Tolerance Voltage		3.0	5.5	3.0	5.5	3.0	5.25	V
TA	Ambient Temperature		-55	-	-40	85	0	70	°C
TC	Case Temperature		-	125	-	-	-	-	°C
K	Delay Factor	-0 Speed Grade	-	-	0.43	1.90	0.46	1.85	n/a
		-1 Speed Grade	0.42	1.64	0.43	1.54	0.46	1.50	n/a
		-2 Speed Grade	0.42	1.37	0.43	1.28	0.46	1.25	n/a
		-3 Speed Grade			0.43	0.90	0.46	0.88	n/a
		-4 Speed Grade			0.43	0.82	0.46	0.80	n/a

Table 8: DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Units
V_{IH}	Input HIGH Voltage		0.5 V_{CC}	V_{CCIO}+0.5	V
V_{IL}	Input LOW Voltage		-0.5	0.3 V_{CC}	V
V_{OH}	Output HIGH Voltage	IOH = -12 mA	2.4		V
		IOH = -500 µA	0.9 V_{CC}		V
V_{OL}	Output LOW Voltage	IOL = 16 mA[a]		0.45	V
		IOL = 1.5 mA		0.1 V_{CC}	V
I_I	I or I/O Input Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
I_{OZ}	3-State Output Leakage Current	VI = V_{CCIO} or GND	-10	10	µA
C_I	Input Capacitance[b]			10	pF
I_{OS}	Output Short Circuit Current[c]	VO = GND	-15	-180	mA
		VO = V_{CC}	40	210	mA
I_{CC}	D.C. Supply Current[d]	VI, VIO = V_{CCIO} or GND	0.50 (typ)	2	mA
I_{CCIO}	D.C. Supply Current on V_{CCIO}		0	100	µA

a. Applies only to -1/-2/-3/-4 commercial grade devices. These speed grades are also PCI-compliant. All other devices have 8 mA IOL specifications.
b. Capacitance is sample tested only. Clock pins are 12 pF maximum.
c. Only one output at a time. Duration should not exceed 30 seconds.
d. For -1/-2/-3/-4 commercial grade devices only. Maximum I_{CC} is 3 mA for -0 commercial grade and all industrial grade devices, and 5 mA for all military grade devices. For AC conditions, contact QuickLogic customer applications group (see **Contact Information**).

Kv and Kt Graphs

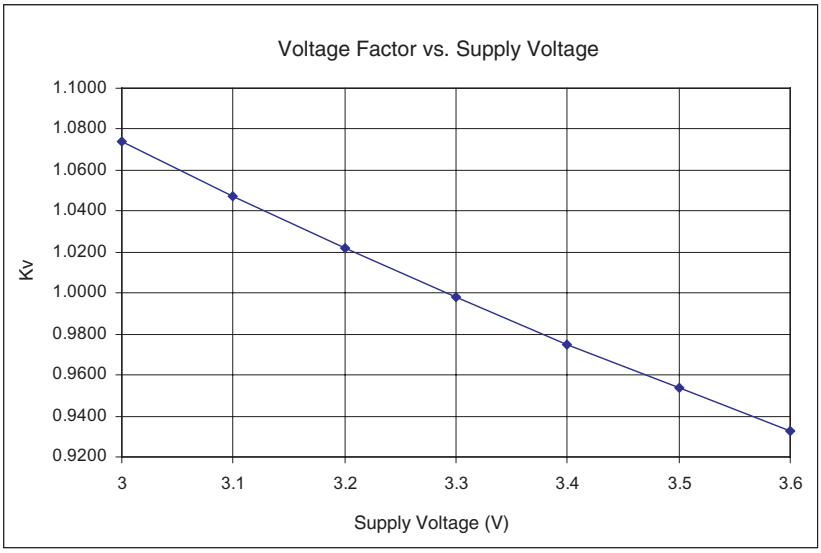


Figure 3: Voltage Factor vs. Supply Voltage

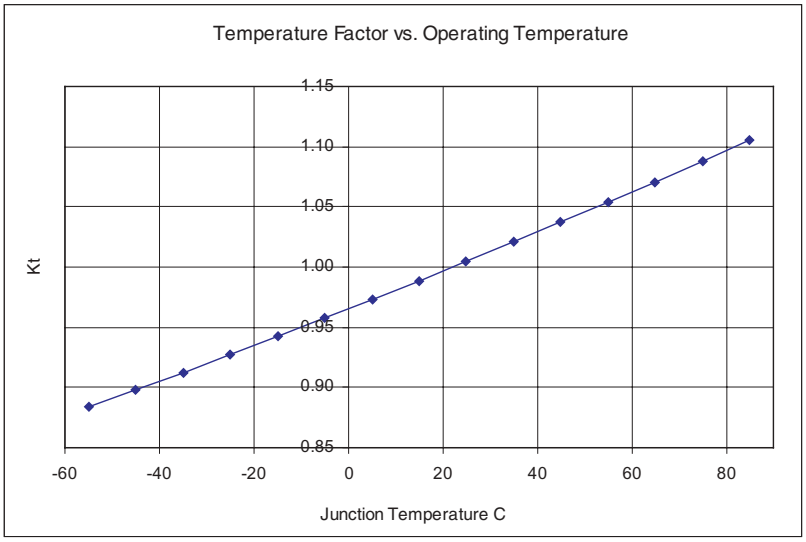


Figure 4: Temperature Factor vs. Operating Temperature

Power-up Sequencing

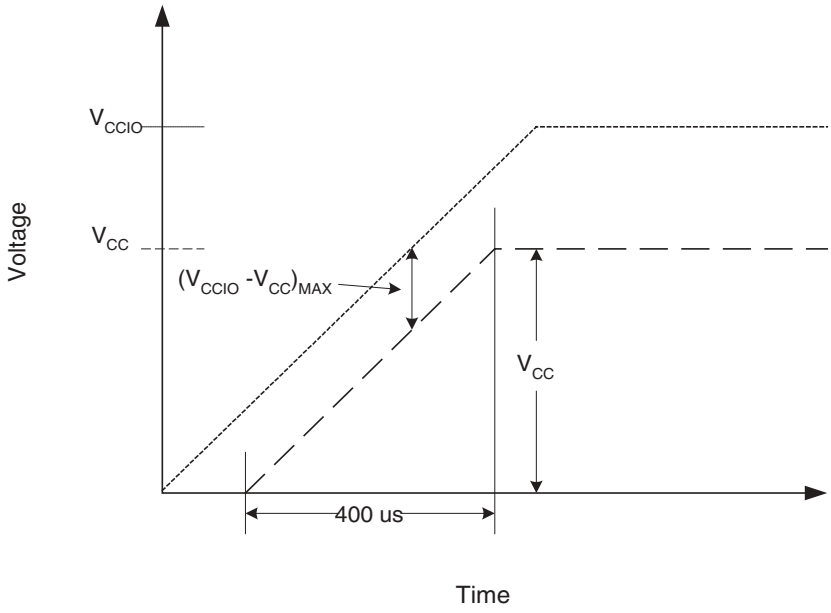


Figure 5: Power-up Requirements

The following requirements must be met when powering up the device (see **Figure 5**). QuickLogic recommends the following for the lowest possible power-up current. Not following these recommendations will cause the device to draw more current during power-up:

- When ramping up the power supplies keep $(V_{CCIO} - V_{CC})_{MAX} \leq 500$ mV.
- V_{CCIO} must lead V_{CC} when ramping the device.

The power supply must take greater than or equal to 400 µs to reach V_{CC}. Ramping to V_{CC}/V_{CCIO} earlier than 400 µs can cause the device to behave improperly.

JTAG

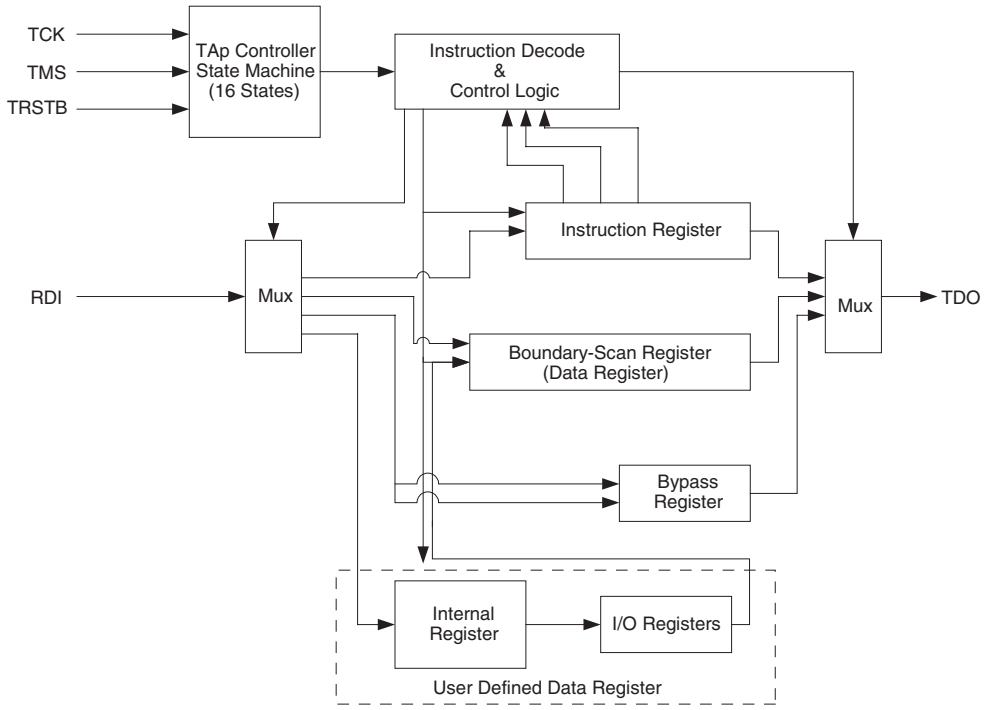


Figure 6: JTAG Block Diagram

Microprocessors and Application Specific Integrated Circuits (ASICs) pose many design challenges, not the least of which concerns the accessibility of test points. The Joint Test Access Group (JTAG) formed in response to this challenge, resulting in IEEE standard 1149.1, the Standard Test Access Port and Boundary Scan Architecture.

The JTAG boundary scan test methodology allows complete observation and control of the boundary pins of a JTAG-compatible device through JTAG software. A Test Access Port (TAP) controller works in concert with the Instruction Register (IR); these allow users to run three required tests, along with several user-defined tests.

JTAG tests allow users to reduce system debug time, reuse test platforms and tools, and reuse subsystem tests for fuller verification of higher level system elements.

The 1149.1 standard requires the following three tests:

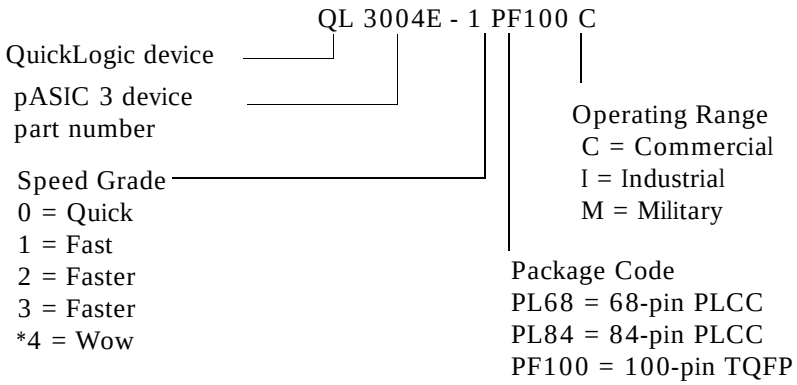
- **Extest Instruction.** The Extest instruction performs a PCB interconnect test. This test places a device into an external boundary test mode, selecting the boundary scan register to be connected between the TAP's Test Data In (TDI) and Test Data Out (TDO) pins. Boundary scan cells are preloaded with test patterns (via the Sample/Preload Instruction), and input boundary cells capture the input data for analysis.
- **Sample/Preload Instruction.** This instruction allows a device to remain in its functional mode, while selecting the boundary scan register to be connected between the TDI and TDO pins. For this test, the boundary scan register can be accessed via a data scan operation, allowing users to sample the functional data entering and leaving the device.
- **Bypass Instruction.** The Bypass instruction allows data to skip a device's boundary scan entirely, so the data passes through the bypass register. The Bypass instruction allows users to test a device without passing through other devices. The bypass register is connected between the TDI and TDO pins, allowing serial data to be transferred through a device without affecting the operation of the device.

Pin Descriptions

Table 9: Pin Descriptions

Pin	Function	Description
TDI	Test Data In for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TRSTB	Active low Reset for JTAG	Hold LOW during normal operation. Connect to ground if not used for JTAG.
TMS	Test Mode Select for JTAG	Hold HIGH during normal operation. Connect to V_{CC} if not used for JTAG.
TCK	Test Clock for JTAG	Hold HIGH or LOW during normal operation. Connect to V_{CC} or ground if not used for JTAG.
TDO	Test data out for JTAG	Output that must be left unconnected if not used for JTAG.
STM	Special Test Mode	Must be grounded during normal operation.
I/ACLK	High-drive input and/or array network driver	Can be configured as either or both.
I/GCLK	High-drive input and/or global network driver	Can be configured as either or both.
I	High-drive input	Use for input signals with high fanout.
I/O	Input/Output pin	Can be configured as an input and/or output.
V_{CC}	Power supply pin	Connect to 3.3 V supply.
V_{CCIO}	Input voltage tolerance pin	Connect to 5.0 V supply if 5 V input tolerance is required, otherwise connect to 3.3 V supply.
GND	Ground pin	Connect to ground.

Ordering Information



* Contact QuickLogic regarding availability (see **Contact Information**)

68 PLCC Pinout Diagram

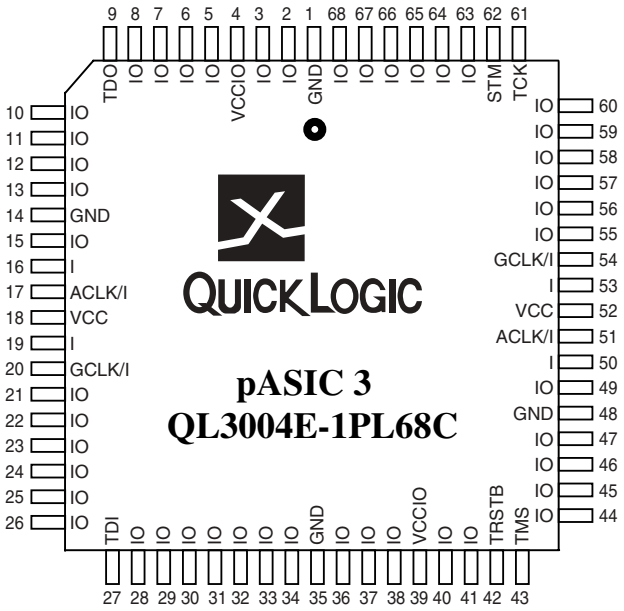


Figure 7: Top View of 68 Pin PLCC

68 PLCC Pinout Table

Table 10: 68 PLCC Pinout Table

68 PLCC	Function	68 PLCC	Function	68 PLCC	Function	68 PLCC	Function
1	GND	18	V_{CC}	35	GND	52	V_{CC}
2	I/O	19	I	36	I/O	53	I
3	I/O	20	GCLK/I	37	I/O	54	GCLK/I
4	V_{CCIO}	21	I/O	38	I/O	55	I/O
5	I/O	22	I/O	39	V_{CCIO}	56	I/O
6	I/O	23	I/O	40	I/O	57	I/O
7	I/O	24	I/O	41	I/O	58	I/O
8	I/O	25	I/O	42	TRSTB	58	I/O
9	TDO	26	I/O	43	TMS	60	I/O
10	I/O	27	TDI	44	I/O	61	TCK
11	I/O	28	I/O	45	I/O	62	STM
12	I/O	29	I/O	46	I/O	63	I/O
13	I/O	30	I/O	47	I/O	64	I/O
14	GND	31	I/O	48	GND	65	I/O
15	I/O	32	I/O	49	I/O	66	I/O
16	I	33	I/O	50	I	67	I/O
17	ACLK/I	34	I/O	51	ACLK/I	68	I/O

84 PLCC Pinout Diagram

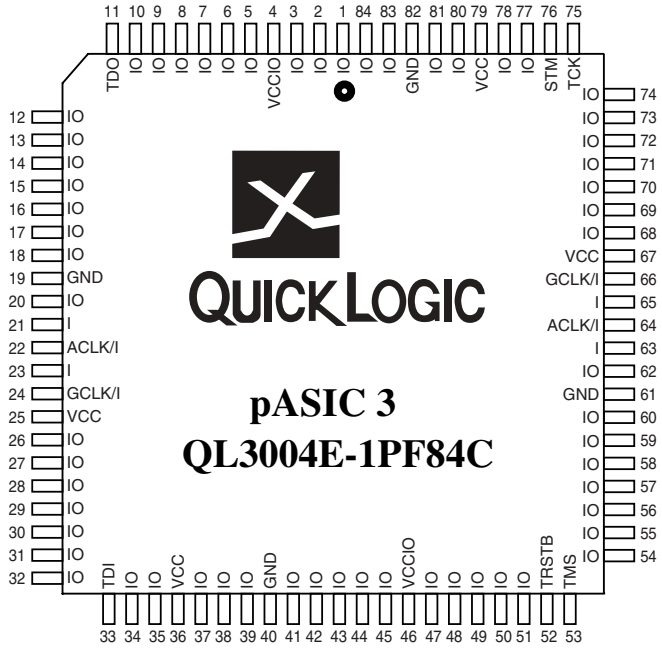


Figure 8: Top View of 84 Pin PLCC

84 PLCC Pinout Diagram

Table 11: 84 PLCC Pinout Diagram

84 PLCC	Function	84 PLCC	Function	84 PLCC	Function	84 PLCC	Function
1	I/O	22	ACLK/I	43	I/O	64	ACLK/I
2	I/O	23	I	44	I/O	65	I
3	I/O	24	GCLK/I	45	I/O	66	GCLK/I
4	V_{CCIO}	25	V_{CC}	46	V_{CCIO}	67	VCC
5	I/O	26	I/O	47	I/O	68	I/O
6	I/O	27	I/O	48	I/O	69	I/O
7	I/O	28	I/O	49	I/O	70	I/O
8	I/O	29	I/O	50	I/O	71	I/O
9	I/O	30	I/O	51	I/O	72	I/O
10	I/O	31	I/O	52	TRSTB	73	I/O
11	TDO	32	I/O	53	TMS	74	I/O
12	I/O	33	TDI	54	I/O	75	TCK
13	I/O	34	I/O	55	I/O	76	STM
14	I/O	35	I/O	56	I/O	77	I/O
15	I/O	36	V_{CC}	57	I/O	78	I/O
16	I/O	37	I/O	58	I/O	79	V_{CC}
17	I/O	38	I/O	59	I/O	80	I/O
18	I/O	39	I/O	60	I/O	81	I/O
19	GND	40	GND	61	GND	82	GND
20	I/O	41	I/O	62	I/O	83	I/O
21	I	42	I/O	63	I	84	I/O

100 TQFP Pinout Diagram

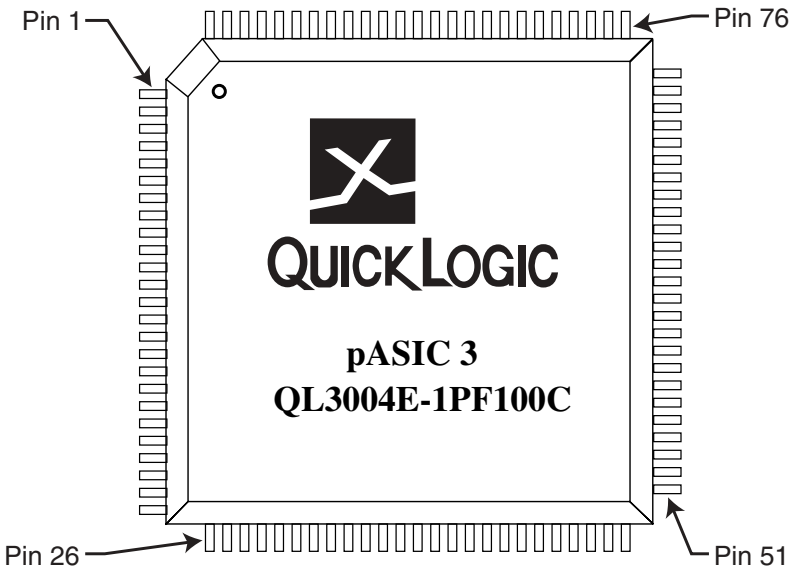


Figure 9: Top View of 100 Pin TQFP

100 TQFP Pinout Table

Table 12: 100 TQFP Pinout Table

100 TQFP	Function	100 TQFP	Function	100 TQFP	Function	100 TQFP	Function
1	I/O	26	TDI	51	I/O	76	TCK
2	I/O	27	I/O	52	I/O	77	STM
3	I/O	28	I/O	53	I/O	78	I/O
4	I/O	29	I/O	54	I/O	79	I/O
5	I/O	30	I/O	55	I/O	80	I/O
6	I/O	31	I/O	56	I/O	81	I/O
7	I/O	32	I/O	57	I/O	82	I/O
8	I/O	33	I/O	58	I/O	83	I/O
9	GND	34	I/O	59	GND	84	I/O
10	I/O	35	GND	60	I/O	85	GND
11	I	36	I/O	61	I	86	I/O
12	ACLK / I	37	I/O	62	ACLK / I	87	I/O
13	V_{CC}	38	GND	63	V_{CC}	88	GND
14	I	39	I/O	64	I	89	I/O
15	GCLK / I	40	I/O	65	GCLK / I	90	I/O
16	V_{CC}	41	I/O	66	V_{CC}	91	I/O
17	I/O	42	V_{CCIO}	67	I/O	92	V_{CCIO}
18	I/O	43	I/O	68	I/O	93	I/O
19	I/O	44	I/O	69	I/O	94	I/O
20	I/O	45	I/O	70	I/O	95	I/O
21	I/O	46	I/O	71	I/O	96	I/O
22	I/O	47	I/O	72	I/O	97	I/O

Table 12: 100 TQFP Pinout Table

100 TQFP	Function	100 TQFP	Function	100 TQFP	Function	100 TQFP	Function
23	I/O	48	I/O	73	I/O	98	I/O
24	I/O	49	TRSTB	74	I/O	99	I/O
25	I/O	50	TMS	75	I/O	100	TDO

Contact Information

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E-mail:	info@quicklogic.com
Support:	support@quicklogic.com
Web site:	http://www.quicklogic.com/

Revision History

Table 13: Revision History

Revision	Date	Comments
A	January 2003	Brian Faith, Andreea Rotaru

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