General Purpose CMOS Six Channel Analog Input Front End

Preliminary Technical Data — AD73360

FEATURES

Six 16-Bit A/D Converters
Programmable Input Sample Rate
75 dB ADC SNR
64 kS/s Maximum Sample Rate
~~TBD~~ dB Crosstalk
Low Group Delay (25 μs typ per ADC Channel
Programmable Input Gain
Flexible Serial Port which Allows multiple devices to be Connected in Cascade
Single (+2.7 V to +5.5 V) Supply Operation
~~TBD~~ mW Max Power Consumption at 2.7 V
On-Chip Reference
28-Pin SOIC & 44-Pin LQFP Packages

APPLICATIONS

General Purpose Analog Input
Industrial Power Metering

GENERAL DESCRIPTION

The AD73360 is a six channel analog input front-end processor for general purpose applications including industrial power metering or multi-channel analog inputs. It features six 16-bit A/D conversion channels each of which provide 70 dB signal-to-noise ratio over a voiceband signal bandwidth. It also features a programmable input gain amplifier (PGA) with gain settings in eight stages from 0 dB to 38 dB.

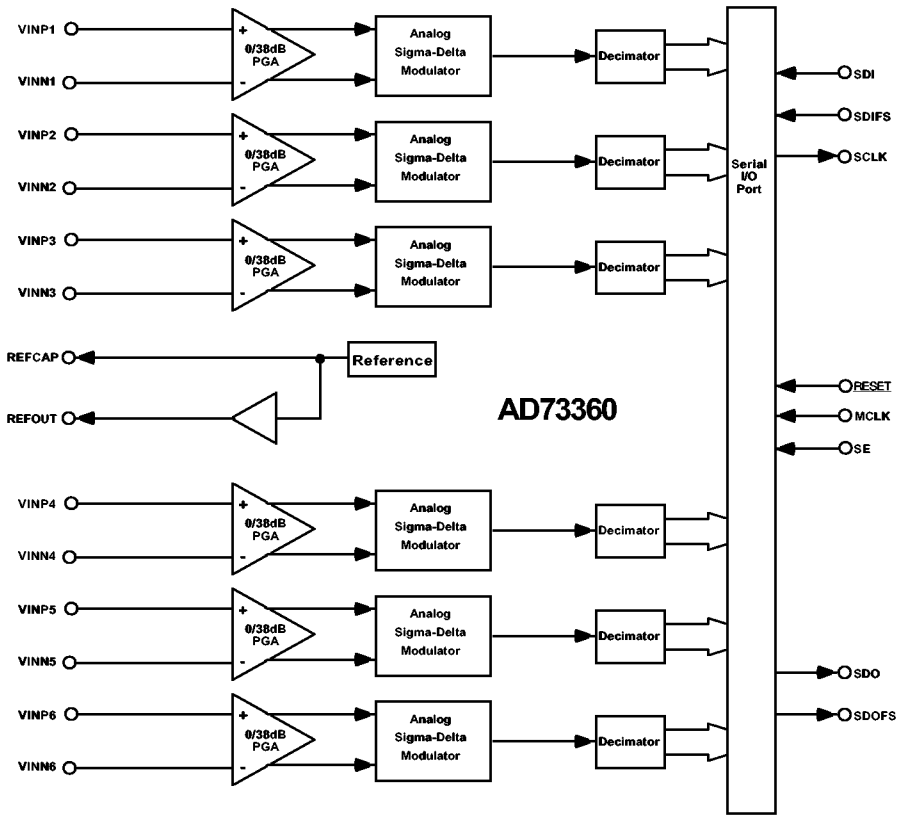
The AD73360 is particularly suitable for industrial power metering as each channel samples synchronously ensuring that there is very little time (phase) delay between the conversions. The AD73360 also features low group delay conversions on all channels.

An on-chip reference voltage is included to allow single supply operation. This reference is programmable to accomodate either 3V or 5V operation.

The sampling rate of the device is programmable with four separate settings offering 64, 32, 16 and 8 kHz sampling rates (from a master clock of 16.384 MHz).

A serial port (SPORT) allows easy interfacing of single or cascaded devices to industry standard DSP engines. The SPORT transfer rate is programmable to allow interfacing to both fast and slow DSP engines.

The AD73360 is available in 28-pin SOIC and 44-pin LQFP packages.



AD73360–SPECIFICATIONS[1] (AVDD = +3 V ± 10%; DVDD = +3 V ± 10%; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, F_S = 64 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	AD73360A Min	Typ	Max	Units	Test Conditions/Comments
REFERENCE					5VEN = 0
REFCAP					
Absolute Voltage, V_{REFCAP}	1.08	1.2	1.32	V	
REFCAP TC		50		ppm/°C	0.1 µF Capacitor Required from
REFOUT					REFCAP to AGND2
Typical Output Impedance		68		Ω	
Absolute Voltage, V_{REFOUT}	1.08	1.2	1.32	V	Unloaded
Minimum Load Resistance	1			kΩ	
Maximum Load Capacitance			100	pF	
ADC SPECIFICATIONS					
Maximum Input Range at VIN[2, 3]			1.578	V p-p	5VEN = 0, Measured Differentially
			–2.85	dBm	
Nominal Reference Level at VIN		1.0954		V p-p	5VEN = 0, Measured Differentially
(0 dBm0)		–6.02		dBm	
Absolute Gain					
PGA = 0 dB	–0.75	0.1	+1.0	dB	1.0 kHz, 0 dBm0
PGA = 38 dB	–1.5	–0.5	+0.5	dB	1.0 kHz, 0 dBm0
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion)					
PGA = 0 dB	70	76		dB	0 Hz to Fs/2; Fs = 8 kHz
				dB	0 Hz to Fs/2; Fs = 16 kHz
				dB	0 Hz to Fs/2; Fs = 32 kHz
				dB	0 Hz to Fs/2; Fs = 64 kHz
PGA = 38 dB	61	65		dB	0 Hz to Fs/2; Fs = 8 kHz
Total Harmonic Distortion					
PGA = 0 dB		–83	–70	dB	
PGA = 38 dB		–83	–70	dB	
Intermodulation Distortion		–78		dB	PGA = 0 dB
Idle Channel Noise		–76		dBm0	PGA = 0 dB
Crosstalk ADC-to-ADC		TBD		dB	ADC1 Input Signal Level: 1.0 kHz, 0 dBm0
					ADC2 Input at Idle
DC Offset	–20	+15	+50	mV	PGA = 0 dB
Power Supply Rejection		–55		dB	Input Signal Level at AVDD and DVDD
					Pins 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	64 kHz Output Sample Rate
		TBD		µs	32 kHz Output Sample Rate
		TBD		µs	16 kHz Output Sample Rate
		TBD		µs	8 kHz Output Sample Rate
Input Resistance at VIN[2, 4]		25		kΩ[6]	DMCLK = 16.384 MHz
FREQUENCY RESPONSE					
(ADC)[9] Typical Output					
Frequency (Normalised to F_S)					
0		0		dB	
0.03125		–0.1		dB	
0.0625		–0.25		dB	
0.125		–0.6		dB	
0.1875		–1.4		dB	
0.25		–2.8		dB	
0.3125		–4.5		dB	
0.375		–7.0		dB	
0.4375		–9.5		dB	
> 0.5		< –12.5		dB	

Parameter	AD73322A Min	Typ	Max	Units	Test Conditions/Comments
LOGIC INPUTS					
V_{INH}, Input High Voltage	V_{DD} – 0.8		V_{DD}	V	
V_{INL}, Input Low Voltage	0		0.8	V	
I_{IH}, Input Current			10	µA	
C_{IN}, Input Capacitance			10	pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	V_{DD} – 0.4		V_{DD}	V	|IOUT| - 100 µA
V_{OL}, Output Low Voltage	0		0.4	V	|IOUT| - 100 µA
Three-State Leakage Current	–10		+10	µA	
POWER SUPPLIES					
AVDD1, AVDD2	2.7		3.3	V	
DVDD	2.7		3.3	V	
I_{DD}[10]					See Table I

NOTES
[1] Operating temperature range is as follows: –40°C to +85°C. Therefore, T_{MIN} = –40°C and T_{MAX} = +85°C.
[2] Test conditions: Input PGA set for 0 dB gain (unless otherwise noted).
[3] At input to sigma-delta modulator of ADC.
[4] Guaranteed by design.
[5] Overall group delay will be affected by the sample rate and the external digital filtering.
[6] The ADC's input impedance is inversely proportional to DMCLK and is approximated by: $(4 * 10^{11})$/DMCLK.
[9] Frequency response of ADC measured with input at audio reference level (the input level that produces an output level of –10 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.
[10] Test Conditions: no load on digital inputs, analog inputs ac coupled to ground.

Specifications subject to change without notice.

Table I. Current Summary (AVDD = DVDD = +3.3 V)

Conditions	Analog Current	Internal Digital Current	External Interface Current	Total Current (Max)	SE	MCLK ON	Comments
ADCs On Only	7	3	0.5	23	1	YES	REFOUT Disabled
All Sections On				TBD	1	YES	
REFCAP On Only	0.75	0	0	1.0	0	NO	REFOUT Disabled
REFCAP and REFOUT On Only	3.0	0	0	4.5	0	NO	
All Sections Off	0	0.85	0	1.0	0	YES	MCLK Active Levels Equal to 0 V and DVDD
All Sections Off	0.00	0.007	0	0.04	0	NO	Digital Inputs Static and Equal to 0 V or DVDD

The above values are in mA and are typical values unless otherwise noted.

AD73360–SPECIFICATIONS[1] (AVDD = +5 V ± 10%; DVDD = +5 V ± 10%; DGND = AGND = 0 V, f_{MCLK} = 16.384 MHz, F_S = 64 kHz; T_A = T_{MIN} to T_{MAX}, unless otherwise noted)

Parameter	AD73360A Min	Typ	Max	Units	Test Conditions/Comments
REFERENCE					
REFCAP					
Absolute Voltage, V_{REFCAP}		1.2		V	5VEN = 0
		2.4		V	5VEN = 1
REFCAP TC		50		ppm/°C	0.1 µF Capacitor Required from REFCAP to AGND2
REFOUT					
Typical Output Impedance		68		Ω	
Absolute Voltage, V_{REFOUT}		1.2		V	5VEN = 0, Unloaded
		2.4		V	5VEN = 1, Unloaded
Minimum Load Resistance	2			kΩ	5VEN = 1
Maximum Load Capacitance			100	pF	
ADC SPECIFICATIONS					
Maximum Input Range at VIN[2, 3]		3.156		V p-p	5VEN = 1, Measured Differentially
		3.17		dBm	
Nominal Reference Level at VIN		2.1908		V p-p	5VEN = 1, Measured Differentially
(0 dBm0)		0		dBm	
Absolute Gain					
PGA = 0 dB		0.1		dB	1.0 kHz, 0 dBm0
PGA = 38 dB		–0.5		dB	1.0 kHz, 0 dBm0
Gain Tracking Error		±0.1		dB	1.0 kHz, +3 dBm0 to –50 dBm0
Signal to (Noise + Distortion)					
PGA = 0 dB	70	76		dB	0 Hz to Fs/2; Fs = 8 kHz
				dB	0 Hz to Fs/2; Fs = 16 kHz
				dB	0 Hz to Fs/2; Fs = 32 kHz
				dB	0 Hz to Fs/2; Fs = 64 kHz
PGA = 38 dB	61	65		dB	0 Hz to Fs/2; Fs = 8 kHz
Total Harmonic Distortion					
PGA = 0 dB		–76		dB	
PGA = 38 dB		–69		dB	
Intermodulation Distortion		–69		dB	PGA = 0 dB
Idle Channel Noise		–67		dBm0	PGA = 0 dB
Crosstalk ADC-to-ADC		TBD		dB	ADC1 Input Signal Level: 1.0 kHz, 0 dBm0 ADC2 Input at Idle
DC Offset		+20		mV	PGA = 0 dB
Power Supply Rejection		–55		dB	Input Signal Level at AVDD and DVDD Pins 1.0 kHz, 100 mV p-p Sine Wave
Group Delay[4, 5]		25		µs	64 kHz Output Sample Rate
		TBD		µs	32 kHz Output Sample Rate
		TBD		µs	16 kHz Output Sample Rate
		TBD		µs	8 kHz Output Sample Rate
Input Resistance at VIN[2, 4]		25		kΩ[6]	DMCLK = 16.384 MHz
FREQUENCY RESPONSE					
(ADC)[9] Typical Output					
Frequency (Normalised to F_S)					
0		0		dB	
0.03125		–0.1		dB	
0.0625		–0.25		dB	
0.125		–0.6		dB	
0.1875		–1.4		dB	
0.25		–2.8		dB	
0.3125		–4.5		dB	
0.375		–7.0		dB	
0.4375		–9.5		dB	
> 0.5		< –12.5		dB	

Parameter	AD73322A Min	Typ	Max	Units	Test Conditions/Comments
LOGIC INPUTS					
V_{INH}, Input High Voltage	V_{DD} – 0.8		V_{DD}	V	
V_{INL}, Input Low Voltage	0		0.8	V	
I_{IH}, Input Current		–0.5		µA	
C_{IN}, Input Capacitance		10		pF	
LOGIC OUTPUT					
V_{OH}, Output High Voltage	V_{DD} – 0.4		V_{DD}	V	$\|I_{OUT}\| \leq 100$ µA
V_{OL}, Output Low Voltage	0		0.4	V	$\|I_{OUT}\| \leq 100$ µA
Three-State Leakage Current		–0.3		µA	
POWER SUPPLIES					
AVDD1, AVDD2	4.5		5.5	V	
DVDD	4.5		5.5	V	
I_{DD}[10]					See Table II

NOTES
[1]Operating temperature range is as follows: –40°C to +85°C. Therefore, T_{MIN} = –40°C and T_{MAX} = +85°C.
[2]Test conditions: Input PGA set for 0 dB gain (unless otherwise stated).
[3]At input to sigma-delta modulator of ADC.
[4]Guaranteed by design.
[5]Overall group delay will be affected by the sample rate and the external digital filtering.
[6]The ADC's input impedance is inversely proportional to DMCLK and is approximated by: $(4 \infty 10^{11})$/DMCLK.
[9]Frequency response of ADC measured with input at audio reference level (the input level that produces an output level of –10 dBm0), with 38 dB preamplifier bypassed and input gain of 0 dB.
[10]Test conditions: no load on digital inputs, analog inputs ac coupled to ground.
Specifications subject to change without notice.

Table II. Current Summary (AVDD = DVDD = +5.5 V)

Conditions	Analog Current	Internal Digital Current	External Interface Current	Total Current	SE	MCLK ON	Comments
ADC On Only	8.5	6	2	33.0	1	YES	REFOUT Disabled
All Sections On				TBD	1	YES	
REFCAP On Only	0.8	0	0	0.8	0	NO	REFOUT Disabled
REFCAP and REFOUT On Only	3.5	0	0	3.5	0	NO	
All Sections Off	0	1.5	0	1.5	0	YES	MCLK Active Levels Equal to 0 V and DVDD
All Sections Off	0	0.01	0	0.01	0	NO	Digital Inputs Static and Equal to 0 V or DVDD

The above values are in mA and are typical values unless otherwise noted.

Table III. Signal Ranges

		3 V Power Supply 5VEN = 0	5 V Power Supply 5VEN = 0	5 V Power Supply 5VEN = 1
V_{REFCAP}		1.2 V ± 10%	1.2 V	2.4 V
V_{REFOUT}		1.2 V ± 10%	1.2 V	2.4 V
ADC	Maximum Input Range at V_{IN}	1.578 V p-p	1.578 V p-p	3.156 V p-p
	Nominal Reference Level	1.0954 V p-p	1.0954 V p-p	2.1908 V p-p

TIMING CHARACTERISTICS (AVDD = +3 V ± 10%; DVDD = +3 V ± 10%; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = –40°C to +85°C	Units	Description
Clock Signals			See Figure 1
t_1	61	ns min	MCLK Period
t_2	24.4	ns min	MCLK Width High
t_3	24.4	ns min	MCLK Width Low
Serial Port			See Figures 3 and 4
t_4	t_1	ns min	SCLK Period
t_5	0.4 * t_1	ns min	SCLK Width High
t_6	0.4 * t_1	ns min	SCLK Width Low
t_7	20	ns min	SDI/SDIFS Setup Before SCLK Low
t_8	0	ns min	SDI/SDIFS Hold After SCLK Low
t_9	10	ns max	SDOFS Delay From SCLK High
t_{10}	10	ns min	SDOFS Hold After SCLK High
t_{11}	10	ns min	SDO Hold After SCLK High
t_{12}	10	ns max	SDO Delay From SCLK High
t_{13}	30	ns max	SCLK Delay from MCLK

TIMING CHARACTERISTICS (AVDD = +5 V ± 10%; DVDD = +5 V ± 10%; AGND = DGND = 0 V; $T_A = T_{MIN}$ to T_{MAX}, unless otherwise noted)

Parameter	Limit at T_A = –40°C to +85°C	Units	Description
Clock Signals			See Figure 1
t_1	61	ns min	MCLK Period
t_2	24.4	ns min	MCLK Width High
t_3	24.4	ns min	MCLK Width Low
Serial Port			See Figures 3 and 4
t_4	t_1	ns min	SCLK Period
t_5	0.4 * t_1	ns min	SCLK Width High
t_6	0.4 * t_1	ns min	SCLK Width Low
t_7	20	ns typ	SDI/SDIFS Setup Before SCLK Low
t_8	0	ns typ	SDI/SDIFS Hold After SCLK Low
t_9	10	ns typ	SDOFS Delay From SCLK High
t_{10}	10	ns typ	SDOFS Hold After SCLK High
t_{11}	10	ns typ	SDO Hold After SCLK High
t_{12}	10	ns typ	SDO Delay From SCLK High
t_{13}	30	ns typ	SCLK Delay from MCLK

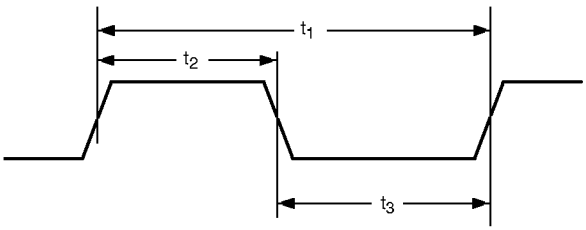


Figure 1. MCLK Timing

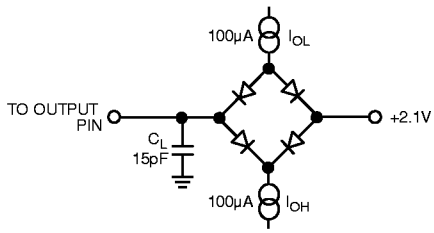


Figure 2. Load Circuit for Timing Specifications

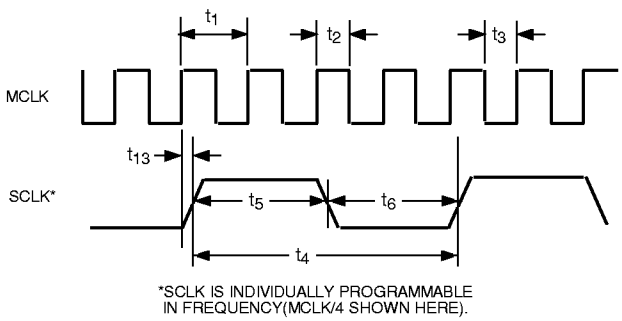


Figure 3. SCLK Timing

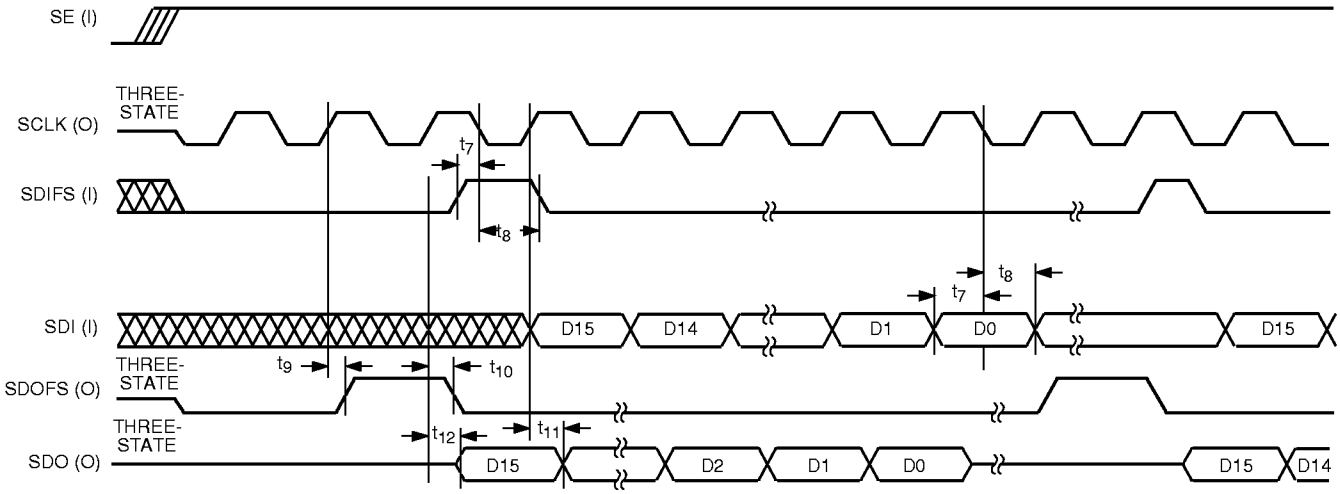


Figure 4. Serial Port (SPORT)

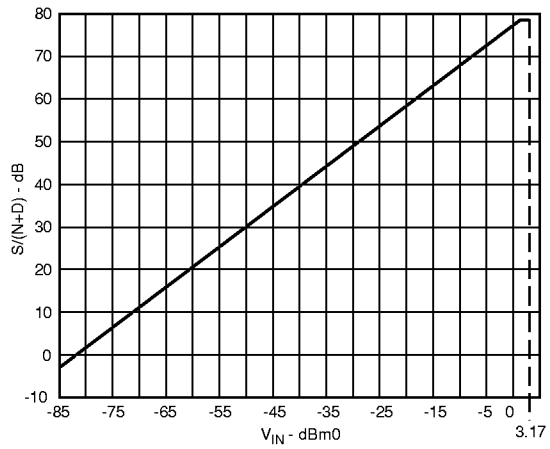


Figure 5a. S/(N+D) vs. V_{IN} (ADC @ 3 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

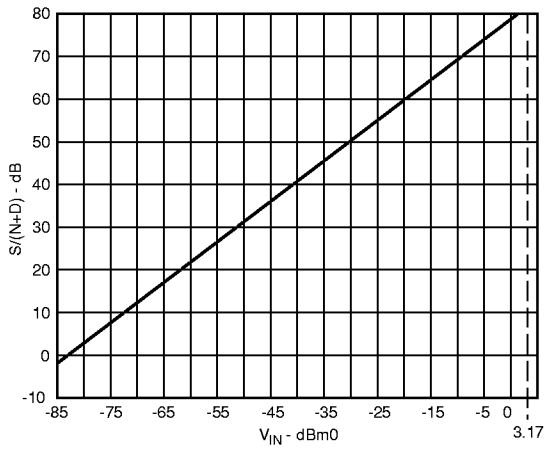


Figure 5b. S/(N+D) vs. V_{IN} (ADC @ 5 V) over Voiceband Bandwidth (300 Hz – 3.4 kHz)

ABSOLUTE MAXIMUM RATINGS*
(T_A = +25°C unless otherwise noted)

AVDD, DVDD to GND ..... –0.3 V to +7 V
AGND to DGND ..... –0.3 V to +0.3 V
Digital I/O Voltage to DGND ..... –0.3 V to DVDD + 0.3 V
Analog I/O Voltage to AGND ..... –0.3 V to AVDD + 0.3 V
Operating Temperature Range
Industrial (A Version) ..... –40°C to +85°C
Storage Temperature Range ..... –65°C to +150°C
Maximum Junction Temperature ..... +150°C
SOIC, θ_{JA} Thermal Impedance ..... 75°C/W
Lead Temperature, Soldering
Vapor Phase (60 sec) ..... +215°C
Infrared (15 sec) ..... +220°C

*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ORDERING GUIDE

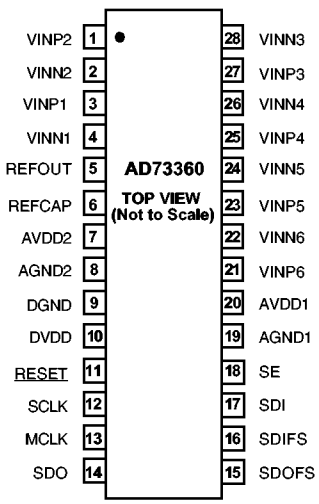
Model	Temperature Range	Package Option
AD73360AR	–40°C to +85°C	R-28[1]
AD73360AS	–40°C to +85°C	S-44[2]
EVAL-AD73360EB	Evaluation Board[3] +EZ-Kit Lite Upgrade[4]	
EVAL-AD73360EZ	Evaluation Board[3] +EZ-Kit Lite[5]	

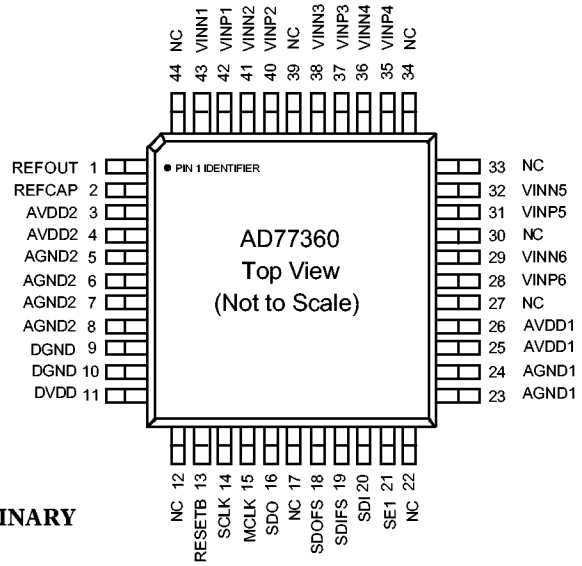
NOTES
[1]R = 0.3' Small Outline IC (SOIC).
[2]S = Plastic Quad Flat Pack IC (PQFP).
[3]The AD73322 evaluation board features a selectable number of codecs in cascade (from 1 to 4). It can be interfaced to an ADSP-2181 EZ-KIT Lite or to a Texas Instruments EVM kit.
[4]The upgrade consists of a connector for the expansion port P3 of the EZKIT-Lite. This option is intended for existing owners of EZ-Kit Lite.
[5]The EZ-Kit Lite has been modified to allow it to interface with the AD73322 evaluation board. This option is intended for users who do not already have an EZ-Kit Lite.

CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the AD73322 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION





PRELIMINARY

PIN FUNCTION DESCRIPTION

Mnemonic	Function
VINP1	Analog Input to the Positive Terminal of Input Channel 1.
VINN1	Analog Input to the Negative Terminal of Input Channel 1.
VINP2	Analog Input to the Positive Terminal of Input Channel 2.
VINN2	Analog Input to the Negative Terminal of Input Channel 2.
VINP3	Analog Input to the Positive Terminal of Input Channel 3.
VINN3	Analog Input to the Negative Terminal of Input Channel 3.
VINP4	Analog Input to the Positive Terminal of Input Channel 4.
VINN4	Analog Input to the Negative Terminal of Input Channel 4.
VINP5	Analog Input to the Positive Terminal of Input Channel 5.
VINN5	Analog Input to the Negative Terminal of Input Channel 5.
VINP6	Analog Input to the Positive Terminal of Input Channel 6.
VINN6	Analog Input to the Negative Terminal of Input Channel 6.
REFOUT	Buffered Reference Output, which has a nominal value of 1.2 V or 2.4 V, the value being dependent on the status of Bit 5VEN (CRC:7).
REFCAP	A Bypass Capacitor to AGND2 of 0.1 μF is required for the on-chip reference. The capacitor should be fixed to this pin.
AVDD2	Analog Power Supply Connection.
AGND2	Analog Ground/Substrate Connection.
DGND	Digital Ground/Substrate Connection.
DVDD	Digital Power Supply Connection.
$\overline{\text{RESET}}$	Active Low Reset Signal. This input resets the entire chip, resetting the control registers and clearing the digital circuitry.
SCLK	Output Serial Clock whose rate determines the serial transfer rate to/from the codec. It is used to clock data or control information to and from the serial port (SPORT). The frequency of SCLK is equal to the frequency of the master clock (MCLK) divided by an integer number—this integer number being the product of the external master clock rate divider and the serial clock rate divider.
MCLK	Master Clock Input. MCLK is driven from an external clock signal.
SDO	Serial Data Output of the Codec. Both data and control information may be output on this pin and is clocked on the positive edge of SCLK. SDO is in three-state when no information is being transmitted and when SE is low.
SDOFS	Framing Signal Output for SDO Serial Transfers. The frame sync is one-bit wide and it is active one SCLK period before the first bit (MSB) of each output word. SDOFS is referenced to the positive edge of SCLK. SDOFS is in three-state when SE is low.
SDIFS	Framing Signal Input for SDI Serial Transfers. The frame sync is one-bit wide and it is valid one SCLK period before the first bit (MSB) of each input word. SDIFS is sampled on the negative edge of SCLK and is ignored when SE is low.
SDI	Serial Data Input of the Codec. Both data and control information may be input on this pin and are clocked on the negative edge of SCLK. SDI is ignored when SE is low.
SE	SPORT Enable. Asynchronous input enable pin for the SPORT. When SE is set low by the DSP, the output pins of the SPORT are three-stated and the input pins are ignored. SCLK is also disabled internally in order to decrease power dissipation. When SE is brought high, the control and data registers of the SPORT are at their original values (before SE was brought low), however the timing counters and other internal registers are at their reset values.
AGND1	Analog Ground Connection.
AVDD1	Analog Power Supply Connection.

TERMINOLOGY

Absolute Gain
Absolute gain is a measure of converter gain for a known signal. Absolute gain is measured (differentially) with a 1 kHz sine wave at 0 dBm0 for each ADC. The absolute gain specification is used for gain tracking error specification.

Crosstalk
Crosstalk is due to coupling of signals from a given channel to an adjacent channel. It is defined as the ratio of the amplitude of the coupled signal to the amplitude of the input signal. Crosstalk is expressed in dB.

Gain Tracking Error
Gain tracking error measures changes in converter output for different signal levels relative to an absolute signal level. The absolute signal level is 0 dBm0 (equal to absolute gain) at 1 kHz for each ADC. Gain tracking error at 0 dBm0 (ADC) is 0 dB by definition.

Group Delay
Group Delay is defined as the derivative of radian phase with respect to radian frequency, dø(f)/df. Group delay is a measure of average delay of a system as a function of frequency. A linear system with a constant group delay has a linear phase response. The deviation of group delay from a constant indicates the degree of nonlinear phase response of the system.

Idle Channel Noise
Idle channel noise is defined as the total signal energy measured at the output of the device when the input is grounded (measured in the frequency range 300 Hz–3400 Hz).

Intermodulation Distortion
With inputs consisting of sine waves at two frequencies, fa and fb, any active device with nonlinearities will create distortion products at sum and difference frequencies of mfa ± nfb where m, n = 0, 1, 2, 3, etc. Intermodulation terms are those for which neither m nor n are equal to zero. For final testing, the second order terms include (fa + fb) and (fa – fb), while the third order terms include (2fa + fb), (2fa – fb), (fa + 2fb) and (fa – 2fb).

Power Supply Rejection
Power supply rejection measures the susceptibility of a device to noise on the power supply. Power supply rejection is measured by modulating the power supply with a sine wave and measuring the noise at the output (relative to 0 dB).

Sample Rate
The sample rate is the rate at which each ADC updates its output register. It is set relative to the DMCLK and the programmable sample rate setting.

SNR+THD
Signal-to-noise ratio plus harmonic distortion is defined to be the ratio of the rms value of the measured input signal to the rms sum of all other spectral components in the frequency range 300 Hz–3400 Hz, including harmonics but excluding dc.

ABBREVIATIONS

ADC	Analog-to-Digital Converter.
ALB	Analog Loop-Back.
BW	Bandwidth.
CRx	A Control Register where *x* is a placeholder for an alphabetic character (A–E). There are five read/write control registers on the AD73322—designated CRA through CRE.
CRx:n	A bit position, where *n* is a placeholder for a numeric character (0–7), within a control register; where *x* is a placeholder for an alphabetic character (A–E). Position 7 represents the MSB and Position 0 represents the LSB.
DGT	Digital Gain Tap
DLB	Digital Loop-Back.
DMCLK	Device (Internal) Master Clock. This is the internal master clock resulting from the external master clock (MCLK) being divided by the on-chip master clock divider.
FSLB	Frame Sync Loop Back—where the SDOFS of the final device in a cascade is connected to the RFS and TFS of the DSP and the SDIFS of first device in the cascade. Data input and output occur simultaneously. In the case of Non-FSLB, SDOFS and SDO are connected to the Rx Port of the DSP while SDIFS and SDI are connected to the Tx Port.
PGA	Programmable Gain Amplifier.
SC	Switched Capacitor.
SNR	Signal-to-Noise Ratio.
SPORT	Serial Port.
THD	Total Harmonic Distortion.
VBW	Voice Bandwidth.

Table XI. Control Register Map

Address (Binary)	Name	Description	Type	Width	Reset Setting (Hex)
000	CRA	Control Register A	R/W	8	0x00
001	CRB	Control Register B	R/W	8	0x00
010	CRC	Control Register C	R/W	8	0x00
011	CRD	Control Register D	R/W	8	0x00
100	CRE	Control Register E	R/W	8	0x00
101	CRF	Control register F	R/W	8	0x00

Table XII. Control Word Description

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C/$\overline{D}$	R/$\overline{W}$	DEVICE ADDRESS			REGISTER ADDRESS			REGISTER DATA							

Control	Frame	Description
Bit 15	Control/Data	When set high, it signifies a control word in Program or Mixed Program/Data Modes. When set low, it signifies a data word in Mixed Program/Data Mode or an invalid control word in Program Mode.
Bit 14	Read/Write	When set low, it tells the device that the data field is to be written to the register selected by the register field setting provided the address field is zero. When set high, it tells the device that the selected register is to be written to the data field in the input serial register and that the new control word is to be output from the device via the serial output.
Bit 13–11	Device Address	This 3-bit field holds the address information. Only when this field is zero is a device selected. If the address is not zero, it is decremented and the control word is passed out of the device via the serial output.
Bits 10–8	Register Address	This 3-bit field is used to select one of the five control registers on the AD73322.
Bits 7–0	Register Data	This 8-bit field holds the data that is to be written to or read from the selected register provided the address field is zero.

Table XIII. Control Register A Description

CONTROL REGISTER A

7	6	5	4	3	2	1	0
RESET	DC2	DC1	DC0	SLB	DLB	MM	DATA/$\overline{\text{PGM}}$

Bit	Name	Description
0	DATA/PGM	Operating Mode (0 = Program; 1 = Data Mode)
1	MM	Mixed Mode (0 = Off; 1 = Enabled)
2	DLB	Digital Loop-Back Mode (0 = Off; 1 = Enabled)
3	SLB	SPORT Loop-Back Mode (0 = Off; 1 = Enabled)
4	DC0	Device Count (Bit 0)
5	DC1	Device Count (Bit 1)
6	DC2	Device Count (Bit 2)
7	RESET	Software Reset (0 = Off; 1 = Initiates Reset)

Table XIV. Control Register B Description

CONTROL REGISTER B

7	6	5	4	3	2	1	0
CEE	MCD2	MCD1	MCD0	SCD1	SCD0	DIR1	DIR0

Bit	Name	Description
0	DIR0	Decimation/Interpolation Rate (Bit 0)
1	DIR1	Decimation/Interpolation Rate (Bit 1)
2	SCD0	Serial Clock Divider (Bit 0)
3	SCD1	Serial Clock Divider (Bit 1)
4	MCD0	Master Clock Divider (Bit 0)
5	MCD1	Master Clock Divider (Bit 1)
6	MCD2	Master Clock Divider (Bit 2)
7	CEE	Control Echo Enable (0 = Off; 1 = Enabled)

Table XV. Control Register C Description

CONTROL REGISTER C

7	6	5	4	3	2	1	0
5VEN	RU	PUREF	-	-	-	-	PU

Bit	Name	Description
0	PU	Power-Up Device (0 = Power Down; 1 = Power On)
1	Reserved	Must be programmed to zero (0)
2	Reserved	Must be programmed to zero (0)
3	Reserved	Must be programmed to zero (0)
4	Reserved	Must be programmed to zero (0)
5	PUREF	REF Power (0 = Power Down; 1 = Power On)
6	RU	REFOUT Use (0 = Disable REFOUT; 1 = Enable REFOUT)
7	5VEN	Enable 5 V Operating Mode (0 = Disable 5 V Mode; 1 = Enable 5 V Mode)

Table XVI. Control Register D Description

CONTROL REGISTER D

7	6	5	4	3	2	1	0
PUADC2	IGADC2-2	IGADC2-1	IGADC2-0	PUADC1	IGADC1-2	IGADC1-1	IGADC1-0

Bit	Name	Description
0	IGADC1-0	ADC1:Input Gain Select (Bit 0)
1	IGADC1-1	ADC1:Input Gain Select (Bit 1)
2	IGADC1-2	ADC1:Input Gain Select (Bit 2)
3	PUADC1	Power Control (ADC1); 1 = ON, 0 = OFF
4	IGADC2-0	ADC2:Input Gain Select (Bit 0)
5	IGADC2-1	ADC2:Input Gain Select (Bit 1)
6	IGADC2-2	ADC2:Input Gain Select (Bit 2)
7	PUADC2	Power Control (ADC2); 1 = ON, 0 = OFF

Table XVII. Control Register E Description

CONTROL REGISTER E

7	6	5	4	3	2	1	0
PUADC4	IGADC4-2	IGADC4-1	IGADC4-0	PUADC3	IGADC3-2	IGADC3-1	IGADC3-0

Bit	Name	Description
0	IGADC3-0	ADC3:Input Gain Select (Bit 0)
1	IGADC3-1	ADC3:Input Gain Select (Bit 1)
2	IGADC3-2	ADC3:Input Gain Select (Bit 2)
3	PUADC3	Power Control (ADC3); 1 = ON, 0 = OFF
4	IGADC4-0	ADC4:Input Gain Select (Bit 0)
5	IGADC4-1	ADC4:Input Gain Select (Bit 1)
6	IGADC4-2	ADC4:Input Gain Select (Bit 2)
7	PUADC4	Power Control (ADC4); 1 = ON, 0 = OFF

Table XVIII. Control Register F Description

CONTROL REGISTER F

7	6	5	4	3	2	1	0
PUADC6	IGADC6-2	IGADC6-1	IGADC6-0	PUADC5	IGADC5-2	IGADC5-1	IGADC5-0

Bit	Name	Description
0	IGADC5-0	ADC5:Input Gain Select (Bit 0)
1	IGADC5-1	ADC5:Input Gain Select (Bit 1)
2	IGADC5-2	ADC5:Input Gain Select (Bit 2)
3	PUADC5	Power Control (ADC5); 1 = ON, 0 = OFF
4	IGADC6-0	ADC6:Input Gain Select (Bit 0)
5	IGADC6-1	ADC6:Input Gain Select (Bit 1)
6	IGADC6-2	ADC6:Input Gain Select (Bit 2)
7	PUADC6	Power Control (ADC6); 1 = ON, 0 = OFF