AK4315

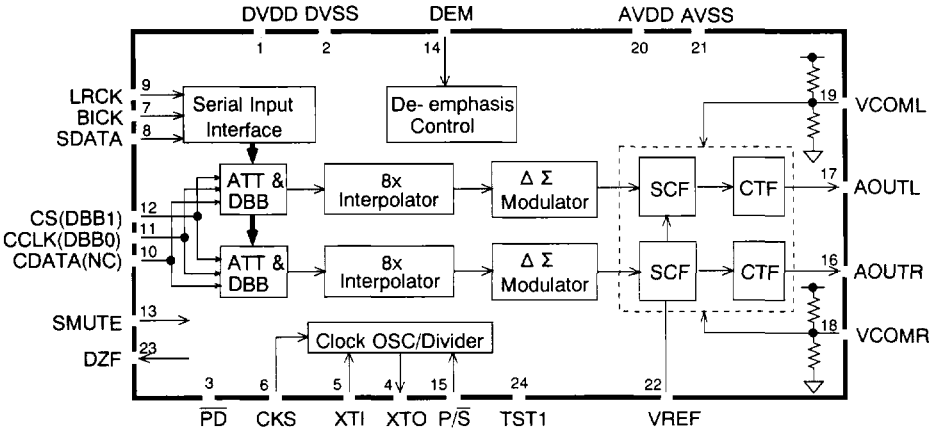
Low Power 16Bit Δ Σ DAC with Digital DBB

General Description

The AK4315 is a low power 1bit stereo DAC with Digital DBB(Dynamic Bass Boost) for multimedia audio system and also includes 16bit digital filter and analog LPF. A 1bit DAC can achieve monotonicity and low distortion with no adjustment and is superior to traditional R- 2R ladder based DACs. In the AK4315, the loss of accuracy from clock jitter is also improved by using SCF techniques for on- chip post filter. The AK4315 includes continuous time filter with single end output and does not need any external parts. The AK4315 also has digital attenuator with 0.75dB step and is suitable for the portable audio systems like MD, etc.

Features

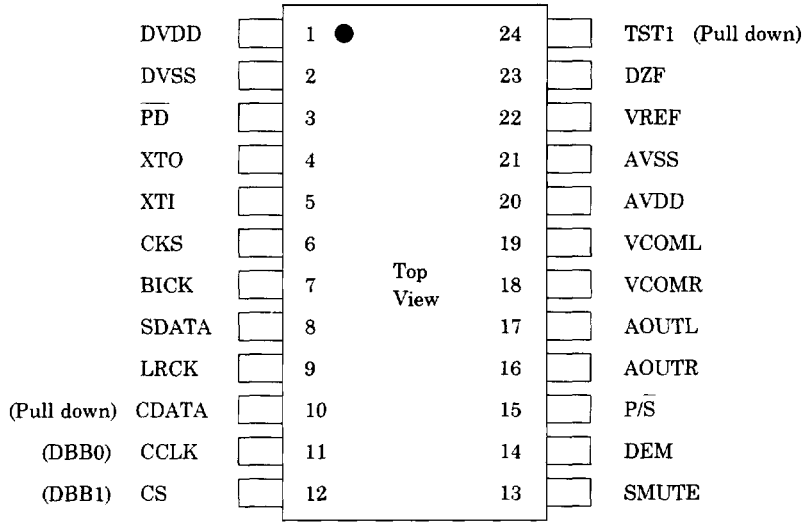
- ☐ Sampling Rate Ranging from 30kHz to 50kHz
- ☐ On chip Perfect filtering 8 times FIR Interpolator, SCF & CTF
- ☐ On chip Buffer with Single End Output
- ☐ Digital de- emphasis for 44.1kHz sampling
  (In serial mode control, De- emphasis of 32, 44.1, 48kHz sampling can be enable.)
- ☐ On chip Digital DBB(Dynamic Bass Boost)
- ☐ On chip digital LOG attenuator
- ☐ Soft Mute
- ☐ Master Clock: 256fs/384fs
- ☐ High Tolerance to Clock Jitter
- ☐ Dynamic Range: 91dB
- ☐ Low Voltage Operation: 2.7V ~ 3.6V
- ☐ Low Power Dissipation: 24mW(@3V)



■ Ordering Guide

AK4315-VF	-10 ~ +70 ℃	24pin VSOP(0.65mm pitch)
AKD4315	Evaluation Board	

■ Pin Layout



PIN/FUNCTION

No.	Pin Name	I/O	Function
1	DVDD	-	Digital Power Supply Pin
2	DVSS	-	Digital Ground Pin
3	$\overline{PD}$	I	Power-Down Pin When at "L", the AK4315 is in power-down mode and is held in reset. The AK4315 should always be reset upon power-up.
4	XTO	O	Crystal Oscillator Output Pin When an external clock is input, this pin should be left floating.
5	XTI	I	Master Clock Input Pin A crystal can be connected between this pin and XTO, or an external CMOS clock can be input on XTI.
6	CKS	I	Master Clock Select Pin "L": XTI=256fs, "H":XTI=384fs
7	BICK	I	Serial Bit Input Clock Pin This clock is used to latch audio data.
8	SDATA	I	Audio Data Input Pin 2's complement MSB-first data is input on this pin.
9	LRCK	I	L/R Clock Pin This input determines which audio channel is currently being input on SDATA pin. "H": Lch, "L": Rch
10	CDATA	I	Control Data Input Pin
11	CCLK	I	Control Clock Input Pin
12	CS	I	Chip Select Pin (Serial mode control)
10	(NC)	I	Must be left floating or tied to AVSS. (Pull-down pin)
11	(DBB0)	I	DBB0 and DBB1 pins select one of the four kind modes for Digital
12	(DBB1)	I	DBB (Parallel mode control)
13	SMUTE	O	Soft Mute Pin When this pin goes "H", soft mute cycle is initiated.
14	DEM	I	De-emphasis Enable Pin When "H", De-emphasis of fs=44.1kHz is enabled.
15	P/S	I	Parallel/Serial Mode Select Pin "H": Parallel mode, "L": Serial mode
16	AOUTR	O	Rch Analog Output Pin
17	AOUTL	O	Lch Analog Output Pin
18	VCOMR	O	Rch Common Voltage pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic cap.
19	VCOML	O	Lch Common Voltage pin, AVDD/2 Normally connected to AVSS with a 0.1uF ceramic capacitor in parallel with a 10uF electrolytic cap.
20	AVDD	-	Analog Power Supply Pin
21	AVSS	-	Analog Ground Pin
22	VREF	I	Voltage Reference Input Pin The differential Voltage between this pin and AVSS sets the analog output range. Normally connected to AVSS with a 0.1uF ceramic capacitor.

23	DZF	O	Zero Input Detect Pin When SDATA of both channels follow a total 8192 LRCK cycles with "0" input data, this pin goes "H".
24	TST1	I	Test Pin (Pull-down pin) Must be left floating or tied to AVSS.

ABSOLUTE MAXIMUM RATINGS

(AVSS,DVSS=0V; Note 1)

Parameter	Symbol	min	max	Units
Power Supplies: Analog (AVDD pin)	AVDD	-0.3	6.0	V
Digital (DVDD pin)	DVDD	-0.3	AVDD+0.3 or 6.0	V
Input Current, Any Pin Except Supplies	IIN	-	± 10	mA
Input Voltage	VIND	-0.3	AVDD+0.3 or 6.0	V
Ambient Operating Temperature	Ta	-10	70	℃
Storage Temperature	Tstg	-65	150	℃

Note: 1 . All voltages with respect to ground.

WARNING: Operation at or beyond these limits may result in permanent damage to the device.
Normal operation is not guaranteed at these extremes.

RECOMMENDED OPERATING CONDITIONS

(AVSS,DVSS=0V; Note 1)

Parameter		Symbol	min	typ	max	Units
Power Supplies: Analog	(AVDD pin)	AVDD	2.7	3.0	3.6	V
Digital	(DVDD pin)	DVDD	2.7	3.0	AVDD	V
Voltage Reference	(Note 2)	VREF	2.3	-	AVDD	V

Notes: 1 . All voltages with respect to ground.
2 . Analog output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)= 1.58Vpp*VREF/3

* AKM assumes no responsibility for the usage beyond the conditions in this data sheet.

ANALOG CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=3.0V; VREF=AVDD; fs=44.1kHz; Signal Frequency=1kHz;
Digital DBB=off, $R_L \geqq 10k\ \Omega$; Measurement Bandwidth=10Hz ~ 20kHz;
unless otherwise specified)

Parameter	min	typ	max	Units
Dynamic Characteristics (Note 3)				
THD+N		-84	-70	dB
Dynamic Range (A-Weighted)	86	91		dB
S/N (A-Weighted)	86	91		dB
Interchannel Isolation	90	100		dB
DC Accuracy				
Interchannel Gain Mismatch		0.1	0.3	dB
Gain Drift		60		ppm/℃
Analog Output				
Output Voltage (Note 4)	1.48	1.58	1.68	Vpp
Load Resistance	10			k Ω
Power Supplies				
Power Supply Current (Note 5)				
Normal Operation (PD="H")				
AVDD+DVDD		8	12	mA
Power-Down-Mode (PD="L")				
AVDD+DVDD (Note 6)		10	50	uA
Power Dissipation				
Normal Operation		24	36	mW
Power-Down-Mode (Note 6)		30	150	uW
Power Supply Rejection	-	50	-	dB

Notes: 3 . Measured by AD725C(SHIBASOKU). Averaging mode.

4 . Full-scale voltage(0dB). Output voltage scales with the voltage of VREF.
AOUT(typ.@0dB)= 1.58Vpp*VREF/3.

5 . XTO pin is open.

6 . Power Dissipation in the power-down mode is applied with no external clocks (XTI,BICK,LRCK held "H" or "L").
When X'tal OSC is connected between XTI pin and XTO pin, the oscillation can not be guaranteed at power-down mode. If the oscillation is required at power-down mode, the resistor of 100k ~ 1M ohms should be connected between XTI pin and XTO pin. In this case, the AK4315 may draw the current of about 1mA.

FILTER CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=2.7 ~ 3.6V; fs=44.1kHz)

Parameter		Symbol	min	typ	max	Units
Digital Filter						
Passband	-0.1dB (Note 7)	PB	0		20.0	kHz
	-6.0dB		-	22.05	-	kHz
Stopband	(Note 7)	SB	24.1			kHz
Passband Ripple		PR			± 0.06	dB
Stopband Attenuation		SA	43			dB
Group Delay	(Note 8)	GD	-	16.1	-	1/fs
Digital Filter + Analog Filter						
Frequency Response	0 ~ 20.0kHz		-	± 0.5	-	dB

Note: 7 . The passband and stopband frequencies scale with fs.
For example, PB=0.4535*fs(@-0.1dB), SB=0.546*fs(@-43dB).

8 . The calculating delay time which occurred by digital filtering. This time is from setting the 16bit data of both channels to input resistor to the output of analog signal.

DIGITAL CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=2.7 ~ 3.6V)

Parameter	Symbol	min	typ	max	Units
High-Level Input Voltage	VIH	70%DVDD	-	-	V
Low-Level Input Voltage	VIL	-	-	30%DVDD	V
Input Voltage at AC coupling(XTI pin)	VAC	1	-	-	Vpp
High-Level Output Voltage Iout=-3mA	VOH	DVDD-0.6	-	-	V
Low-Level Output Voltage Iout=3mA	VOL	-	-	0.6	V
Input Leakage Current (Note 9)	Iin	-	-	± 10	uA

Note: 9 . CDATA,TST1 pins have internal pull-down devices. (typ. 200k Ω)

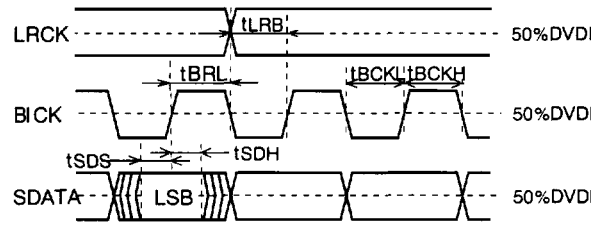
SWITCHING CHARACTERISTICS

(Ta=25 ℃ ; AVDD,DVDD=2.7 ~ 3.6V; CL=20pF)

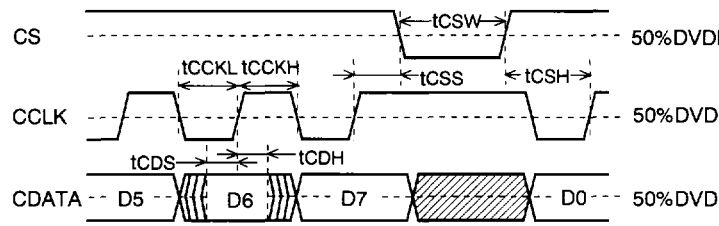
Parameter	Symbol	min	typ	max	Unit
Master Clock Frequency					
Crystal Resonator 256fs:	fCLK	7.68	11.2896	12.8	MHz
Crystal Resonator 384fs:	fCLK	11.52	16.9344	19.2	MHz
External Clock 256fs:	fCLK	7.68	11.2896	12.8	MHz
Pulse Width Low	tCLKL	28			ns
Pulse Width High	tCLKH	28			ns
External Clock 384fs:	fCLK	11.52	16.9344	19.2	MHz
Pulse Width Low	tCLKL	23			ns
Pulse Width High	tCLKH	23			ns
LRCK Frequency	fs	30	44.1	50	kHz
Audio Interface Timing (Note 10)					
BICK Period	tBCK	312.5			ns
BICK Pulse Width Low	tBCKL	100			ns
Pulse Width High	tBCKH	100			ns
LRCK Edge to BICK rising (Note 11)	tLRB	50			ns
BICK rising to LRCK Edge (Note 11)	tBRL	50			ns
SDATA Setup Time	tSDS	70			ns
SDATA Hold Time	tSDH	50			ns
Control Interface Timing (Note 12)					
CCLK Pulse Width Low	tCCKL	100			ns
Pulse Width High	tCCKH	100			ns
CDATA Latch Hold Time	tCDS	50			ns
CDATA Latch Setup Time	tCDH	50			ns
CS Pulse Width Low	tCSW	100			ns
CCLK to CS falling	tCSS	50			ns
CS rising to CCLK	tCSH	50			ns
Reset Timing					
PD Pulse Width (Note 13)	tRST	100			ns

Notes: 10. Refer to the operating overview section "Audio Data Interface".
11. BICK rising edge must not occur at the same time as LRCK edge.
12. Refer to the operating overview section "Serial Mode Control".
13. The AK4315 can be reset by bringing PD "L" to "H" only upon power up.

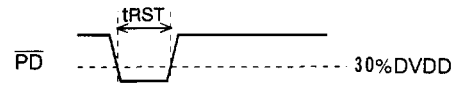
■ Timing Diagram



Audio Data Input Timing



Mode Control Timing



Reset Timing

OPERATION OVERVIEW

■ System Clock Input

The external clocks which are required to operate the AK4315 are XTI(256fs/384fs), LRCK(fs), BICK(32fs ~). The master clock (XTI) should be synchronized with LRCK but the phase is free of care. The XTI is used to operate the digital interpolation filter and the delta-sigma modulator. The frequency of XTI is determined by the sampling rate(LRCK), and the setting of the Clock Select, CKS pin. Setting CKS "L" selects an XTI frequency of 256fs while setting CKS "H" selects 384fs. When the 384fs is selected, the internal master clock becomes 256fs(=384fs*2/3).
*fs is audio word rate.

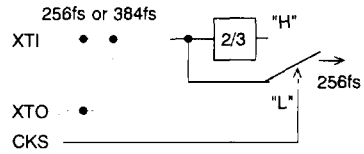


Figure 1. Internal Clock Circuit

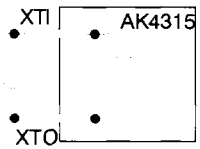


Figure 2. Crystal resonator connection

The master clock can be either a crystal resonator placed across the XTI and XTO pins, or external clock input to the XTI pin with the XTO pin left floating. Not only CMOS clock but sine wave signal with 1Vpp can be input to the XTI pin by AC coupling. Table 1 illustrates standard audio word rates and corresponding frequencies used in the DAC. When X'tal OSC is connected between XTI pin and XTO pin, the oscillation by x'tal can not guaranteed at power-down mode. If the oscillation is required at power-down mode, the resistor of 100k ~ 1M ohms(Table 1) should be connected between XTI pin and XTO pin.
The load capacitor of XTO pin is 20pF(Max.).
The load capacitor connecting XTO pin should be considered its value and the internal capacitor of the crystal resonator.
In this case, the AK4315 may draw the current of about 1mA.

LRCK(fs) (kHz)	CKS	XTI (MHz)
32.0	L	8.1920
	H	12.2880
44.1	L	11.2896
	H	16.9344
48.0	L	12.2880
	H	18.4320

Table 2. Examples of System Clock

All external clocks(XTI,BICK,LRCK) should always be present whenever the AK4315 is in normal operation mode(PD="H"). If these clocks are not provided, the AK4315 may draw excess current and do not possibly operate properly because the device utilizes dynamic refreshed logic internally. If the external clocks are not present, the AK4315 should be in the power-down mode(PD="L").

■ Audio Data Interface

The AK4315 has three serial input pins(SDATA, BICK, LRCK). Data bits is clocked into the AK4315 via SDATA pin and is latched by LRCK. The data format is MSB-first, 2's complement and LSB justified.

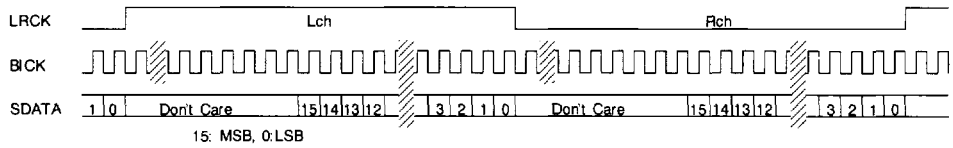


Figure 3. Audio Data Input Format

■ Parallel/Serial Mode Control

When P/$\overline{S}$ pin goes "H", the AK4315 becomes parallel mode, Digital DBB mode can be selected by DBB0 pin and DBB1 pin. When P/$\overline{S}$ pin goes "L", the AK4315 becomes serial mode. In this mode, the functions of DBB0 pin, DBB1 pin and NC pin are redefined to CCLK pin, CS pin and CDATA pin.

■ De-emphasis filter

The AK4315 includes the digital de-emphasis filter(tc=50/15us) by IIR filter. This filter corresponds to three sampling frequencies(32kHz,44.1kHz,48kHz). De-emphasis is enabled by the following two ways.

1. Way of using DEM pin

Only one de-emphasis(fs=44.1kHz) set initially can be controlled by DEM pin at resetting. The de-emphasis is enabled by setting DEM pin "H". When the frequency of de-emphasis is set by FS0, FS1 of serial mode control bits, the corresponding de-emphasis can be enabled. In this case, DEM bit in the serial mode control should be "0".

2. Way of using serial mode control

DEM pin should be open or "L". In this case, The de-emphasis corresponding to fs=32kHz, 44.1kHz, 48kHz can be controlled by DEM, FS0 and FS1 in the serial mode control bits.

■ Digital DBB(Dynamic Bass Boost) Mode

The Digital DBB mode in the AK4315 has the four kind modes(off, min, mid, max). The Digital DBB mode is enabled by the following two ways.

1. Parallel mode control

The Digital DBB mode can be selected by DBB0 pin and DBB1 pin.

2. Serial mode control

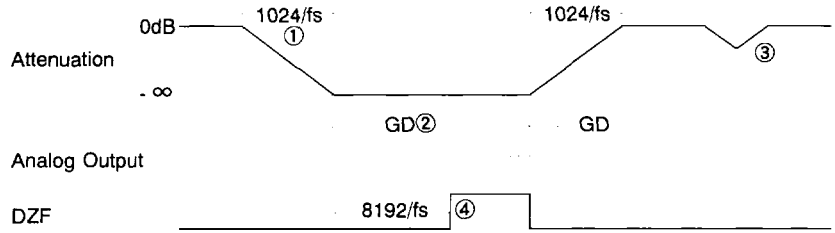
The Digital DBB mode can be selected by DBB0 bit and DBB1 bit in the serial control data.

■ Zero detection

When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".

■ Soft mute operation

Soft mute operation is performed at digital domain. When SMUTE goes "H", the output signal is attenuated by - ∞ during 1024 LRCK cycles. When SMUTE is returned to "L", the mute is cancelled and the output attenuation gradually changes to 0dB during 1024 LRCK cycles. If the soft mute is cancelled within 1024 LRCK cycles after starting the operation, the attenuation is discontinued and returned to 0dB. The soft mute is effective for changing the signal source without stopping the signal transmission.



Notes:

① The output signal is attenuated by - ∞ during 1024 LRCK cycles(1024/fs).

② Analog output corresponding to digital input have the group delay(GD).

③ If the soft mute is cancelled within 1024 LRCK cycles, the attenuation is discontinued and returned to 0dB.

④ When the input data at both channels are continuously zeros for 8192 LRCK cycles, DZF goes to "H". DZF immediately goes "L" if input data are not zero after going DZF "H".

Figure 4. Soft mute and zero detection

■ Serial Mode Control

The AK4315 can control Digital DBB mode, attenuation level, de-emphasis mode and soft mute via the serial control interface. The serial data consists of 8bit. (See the Table 3 and Figure 6.)

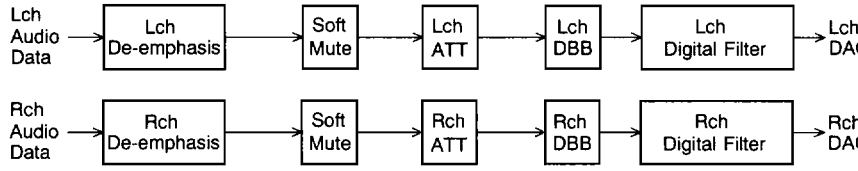


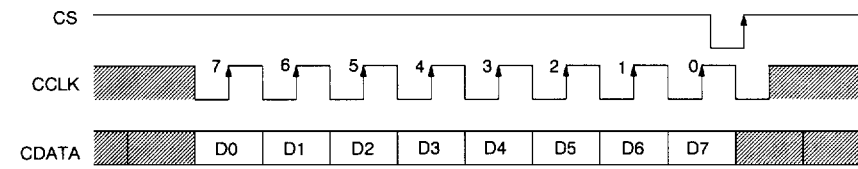
Figure 5. Internal Configuration of AK4315

Serial Data	Control Signal	
D0	0	1
D1	ATT0	DEM
D2	ATT1	FS0
D3	ATT2	FS1
D4	ATT3	DBB0
D5	ATT4	DBB1
D6	ATT5	SMUTE
D7	ATT6	Not use

*When power-down mode and reset mode, D0 is "0".
ATT0 ~ 6:ATT.Level(ATT0=LSB,ATT6=MSB);7FH at RESET
DEM: De-emphasis control ; 0 at RESET
FS0,FS1: fs Control for de-emphasis filter; 00 at RESET
DBB0,DBB1: Digital DBB control ; 00 at RESET

SMUTE: Soft mute control ; 0 at RESET

Table 3.Serial mode bit



Note: CCLK should be held "H" or "L" except writing to ATT & mode registers in order to avoid the performance degradation.

Figure 6. Serial mode control timing

1 . Attenuator Operation

The attenuator sets common attenuation level for both L/R channels. The step size is 0.75dB and the control ranges from 0dB to -90dB. The change between ATT setting is direct transition, not soft transition. When the ATT register is set only all "0", the soft mute operation is performed during 1024LRCK cycles. Once the ATT register is set not 00H, the soft mute condition is cancelled and it takes 1024LRCK cycles to set the ATT level. When resetting, ATT value is set 7FH.

ATT0	ATT1	ATT2	ATT3	ATT4	ATT5	ATT6	(HEX)	Level
1	1	1	1	1	1	1	(7FH)	0dB
0	1	1	1	1	1	1	(7EH)	-0.75dB
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	0	0	0	0	(07H)	-90.0dB
×	×	×	0	0	0	0	⋮	≦ -90.0dB
0	0	0	0	0	0	0	(00H)	Mute(- ∞)

Table 4.Attenuation Level

2 . Digital DBB(Dynamic Bass Boost) Mode

The Digital DBB in the AK4315 has four kind Digital DBB modes(off, min, mid, max).
(Table 5) When resetting, Digital DBB mode is set DBB0=DBB1=0(OFF).

mode	DBB1	DBB0
off	0	0
min	0	1
mid	1	0
max	1	1

Table 5. Digital DBB mode

3. De-emphasis control

DEM bit and DEM pin are ORed internally. The de-emphasis(tc=50/15us) corresponding to fs(sampling frequency) selected by FS0 and FS1 is enabled by setting DEM bit "1" or DEM pin "H". When DEM bit is "0" and DEM pin is "L", the de-emphasis is disabled and the setting of FS0 and FS1 is invalid. The de-emphasis is also disabled at FS0="1" and FS1="0". When resetting, DEM bit is set "0".
For example, when the de-emphasis is controlled by only DEM pin at fs=44.1kHz, DEM, FS0, FS1 bits should be "0". This condition is also set at resetting.

FS0	FS1	Mode
0	0	44.1kHz
1	0	OFF
0	1	48kHz
1	1	32kHz

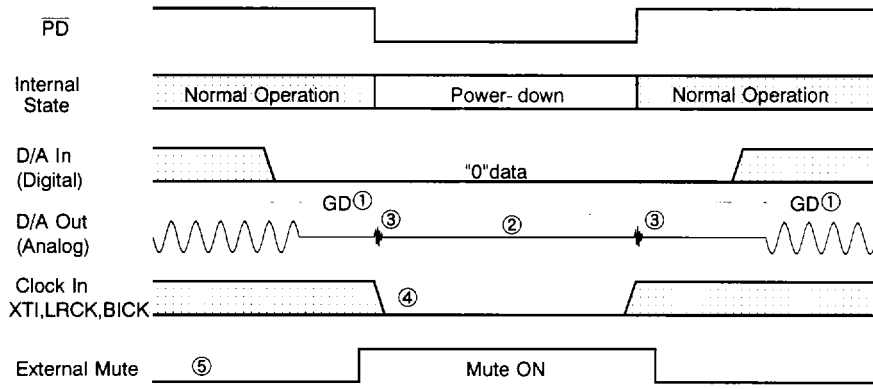
Table 6. De-emphasis filter setting
(Valid at DEM bit="1" or DEM pin="H")

4. Soft mute operation

When SMUTE bit goes "1", the output signal is attenuated by - ∞ ("0") during 1024LRCK cycles. This is same as SMUTE pin operation. SMUTE bit and SMUTE pin are ORed internally. When resetting, SMUTE bit is set "0"(OFF).

■ Power-Down

The AK4315 is placed in the power-down mode by bringing $\overline{PD}$ pin "L" and the analog outputs are floating(Hi-Z). When exiting the power-down mode, ATT value is set 7FH(0dB). Figure 7 shows an example of the system timing at the power-down and power-up.



Notes:

① Analog output corresponding to digital input have the group delay(GD).

② Analog outputs are floating(Hi-Z) at the power-down mode. The output noise level is about -110dB.

③ Click noise about -50dB occurs at the edges(" ↑ ↓ ") of $\overline{PD}$ signal.

④ When the external clocks(XTI,BICK,LRCK) are stopped, the AK4315 should be in the power-down mode.

⑤ Please mute the analog output externally if the click noise(③) influences system application. The timing example is shown in this figure.

Figure 7. Power-down/up sequence example

■ System Reset

The AK4315 should be reset once by bringing $\overline{PD}$ "L" upon power-up. The internal timing starts clocking by LRCK " ↑ " upon exiting reset.

SYSTEM DESIGN

Figure 8 shows the system connection diagram. An evaluation board[AKD4315] is available which demonstrates the optimum layout, power supply arrangements and measurement results.

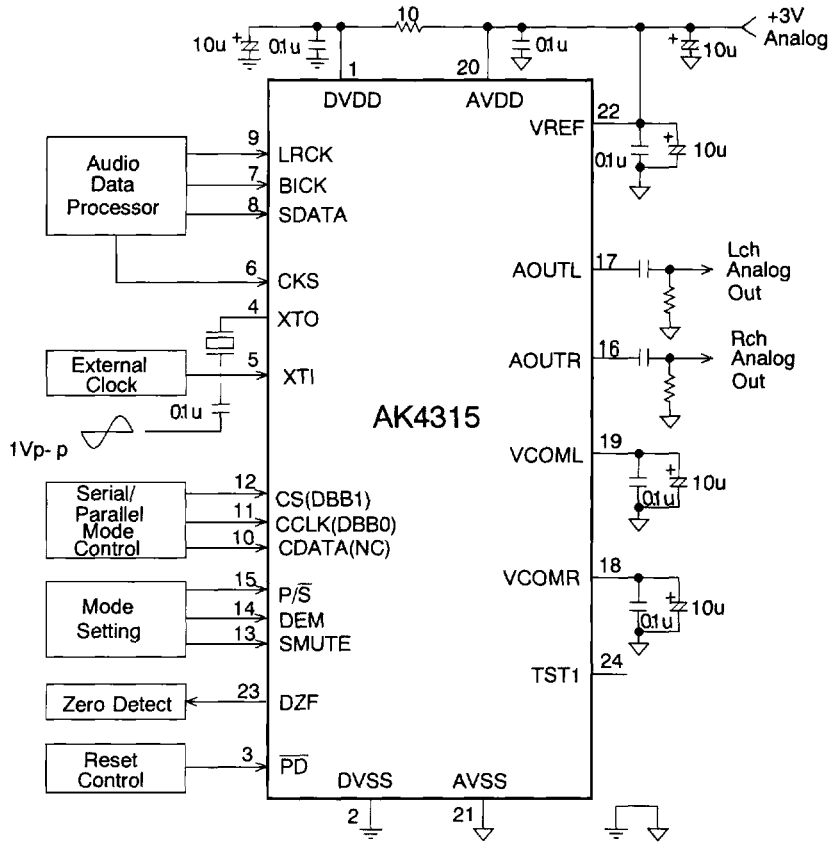


Figure 8. Typical Connection Diagram

Notes:

- LRCK=fs, BICK ≧ 32fs, XTI=256fs/384fs
- CCLK should be held "H" or "L" except writing to ATT & mode registers.
- When AOUT drives some capacitive load, some resistor should be added in series between AOUT and capacitive load.

■ System design consideration

1. Grounding and Power Supply Decoupling

To minimize coupling by digital noise, decoupling capacitors should be connected to AVDD and DVDD, respectively. AVDD is supplied from analog supply in system and DVDD is supplied from AVDD via 10 Ω resistor. Alternatively if AVDD and DVDD are supplied separately, AVDD and DVDD should be powered at the same time or AVDD should be powered earlier than DVDD.
Analog ground and digital ground should be connected together near to where the supplies are brought onto the printed circuit board. Decoupling capacitors for high frequency should be as near to the AK4315 device as possible, with the low value ceramic capacitor of VREF being the nearest.

2. Voltage reference

The differential Voltage between VREF and AVSS set the analog output range. VREF pin is normally connected to AVDD with a 0.1uF ceramic capacitor. VCOML and VCOMR are a signal ground of this chip. An electrolytic capacitor less than 10uF in parallel with a 0.1uF ceramic capacitor attached to these pins eliminates the effects of high frequency noise.
No load current may be drawn from VCOML and VCOMR pins. All signals, especially clocks, should be kept away from the VREF, VCOML and VCOMR pins in order to avoid unwanted coupling into the AK4315.

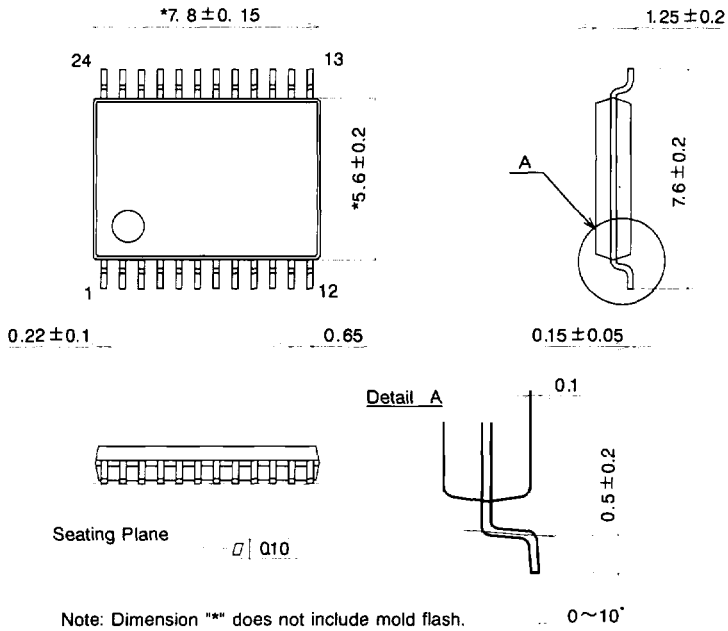
3. Analog Outputs

The analog outputs are also single-ended and centered around the VCOM voltage. The output signal range is typically 1.58Vpp. AC coupling capacitors of larger than 1uF are recommended. The internal switched-capacitor filter and continuous-time filter attenuate the noise generated by the delta-sigma modulator beyond the audio passband. Therefore, any external filters are not required for typical application. The output voltage is a positive full scale for 7FFFH and a negative full scale for 8000H. The ideal output is VCOM voltage for 0000H.

DC offsets on analog outputs are eliminated by AC coupling since analog outputs have DC offsets of a few mV + VCOM voltage.

PACKAGE

● 24pin VSOP (Unit: mm)

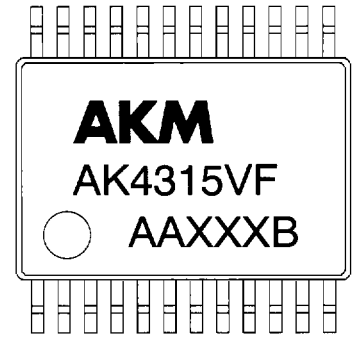


Note: Dimension "*" does not include mold flash.

■ Package & Lead frame material

Package molding compound :	Epoxy
Lead frame material :	Cu
Lead frame surface treatment:	Solder plate

MARKING



Contents of A A X X X B

A A : Lot# (alphabet)

X X X B : Date Code (X : numbers, B : alphabet)