Document Title

64Kx8 bit Low Power and Low Voltage CMOS Static RAM

Revision History

Revision No.	History	Draft Data	Remark
0	Design target	November 25, 1997	Advance
1.0	Finalize	August 27, 1998	Final

64Kx8 bit Low Power and Low Voltage CMOS Static RAM

FEATURES

- Process Technology: TFT
- Organization: 64Kx8
- Power Supply Voltage
  KM68V512A family: 3.0~3.6V
  KM68U512A family: 2.7~3.3V
- Low Data Retention Voltage: 2V(Min)
- Three state output and TTL Compatible
- Package Type: 32-TSOP1-0820F, 32-TSOP1-0813.4F

GENERAL DESCRIPTION

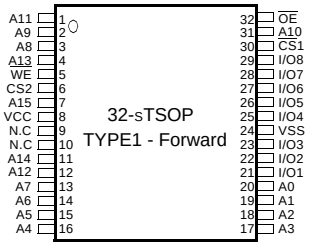
The K6T0908V2B and K6T0908U2B families are fabricated by SAMSUNG′s advanced CMOS process technology. The families support various operating temperature ranges and has various package types for user flexibility of system design. The family also support low data retention voltage for battery back-up operation with low data retention current.

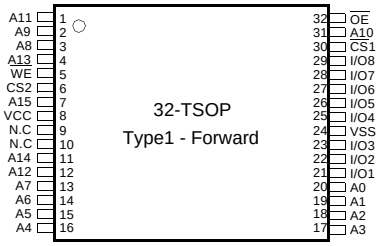
PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I_{SB1}, Max)	Operating (I_{CC2}, Max)	
K6T0908V2B-B	Commercial(0~70°C)	3.0 ~ 3.6V	85[1]/100ns	10μA	30mA	32-TSOP1-F 32-sTSOP1-F
K6T0908U2B-B		2.7 ~ 3.3V			25mA	
K6T0908V2B-F	Industrial(-40~85°C)	3.0 ~ 3.6V			30mA	
K6T0908U2B-F		2.7 ~ 3.3V			25mA	

1. The parameter is measured with 30pF test load.

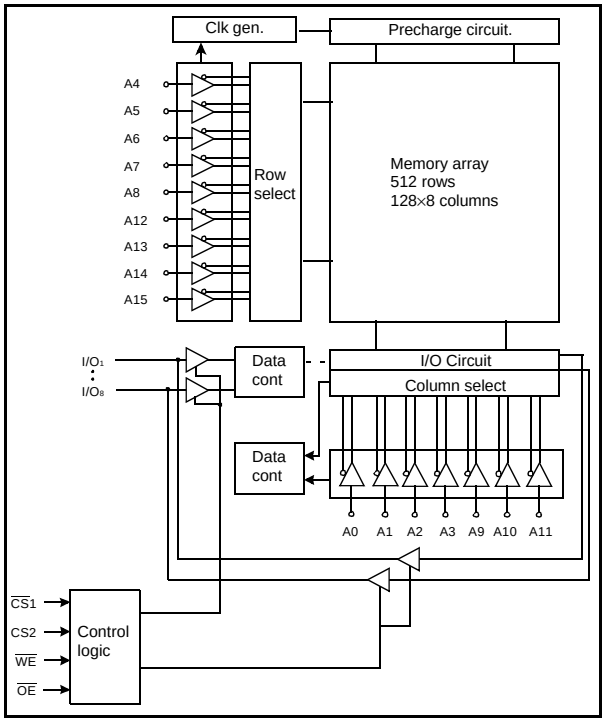
PIN DESCRIPTION





Name	Function	Name	Function
$\overline{CS_1}$,CS_2	Chip Select Inputs	I/O_1~I/O_8	Data Inputs/Outputs
$\overline{OE}$	Output Enable	Vcc	Power
$\overline{WE}$	Write Enable Input	Vss	Ground
A_0~A_{15}	Address Inputs	N.C	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Commercial Temperature Products(0~70°C)		Industrial Temperature Products(-40~85°C)	
Part Name	**Function**	**Part Name**	**Function**
K6T0908V2B-TB85	32-TSOP1 F, 85ns, 3.3V, LL	K6T0908V2B-TF85	32-TSOP1 F, 85ns, 3.3V, LL
K6T0908V2B-TB10	32-TSOP1 F, 100ns, 3.3V, LL	K6T0908V2B-TF10	32-TSOP1 F, 100ns, 3.3V, LL
		K6T0908V2B-YF85	32-sTSOP1 F, 85ns,3.3V,LL
K6T0908U2B-TB85	32-TSOP1 F, 85ns, 3.0V, LL	K6T0908V2B-YF10	32-sTSOP1 F, 100ns,3.3V,LL
K6T0908U2B-TB10	32-TSOP1 F, 100ns, 3.0V, LL		
		K6T0908U2B-TF85	32-TSOP1 F, 85ns, 3.0V, LL
		K6T0908U2B-TF10	32-TSOP1 F, 100ns, 3.0V, LL
		K6T0908U2B-YF85	32-sTSOP1 F, 85ns, 3.0V, LL
		K6T0908U2B-YF10	32-sTSOP1 F, 100ns,3.0V, LL

FUNCTIONAL DESCRIPTION

$\overline{CS_1}$	CS_2	$\overline{OE}$	$\overline{WE}$	I/O	Mode	Power
H	X[1)]	X[1)]	X[1)]	High-Z	Deselected	Standby
X[1)]	L	X[1)]	X[1)]	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X[1)]	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS[1)]

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V_{IN},V_{OUT}	-0.5 to V_{CC}+0.5	V	-
Voltage on Vcc supply relative to Vss	V_{CC}	-0.3 to 4.6	V	-
Power Dissipation	P_D	1	W	-
Storage temperature	T_{STG}	-65 to 150	°C	-
Operating Temperature	T_A	0 to 70	°C	K6T0908V2B-L, K6T0908U2B-L
		-40 to 85	°C	K6T0908V2B-P, K6T0908U2B-P
Soldering temperature and time	T_{SOLDER}	260°C, 10sec (Lead Only)	-	-

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS[1)]

Item	Symbol	Product	Min	Typ	Max	Unit
Supply voltage	Vcc	K6T0908V2B Family	3.0	3.3	3.6	V
		K6T0908U2B Family	2.7	3.0	3.3	V
Ground	Vss	All Family	0	0	0	V
Input high voltage	V_{IH}	K6T0908V2B, K6T0908U2B Family	2.2	-	Vcc+0.3V[2)]	V
Input low voltage	V_{IL}	K6T0908V2B, K6T0908U2B Family	-0.3[3)]	-	0.6	V

Note:
1. Commercial Product : T_A=0 to 70°C, otherwise specified
   Industrial Product : T_A=-40 to 85°C, otherwise specified
2. Overshoot : V_{CC}+3.0V in case of pulse width ≤ 30ns
3. Undershoot : -3.0V in case of pulse width ≤ 30ns
4. Overshoot and undershoot are sampled, not 100% tested

CAPACITANCE[1)] (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Input/Output capacitance	C_{IO}	V_{IO}=0V	-	8	pF

1. Capacitance is sampled, not 100% tested

DC AND OPERATING CHARACTERISTICS

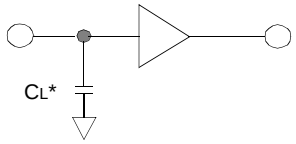
Item	Symbol	Test Conditions		Min	Typ	Max	Unit
Input leakage current	I_{LI}	V_{IN}=Vss to Vcc		-1	-	1	µA
Output leakage current	I_{LO}	$\overline{CS_1}$=V_{IH} or CS_2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}, V_{IO}=Vss to Vcc		-1	-	1	µA
Operating power supply	I_{CC}	I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IH} or V_{IL}, Read		-	-	5	mA
Average operating current	I_{CC1}	Cycle time=1µs, 100% duty, I_{IO}=0mA, $\overline{CS_1}$≤0.2V, CS_2≥Vcc-0.2V, V_{IN}≤0.2V or V_{IN}≥Vcc-0.2V		-	-	5	mA
	I_{CC2}	Cycle time=Min, 100% duty, I_{IO}=0mA, $\overline{CS_1}$=V_{IL}, CS_2=V_{IH}, V_{IN}=V_{IL} or V_{IH}	K6T0908V2B	-	-	30	mA
			K6T0908U2B	-	-	25	mA
Output low voltage	V_{OL}	I_{OL}=2.1mA		-	-	0.4	V
Output high voltage	V_{OH}	I_{OH}=-1.0mA		2.4	-	-	V
Standby Current(TTL)	I_{SB}	$\overline{CS_1}$=V_{IH}, CS_2=V_{IL}, Other inputs=V_{IL} or V_{IH}		-	-	0.3	mA
Standby Current (CMOS)	I_{SB1}	$\overline{CS_1}$≥Vcc-0.2V, CS_2≥Vcc-0.2V, or CS_2≤0.2V, Other inputs=0~Vcc		-	-	10	µA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Test Input/Output Reference)

Input pulse level : 0.4 to 2.2V
Input rising and falling time : 5ns
Input and output reference voltage : 1.5V
Output load (See right) : C_L[1)]=100pF+1TTL

1. 85ns part tested with 30pF test load.



* Including scope and jig capacitance

AC CHARACTERISTICS (K6T0908V2B Family:Vcc=3.0~3.6V, K6T0908U2B Family:Vcc=2.7~3.3V, Commercial products:T_A=0 to 70°C, Industrial products:T_A=-40 to 85°C)

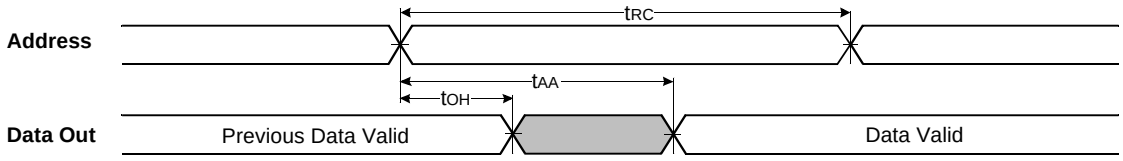
Parameter List		Symbol	Speed Bins				Units
			85ns		100ns		
			Min	Max	Min	Max	
Read	Read cycle time	t_{RC}	85	-	100	-	ns
	Address access time	t_{AA}	-	85	-	100	ns
	Chip select to output	t_{CO}	-	85	-	100	ns
	Output enable to valid output	t_{OE}	-	45	-	50	ns
	Chip select to low-Z output	t_{LZ}	10	-	10	-	ns
	Output enable to low-Z output	t_{OLZ}	5	-	5	-	ns
	Chip disable to high-Z output	t_{HZ}	0	30	0	30	ns
	Output disable to high-Z output	t_{OHZ}	0	20	0	20	ns
	Output hold from address change	t_{OH}	10	-	15	-	ns
Write	Write cycle time	t_{WC}	85	-	100	-	ns
	Chip select to end of write	t_{CW}	70	-	80	-	ns
	Address set-up time	t_{AS}	0	-	0	-	ns
	Address valid to end of write	t_{AW}	70	-	80	-	ns
	Write pulse width	t_{WP}	60	-	70	-	ns
	Write recovery time	t_{WR}	0	-	0	-	ns
	Write recovery time	t_{WR1}	0	-	0	-	ns
	Write to output high-Z	t_{WHZ}	0	25	0	30	ns
	Data to write time overlap	t_{DW}	35	-	40	-	ns
	Data hold from write time	t_{DH}	0	-	0	-	ns
	End write to output low-Z	t_{OW}	5	-	5	-	ns

DATA RETENTION CHARACTERISTICS

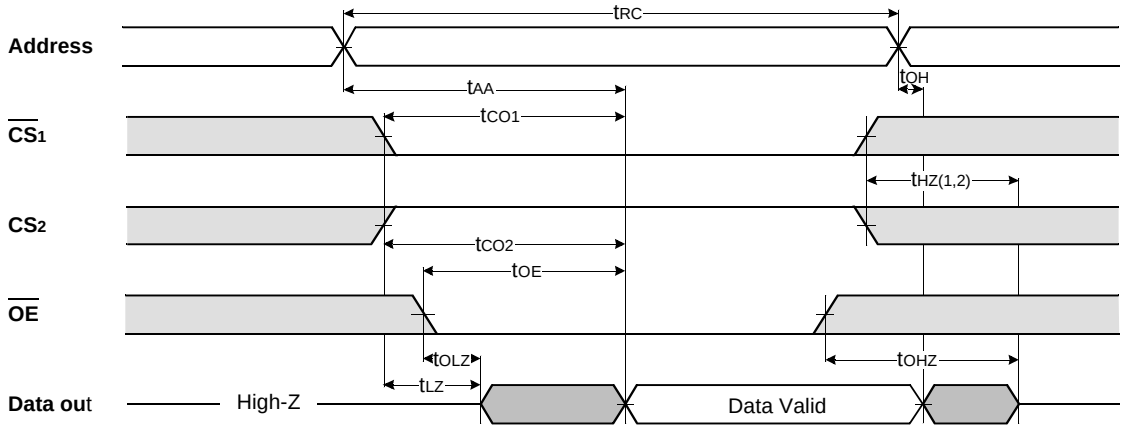
Item	Sym	Test Condition	Min	Typ	Max	Unit
Vcc for data retention	V_{DR}	$\overline{CS_1} \geq$ Vcc-2.0V, $CS_2 \geq$ Vcc-2.0V or $CS_2 \leq$ 0.2V	2.0	-	3.6	V
Data retention current	I_{DR}	Vcc=3.0V, $\overline{CS_1} \leq$ Vcc-0.2V, $CS_2 \geq$ Vcc-0.2V or $CS_2 \leq$ 0.2V	-	-	10	µA
Data retention set-up time	t_{SDR}	See data retention waveform	0	-	-	ms
Recovery time	t_{RDR}		5	-	-	

TIMMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS_1}$=$\overline{OE}$=V_{IL}, $\overline{WE}$=V_{IH})



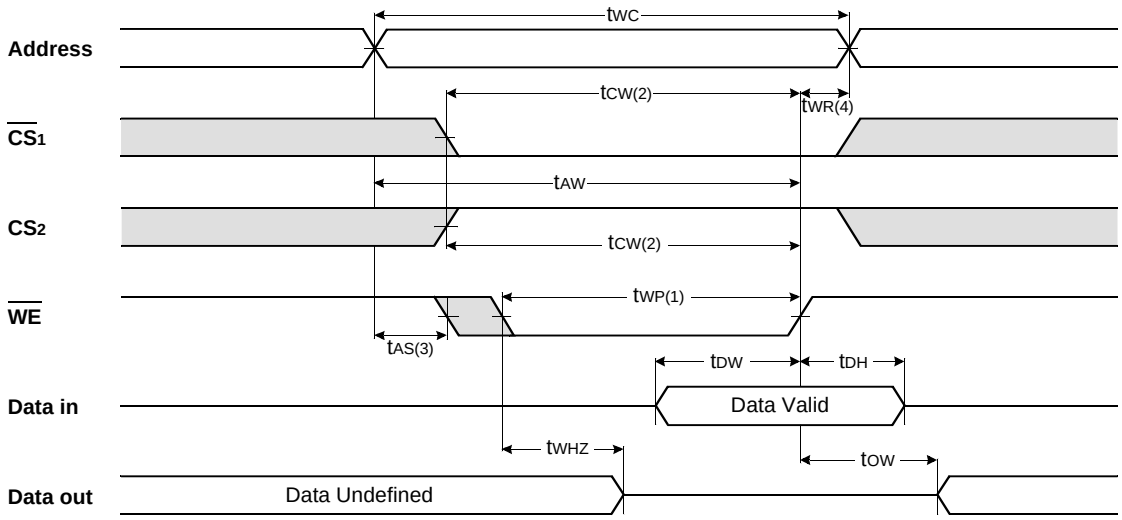
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}$=V_{IH})



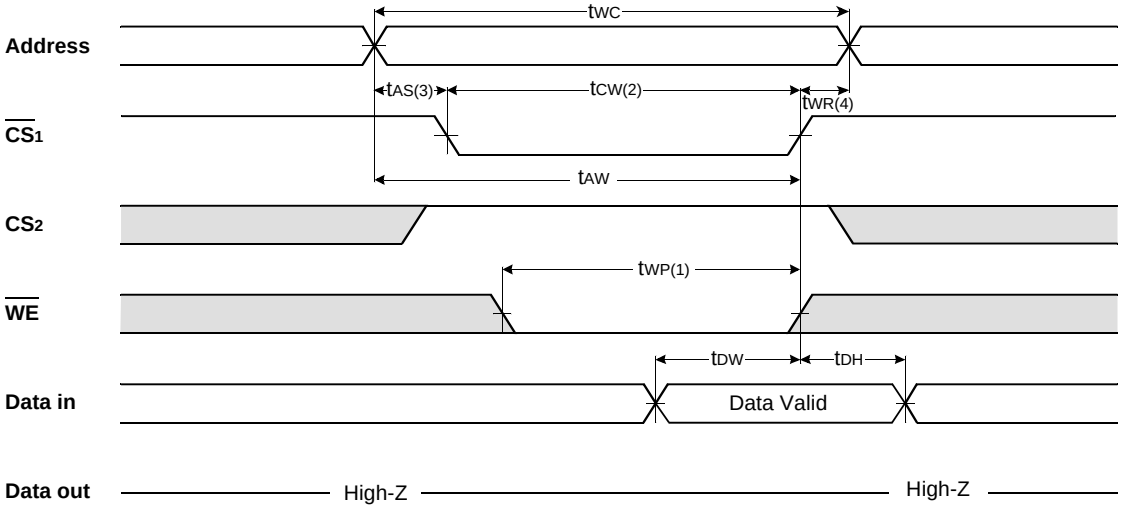
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.

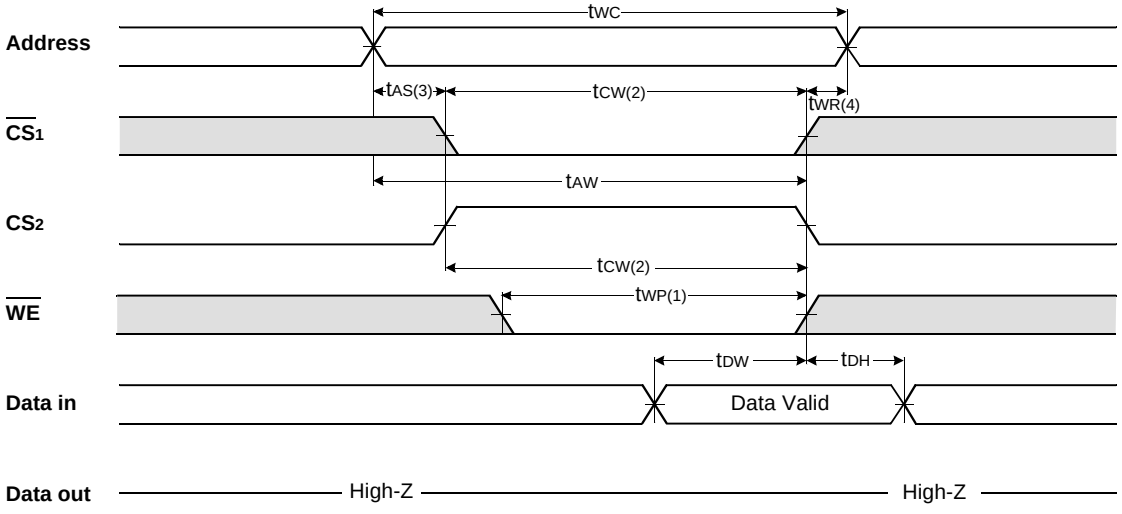
TIMING WAVEFORM OF WRITE CYCLE(1) ($\overline{WE}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS_1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS_2 Controlled)

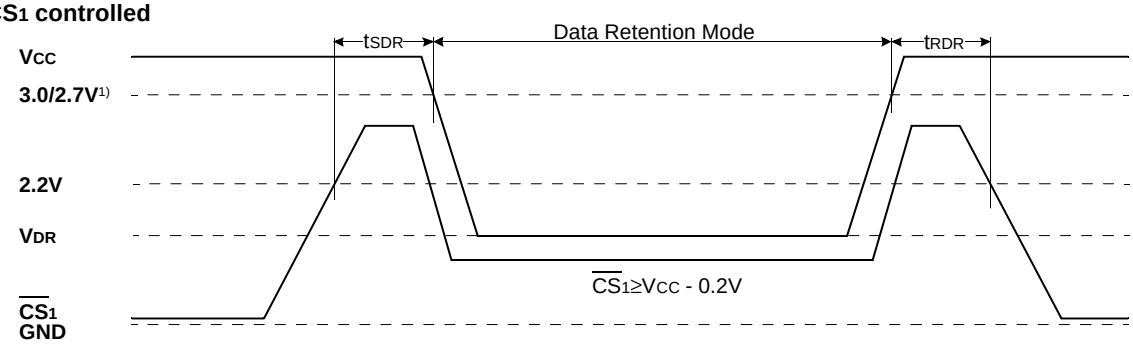


NOTES (WRITE CYCLE)

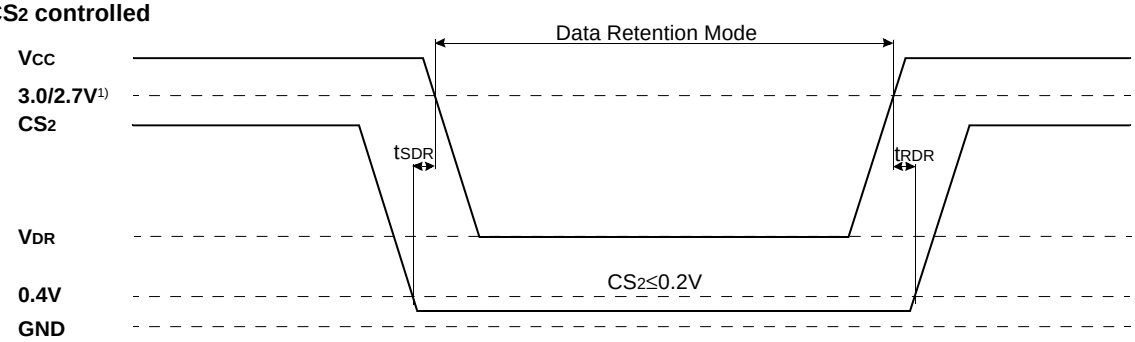
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS_2 and a low $\overline{WE}$. A write begins at the latest transition among $\overline{CS_1}$ goes low, CS_2 going high and $\overline{WE}$ going low : A write end at the earliest transition among $\overline{CS_1}$ going high, CS_2 going low and $\overline{WE}$ going high, t_{WP} is measured from the begining of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. $t_{WR(1)}$ applied in case a write ends as $\overline{CS_1}$ or $\overline{WE}$ going high $t_{WR(2)}$ applied in case a write ends as CS_2 going to low.

DATA RETENTION WAVE FORM

$\overline{CS_1}$ controlled



CS_2 controlled

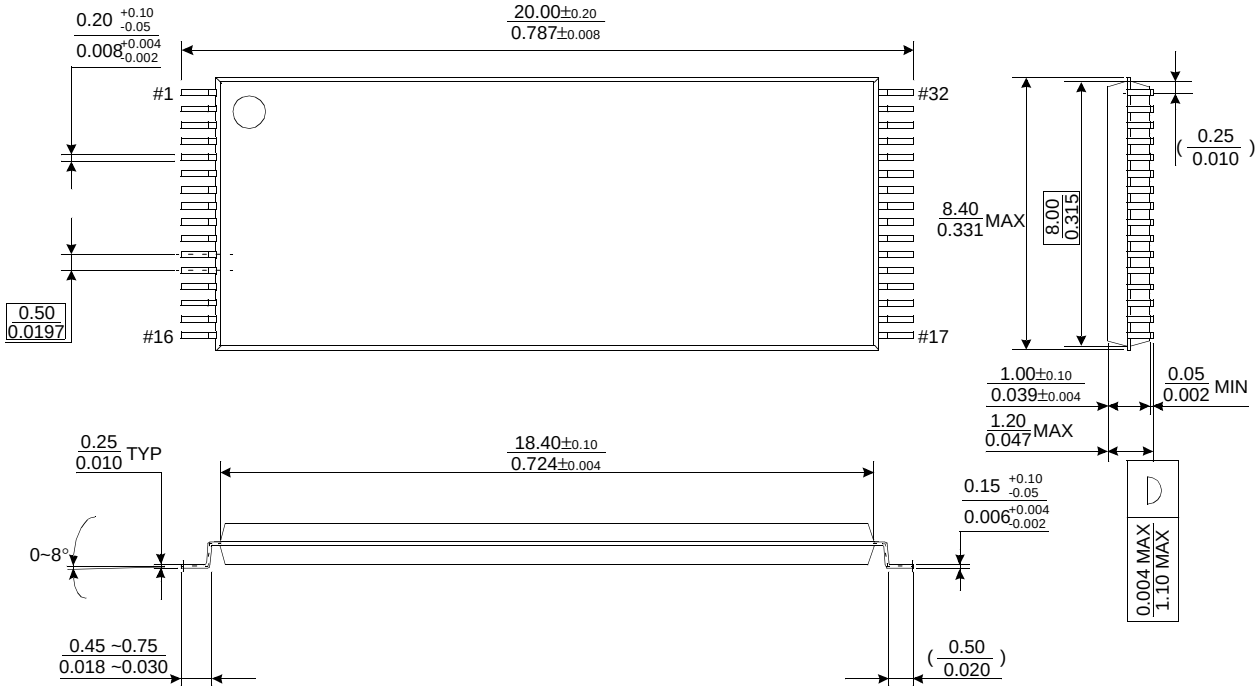


1. 3.0V for K6T0908V2B Family, 2.7V for K6T0908U2B Family

PACKAGE DIMENSIONS

Units: millimeter(Inch)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)



32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0813.4F)