2GB – 2x128Mx72 DDR2 SDRAM REGISTERED, ECC, w/PLL

FEATURES

- 200-pin, small-outline dual in-line memory module (SO-DIMM)
- Fast data transfer rates: PC2-6400*, PC2-5300*, PC2-4200 and PC2-3200
- Utilizes 800*, 667*, 533 and 400 MT/s DDR2 SDRAM components
- V_{CC} = V_{CC} = 1.8V (± 0.1V)
- V_{CCSPD} = 1.7V to 3.6V
- JEDEC standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL): 3, 4, 5 and 6
- Adjustable data-output drive strength
- On-die termination (ODT)
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- 64ms: 8,192 cycle refresh
- Gold edge contacts
- Dual Rank
- RoHS compliant
- JEDEC Package
  - 200 Pin (SO-DIMM): 30.00mm (1.181") TYP.

DESCRIPTION

The W3HG2128M72EER is a 2x128Mx72 Double Data Rate DDR2 SDRAM high density SODIMM. This memory module consists of eighteen 128Mx8 (1Gb) bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 200-pin SO-DIMM FR4 substrate.

* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

NOTE: Consult factory for availability of:
- Vendor source control options
- Industrial temperature option

OPERATING FREQUENCIES

	PC2-3200	PC2-4300	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t_{RCD}-t_{RP}	3-3-3	4-4-4	5-5-5	6-6-6

* Consult factory for availability

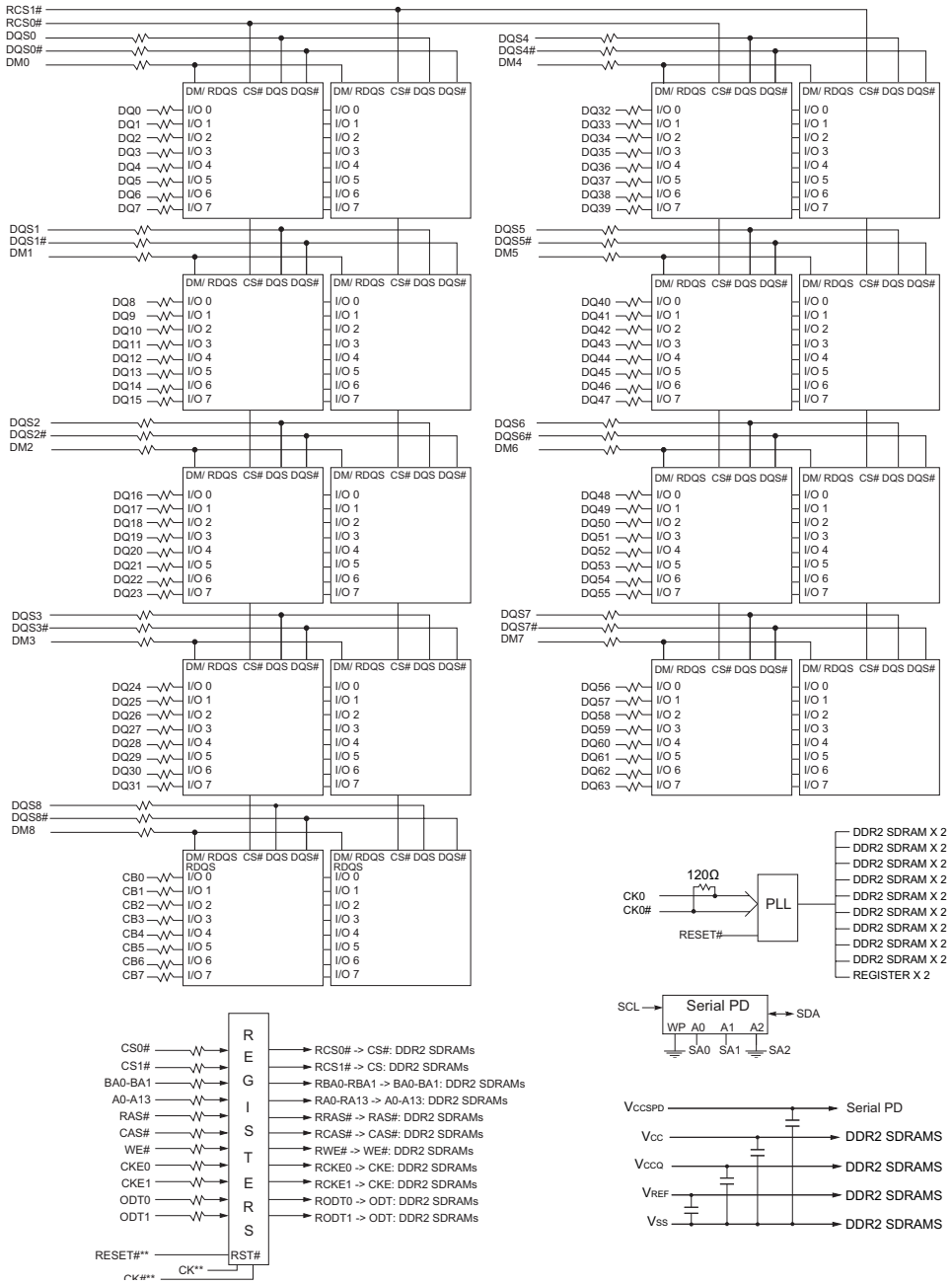
PIN CONFIGURATION

PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL	PIN#	SYMBOL
1	V_{REF}	51	DQ18	101	V_{CC}	151	V_{SS}
2	V_{SS}	52	V_{SS}	102	A6	152	V_{SS}
3	DQ0	53	DQ19	103	A5	153	DQS5#
4	DQ4	54	DQ28	104	A4	154	DM5
5	V_{SS}	55	V_{SS}	105	A3	155	DQS5
6	DQ5	56	DQ29	106	V_{CC}	156	V_{SS}
7	DQ1	57	DQ24	107	A2	157	V_{SS}
8	V_{SS}	58	V_{SS}	108	A1	158	DQ46
9	DQS0#	59	DQ25	109	V_{CC}	159	DQ42
10	DM0	60	DM3	110	A0	160	DQ47
11	DQS0	61	V_{SS}	111	A10/AP	161	DQ43
12	V_{SS}	62	V_{SS}	112	BA1	162	V_{SS}
13	V_{SS}	63	DQS3#	113	BA0	163	V_{SS}
14	DQ6	64	DQ30	114	V_{CC}	164	DQ52
15	DQ2	65	DQS3	115	RAS#	165	DQ48
16	DQ7	66	DQ31	116	WE#	166	DQ53
17	DQ3	67	V_{SS}	117	V_{CC}	167	DQ49
18	V_{SS}	68	V_{SS}	118	S0#	168	V_{SS}
19	V_{SS}	69	DQ26	119	CAS#	169	V_{SS}
20	DQ12	70	CB4	120	ODT0	170	DM6
21	DQ8	71	DQ27	121	NC/S1#	171	DQS6#
22	DQ13	72	CB5	122	A13	172	V_{SS}
23	DQ9	73	V_{SS}	123	V_{CC}	173	DQS6
24	V_{SS}	74	V_{SS}	124	V_{CC}	174	DQ54
25	V_{SS}	75	CB0	125	ODT1	175	V_{SS}
26	DM1	76	DM8	126	CK	176	DQ55
27	DQS1#	77	CB1	127	NC/S3#	177	DQ50
28	V_{SS}	78	V_{SS}	128	CK#	178	V_{SS}
29	DQS1	79	V_{SS}	129	DQ32	179	DQ51
30	DQ14	80	CB6	130	V_{SS}	180	DQ60
31	V_{SS}	81	DQS8#	131	V_{SS}	181	V_{SS}
32	DQ15	82	CB7	132	DQ36	182	DQ61
33	DQ10	83	DQS8	133	DQ33	183	DQ56
34	V_{SS}	84	V_{SS}	134	DQ37	184	V_{SS}
35	DQ11	85	V_{SS}	135	DQS4#	185	DQ57
36	DQ20	86	CB2	136	V_{SS}	186	DM7
37	V_{SS}	87	CKE0	137	DQS4	187	V_{SS}
38	DQ21	88	CB3	138	DM4	188	DQ62
39	DQ16	89	NC/CKE1	139	V_{SS}	189	DQS7#
40	V_{SS}	90	V_{SS}	140	V_{SS}	190	V_{SS}
41	DQ17	91	NC/S2#	141	DQ34	191	DQS7
42	RESET#	92	NC/BA2	142	DQ38	192	DQ63
43	V_{SS}	93	V_{CC}	143	DQ35	193	DQ58
44	DM2	94	NC	144	DQ39	194	SDA
45	DQS2#	95	A12	145	V_{SS}	195	V_{SS}
46	V_{SS}	96	A11	146	V_{SS}	196	SCL
47	DQS2	97	A9	147	DQ40	197	DQ59
48	DQ22	98	V_{CC}	148	DQ44	198	SA1
49	V_{SS}	99	A7	149	DQ41	199	V_{CCSPD}
50	DQ23	100	A8	150	DQ45	200	SA0

PIN NAMES

Pin Name	Function
A0 ~ A13	Address Inputs
BA0 ~ BA1	Bank Address Inputs
DQ0 ~ DQ63	Data Input/Output
CB0 ~ CB7	Check Bits
DQS0 ~ DQS8	Data Strobes
DQS0# ~ DQS8#	Data Strobes Complement
ODT0, ODT1	On-die Termination Control
CK,CK#	Clock Imput
CKE0, CKE1	Clock Enables
CS0# ~ CS3#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
DM0 ~ DM8	Data Masks
V_{CC}	Voltage Supply 1.8V +/- 0.1V
A10/AP	Address input/Autoprecharge
V_{CC}SPD	SPD Voltage supply 1.7V to 3.6V
V_{CCQ}	I/O Power (1.8v)
V_{SS}	Ground
SA0 ~ SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
V_{REF}	SSTL_18 Refrence Voltage
NC	No Connect

FUNCTIONAL BLOCK DIAGRAM



**RESET#. CK and CK# connects to both Registers. Other signals connect to one of two Registers.

Note:

- Unless otherwise noted, resister values are 22 Ohms.

DC OPERATING CONDITIONS

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V_{CC}	1.7	1.8	1.9	V	1
I/O Supply Voltage	V_{CCQ}	1.7	1.8	1.9	V	4
V_{CCL} Supply Voltage	V_{CCL}	1.7	1.8	1.9	V	4
I/O Reference Voltage	V_{REF}	0.49 x V_{CCQ}	0.50 x V_{CCQ}	0.51 x V_{CCQ}	V	2
I/O Termination Voltage	V_{TT}	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3

Notes:

1. V_{CC} & V_{CCQ} must track each other. V_{CCQ} must be less than or equal to V_{CC}.
2. V_{REF} is expected to equal $V_{CCQ/2}$ of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not excedd +/-1percent of the DC value. Peak-to-peak AC noise on V_{REF} may not exceed +/-2 percent of V_{REF}. This measurement is to be taken at the nearest V_{REF} bypass capacitor.
3. V_{TT} is not applied directly to the device. V_{TT} is a system supply for signal termination resistors, is expected to be set equal.
4. V_{CCQ} tracks with V_{CC};V_{CCL} tracke with V_{CC}

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Min	Max	Units
V_{CC}	Voltage on V_{CC} pin relative to V_{SS}		-1.0	2.3	V
V_{CCQ}	Voltage on V_{CCQ} pin relative to V_{SS}		-0.5	2.3	V
V_{CCL}	Voltage on V_{CCL} pin relative to V_{SS}		-0.5	2.3	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.5	2.3	V
T_{STG}	Storage Temperature		-55	100	°C
T_{CAS}	Device operating temperature		0	85	°C
I_L	Input leakage current; Any input 0V<V_{IN}<V_{CC}; V_{REF} input 0V,V_{IN},0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE, ODT	-5	5	µA
		CK, CK#	-10	10	µA
		DM	-10	10	µA
I_{OZ}	Output leakage current; 0V<V_{IN}<V_{CC}; DQs and ODT are disable	DQ, DQS, DQS#	-10	10	µA
I_{VREF}	V_{REF} leakage current; V_{REF} = Valid V_{REF} level		-36	36	µA

INPUT/OUTPUT CAPACITANCE

T_A = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance (A0~A13, BA0~BA1, RAS#, CAS#, WE#)	C_{IN1}			pF
Input Capacitance (CKE0, CKE1), (ODT, ODT1)	C_{IN2}			pF
Input Capacitance (CS0#, CS1#)	C_{IN3}			pF
Input Capacitance (CK0, CK0#, CK1, CK1#)	C_{IN4}			pF
Input Capacitance (DM0 ~ DM7), (DQS0 ~ DQS7)	C_{IN5} (E6)			pF
	C_{IN5} (D5)			pF
Input Capacitance (DQ0 ~ DQ63)	C_{OUT1} (E6)			pF
	C_{OUT1} (D5)			pF

OPERATING TEMPERATURE CONDITION

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0°C to 85°C	°C	1, 2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDED JESD51.2
2. At 0°C - 85°C, operation temperature range, all DRAM specification will be supported.

INPUT DC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage	V_{IH}(DC)	V_{REF} + 0.125	V_{CC} + 0.300	V
Input Low (Logic 0) Voltage	V_{IL}(DC)	-0.300	V_{REF} - 0.125	V

INPUT AC LOGIC LEVEL

All voltages referenced to V_{SS}

Parameter	Symbol	Min	Max	Units
Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V_{IH}(DC)	V_{REF} + 0.250	-	V
Input Low (Logic 1) Voltage DDR2-667	V_{IH}(DC)	V_{REF} + 0.200	-	V
Input Low (Logic 0) Voltage DDR2-400 & DDR2-533	V_{IL}(DC)	-	V_{REF} - 0.250	V
Input Low (Logic 0) Voltage DDR2-667, DDR2-800(TBD)	V_{IL}(DC)	-	V_{REF} - 0.200	V

I_{CC} SPECIFICATION

Symbol	Proposed Conditions		806	665	534	403	Units
I_{CC0}*	Operating one bank active-precharge; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING						mA
I_{CC1}*	Operating one bank active-read-precharge; I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Address businputs are SWITCHING; Data pattern is same as I_{CC}4W						mA
I_{CC2P}**	Precharge power-down current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING						mA
I_{CC2Q}**	Precharge quiet standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputsare STABLE; Data bus inputs are FLOATING						mA
I_{CC2N}**	Precharge standby current; All banks idle; $t_{CK} = t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING						mA
I_{CC3P}**	Active power-down current; All banks open; $t_{CK} = t_{CK}(I_{CC})$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0					mA
		Slow PDN Exit MRS(12) = 1					mA
I_{CC3N}**	Active standby current; All banks open; $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC}$, $t_{RAS} = t_{RAS}$ min(I_{CC}); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING						mA
I_{CC4W}*	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$max(I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING						mA
I_{CC4R}*	Operating burst read current; All banks open, Continuous burst reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = 0; $t_{CK} = t_{CK}(I_{CC})$, $t_{RAS} = t_{RAS}$max(I_{CC}), $t_{RP} = t_{RP}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I_{CC}4W						mA
I_{CC5}**	Burst auto refresh current; $t_{CK} = t_{CK}(I_{CC})$; Refresh command at every $t_{RFC}(I_{CC})$ interval; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING						mA
I_{CC6}**	Self refresh current; CK and CK# at 0V; CKE 0.2V; Other control and address bus inputs vre FLOATING; Data bus inputs are FLOATING	Normal					mA
I_{CC7}*	Operating bank interleave read current; All bank interleaving reads, I_{OUT} = 0mA; BL = 4, CL = CL(I_{CC}), AL = t_{RC}D(I_{CC})-1*t_{CK}(I_{CC}); $t_{CK} = t_{CK}(I_{CC})$, $t_{RC} = t_{RC}(I_{CC})$, $t_{RRD} = t_{RRD}(I_{CC})$, $t_{RCD} = 1*t_{CK}(I_{CC})$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.						mA

I_{CC} specification is based on xxxx components. Other DRAM manufactures specification may be different.

Note:

* Value calculated as one module rank in this operating condition, and all other module ranks in I_{CC}2P (CKE LOW) mode.

** Value calculated reflects all module ranks in this operating condition.

DDR2 SDRAM COMPONENTAC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS				806		665		534		403		
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	$t_{CK\ (6)}$									ps
		CL = 5	$t_{CK\ (5)}$									ps
		CL = 4	$t_{CK\ (4)}$									ps
		CL = 3	$t_{CK\ (3)}$									ps
	CK high-level width		t_{CH}									t_{CK}
	CK low-level width		t_{CL}									t_{CK}
	Half clock period		t_{HP}									ps
	Clock jitter		t_{JIT}									ps
Data	DQ output access time from CK/CK#		t_{AC}									ps
	Data-out high-impedance window from CK/CK#		t_{HZ}									ps
	Data-out low-impedance window from CK/CK#		t_{LZ}									ps
	DQ and DM input setup time relative to DQS		t_{DS}									ps
	DQ and DM input hold time relative to DQS		t_{DH}									ps
	DQ and DM input pulse width (for each input)		t_{DIPW}									t_{CK}
	Data hold skew factor		t_{QHS}									ps
	DQ…DQS hold, DQS to first DQ to go nonvalid, per access		t_{QH}									ps
	Data valid output window (DVW)		t_{DVW}									ns
Data Strobe	DQS input high pulse width		t_{DQSH}									t_{CK}
	DQS input low pulse width		t_{DQSL}									t_{CK}
	DQS output access time from CK/CK#		t_{DQSCK}									ps
	DQS falling edge to CK rising … setup time		t_{DSS}									t_{CK}
	DQS falling edge from CK rising … hold time		t_{DSH}									t_{CK}
	DQS…DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}									ps
	DQS read preamble		t_{RPRE}									t_{CK}
	DQS read postamble		t_{RPST}									t_{CK}
	DQS write preamble setup time		t_{WPRES}									p s
	DQS write preamble		t_{WPRE}									t_{CK}
	DQS write postamble		t_{WPST}									t_{CK}
	Write command to first DQS latching transition		t_{DQSS}									t_{CK}
	Address and control input pulse width for each input		t_{IPW}									t_{CK}
	Address and control input setup time		t_{IS}									ps
	Address and control input hold time		t_{IH}									ps
	Address and control input hold time		t_{CCD}									t_{CK}

AC specification is based on xxxx components. Other DRAM manufactures specification may be different.

Continued on next page

DDR2 SDRAM COMPONENTAC TIMING PARAMETERS & SPECIFICATIONS (cont'd)

AC CHARACTERISTICS			806		665		534		403		
	PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t_{RC}									ns
	ACTIVE bank a to ACTIVE bank b command	t_{RRD}									ns
	ACTIVE to READ or WRITE delay	t_{RCD}									ns
	Four Bank Activate period	t_{FAW}									ns
	ACTIVE to PRECHARGE command	t_{RAS}									ns
	Internal READ to precharge command delay	t_{RTP}									ns
	Write recovery time	t_{WR}									ns
	Auto precharge write recovery + precharge time	t_{DAL}									ns
	Internal WRITE to READ command delay	t_{WTR}									ns
	PRECHARGE command period	t_{RP}									ns
	PRECHARGE ALL command period	t_{RPA}									ns
	LOAD MODE command cycle time	t_{MRD}									t_{CK}
	CKE low to CK,CK# uncertainty	t_{DELAY}									ns
Self Refresh	REFRESH to Active of Refresh to Refresh command interval	t_{RFC}									ns
	Average periodic refresh interval	t_{REFI}									µs
	Exit self refresh to non-READ command	t_{XSNR}									ns
	Exit self refresh to READ command	t_{XSRD}									t_{CK}
	Exit self refresh timing reference	t_{ISXR}									ps
ODT	ODT turn-on delay	t_{AOND}									t_{CK}
	ODT turn-on	t_{AON}									ps
	ODT turn-off delay	t_{AOFD}									t_{CK}
	ODT turn-off	t_{AOF}									ps
	ODT turn-on (power-down mode)	t_{AONPD}									ps
	ODT turn-off (power-down mode)	t_{AOFPD}									ps
	ODT to power-down entry latency	t_{ANPD}									t_{CK}
	ODT power-down exit latency	t_{AXPD}									t_{CK}
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t_{XARD}									t_{CK}
	Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}									t_{CK}
	A Exit precharge power-down to any non-READ command.	t_{XP}									t_{CK}
	CKE minimum high/low time	t_{CKE}									t_{CK}

AC specification is based on xxxx components. Other DRAM manufactures specification may be different.

ORDERING INFORMATION FOR D4

Part Number	Speed/Data Rate Frequency	CAS Latency	t_{RCD}	t_{RP}	Height**
W3HG2128M72EER806D4xG*	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
W3HG2128M72EER665D4xG*	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
W3HG2128M72EER534D4xG	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
W3HG2128M72EER403D4xG	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

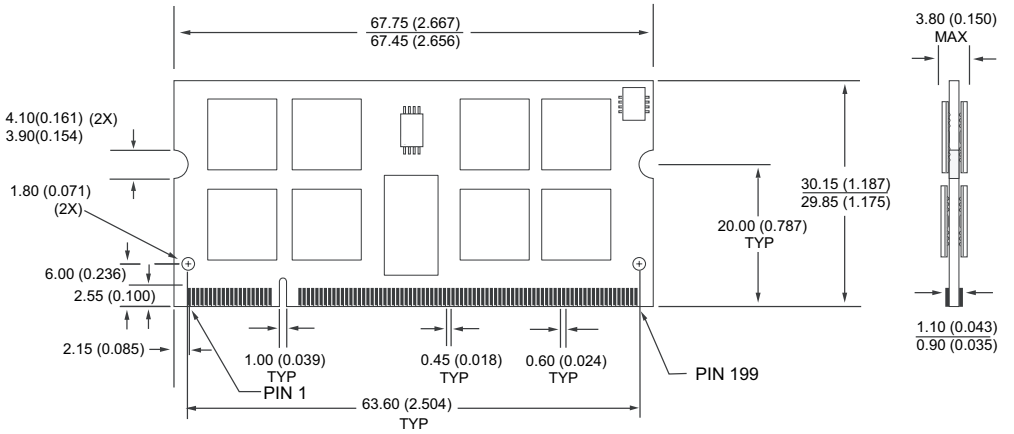
* Consult factory for availability

Notes:

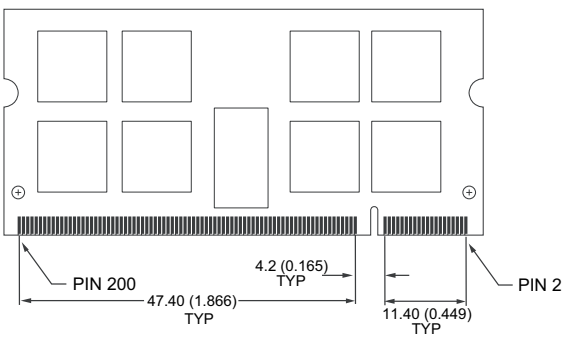
- RoHS product. ("G" = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)

PACKAGE DIMENSIONS FOR D4

FRONT VIEW

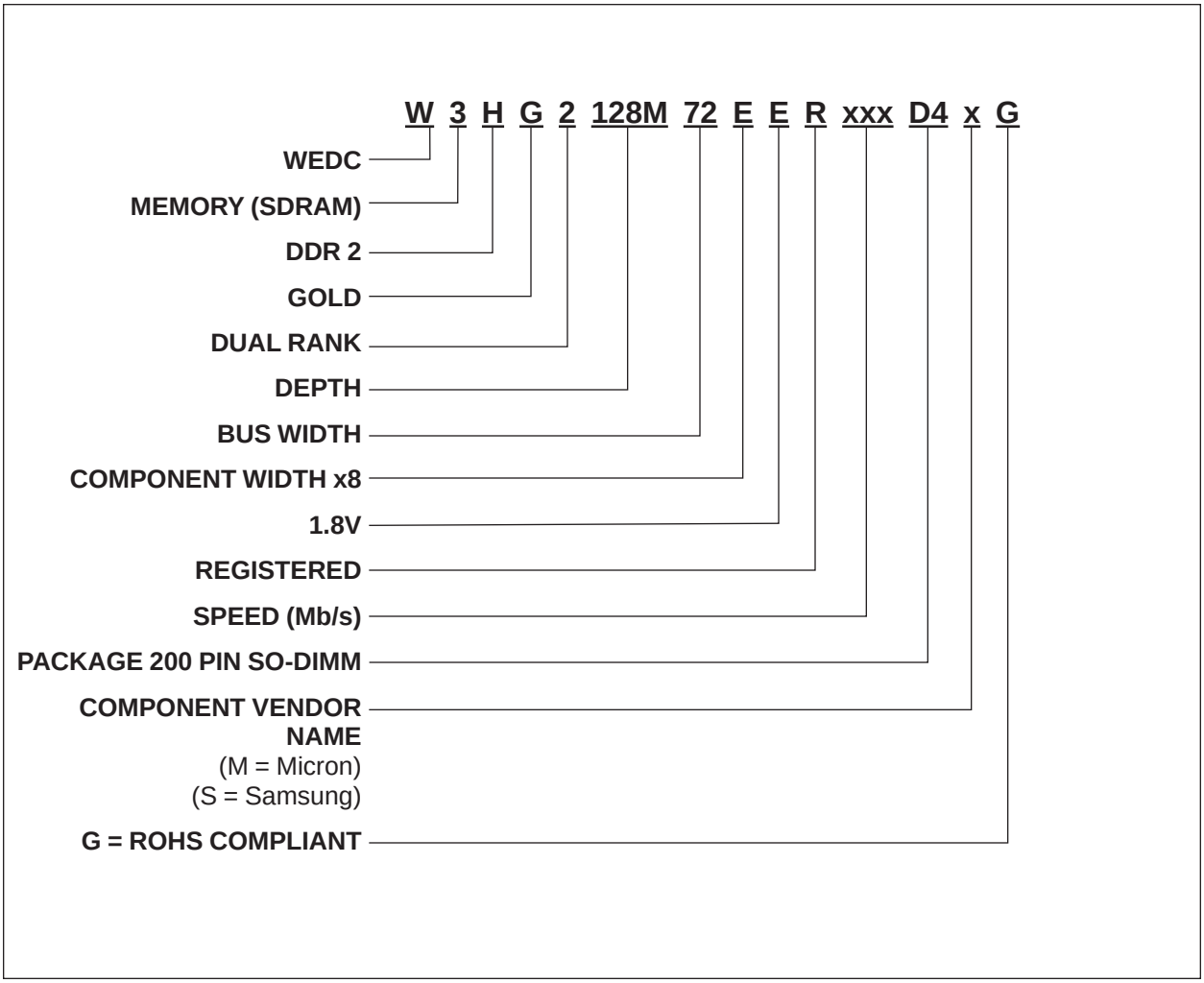


BACK VIEW



** ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)

PART NUMBERING GUIDE



Document Title

2GB – 2x128Mx72 DDR2 SDRAM REGISTERED,PLL, SO-DIMM

Revision History

Rev #	History	Release Date	Status
Rev 0	Created	January 2006	Concept
Rev 1	1.0 Updated AC title to indicate component AC spec only	October 2006	Advanced