Integrated Device Technology, Inc.

256K (16K x 16) CMOS STATIC RAM DUAL SIP MODULE

IDT 7MC4005

FEATURES:

- High-density 16-bit word 256K (16K x 16) static RAM module
- Low profile 36-pin sidebraze ceramic DSIP (dual single-in-line package)
- Fast access time: 20ns (max.)
- Surface mounted LCC components mounted on a co-fired ceramic substrate
- CEMOS™ process virtually eliminates alpha particle soft error rates (with no organic die coating)
- Single 5V (±10%)
- Inputs/outputs directly TTL-compatible
- Multiple GND pins for maximum noise immunity

DESCRIPTION:

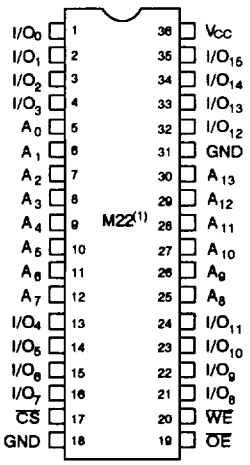
The IDT7MC4005 is a 16-bit wide 256K (16K x 16) static RAM module constructed on a co-fired ceramic substrate using four IDT7198 16K x 4 static RAMs in leadless chip carriers. Extremely fast speeds can be achieved due to the use of 64K static RAMs fabricated in IDT's high-performance, high-reliability CEMOS technology. The IDT7MC4005 is available with access times as fast as 20ns, with minimal power consumption.

The IDT7MC family of ceramic DSIPs offers the optimum in packing density and profile height. The IDT7MC4005 is packaged in a 36-pin ceramic DSIP (dual single-in-line package). The dual row configuration allows 36 pins to be placed on a package 1.8 inches long and .27 inches wide. At only .500 inches high, this low profile package is ideal for systems with minimum board spacing. Extremely high packing density can also be achieved, allowing four IDT7MC4005 modules to be stacked per 1.2 inches of board space.

All inputs and outputs of the IDT7MC4005 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry is used, requiring no clocks or refreshing for operation, and providing equal access and cycle times for ease of use.

All IDT military module semiconductor components are manufactured in compliance to the latest revision of MIL-STD-883, Class B, making them ideally suited to applications demanding the highest level of performance and reliability.

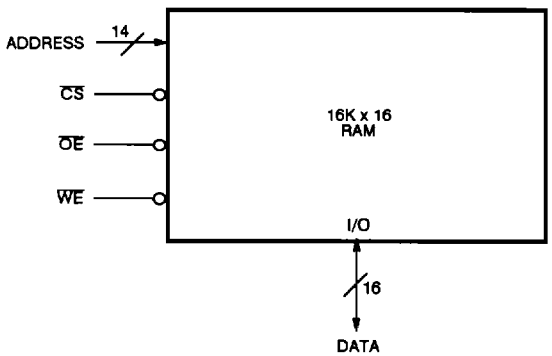
PIN CONFIGURATION



NOTE:

1. For module dimensions, please refer to module drawing M22 in the packaging section.

FUNCTIONAL BLOCK DIAGRAM



PIN NAMES

I/O_{0-15}	Data Inputs/Outputs
A_{0-13}	Addresses
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
V_{CC}	Power
GND	Ground

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ABSOLUTE MAXIMUM RATINGS [1]

SYMBOL	RATING	COMMERCIAL	MILITARY	UNIT
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-10 to +85	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
I_{OUT}	DC Output Current	50	50	mA

NOTE:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	–	6.0	V
V_{IL}	Input Low Voltage	0.5[1]	–	0.8	V

NOTE:

1. V_{IL} = -3.0V for pulse width less than 20ns.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

GRADE	AMBIENT TEMPERATURE	GND	V_{CC}
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	MILITARY MIN.	MILITARY MAX.	COMMERCIAL MIN.	COMMERCIAL MAX.	UNIT
$\|I_{LI}\|$	Input Leakage Current (Address & Control)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	40	–	20	µA
$\|I_{LI}\|$	Input Leakage (Data)	V_{CC} = Max. V_{IN} = GND to V_{CC}	–	10	–	5	µA
$\|I_{LO}\|$	Output Leakage	V_{CC} = Max. $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	–	10	–	5	µA
V_{OL}	Output Low Voltage	V_{CC} = Min., I_{OL} = 8mA	–	0.4	–	0.4	V
V_{OH}	Output High Voltage	V_{CC} = Min., I_{OH} = -4mA	2.4	–	2.4	–	V

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = -55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	TEST CONDITIONS	IDT7MC4005 20ns COM'L.	IDT7MC4005 20ns MIL.	IDT7MC4005 25ns COM'L.	IDT7MC4005 25ns MIL.	IDT7MC4005 30, 35, 45, 55ns COM'L.	IDT7MC4005 30, 35, 45, 55ns MIL.	UNIT
I_{CC1}	Operating Current	F = 0, $\overline{CS}$ = V_{IL} V_{CC} = Max.; Output Open	480	–	480	500	400	440	mA
I_{CC2}	Dynamic Operating Current	V_{CC} = Max.; $\overline{CS}$ = V_{IL}; f = f_{MAX} Output Open	600	–	600	620	500	560	mA
I_{SB}	Standby Supply Current	$\overline{CS}$ = V_{IL}	240	–	240	240	200	220	mA
I_{SB1}	Full Standby Supply Current	$\overline{CS}$ ≥ V_{CC} -0.2V V_{IN} > V_{CC} -0.2V or < 0.2V	80	–	80	80	60	80	mA

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AC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5V ±10%, T_A = −55°C to +125°C and 0°C to +70°C)

SYMBOL	PARAMETER	7MC4005S20 (COM'L.)		7MC4005S25		7MC4005S30		7MC4005S35		7MC4005S45		7MC4005S55		UNIT
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
READ CYCLE														
t_{RC}	Read Cycle Time	20	–	25	–	30	–	35	–	45	–	55	–	ns
t_{AA}	Address Access Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
t_{ACS}	Chip Select Access Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
$t_{CLZ1,2}$(1)	Chip Select to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{OE}	Output Enable to Output Valid	–	15	–	15	–	20	–	20	–	25	–	35	ns
t_{OLZ}(1)	Output Enable to Output in Low Z	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{CHZ}(1)	Chip Deselect to Output in High Z	–	8	–	10	–	13	–	15	–	15	–	20	ns
t_{OHZ}(1)	Output Disable to Output in High Z	–	8	–	15	–	15	–	15	–	15	–	20	ns
t_{OH}	Output Hold from Address Change	5	–	5	–	5	–	5	–	5	–	5	–	ns
t_{PU}(1)	Chip Select to Power Up Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{PD}(1)	Chip Deselect to Power Down Time	–	20	–	25	–	30	–	35	–	45	–	55	ns
WRITE CYCLE														
t_{WC}	Write Cycle Time	17	–	20	–	25	–	30	–	40	–	50	–	ns
t_{CW}	Chip Selection to End of Write	17	–	20	–	25	–	25	–	35	–	50	–	ns
t_{AW}	Address Valid to End of Write	17	–	20	–	25	–	27	–	37	–	50	–	ns
t_{AS}	Address Set-up Time	0	–	0	–	0	–	2	–	2	–	2	–	ns
t_{WP}	Write Pulse Width	17	–	20	–	25	–	25	–	35	–	48	–	ns
t_{WR}	Write Recovery Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{WHZ}(1)	Write Enable to Output in High Z	–	7	–	7	–	10	–	10	–	15	–	25	ns
t_{DW}	Data to Write Time Overlap	10	–	13	–	15	–	15	–	20	–	25	–	ns
t_{DH}	Data Hold from Write Time	0	–	0	–	0	–	0	–	0	–	0	–	ns
t_{OW}(1)	Output Active from End of Write	5	–	5	–	5	–	5	–	5	–	5	–	ns

NOTE:
1. This parameter guaranteed but not tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	10ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

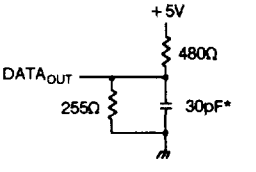


Figure 1. Output Load

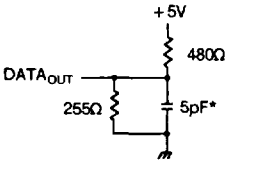
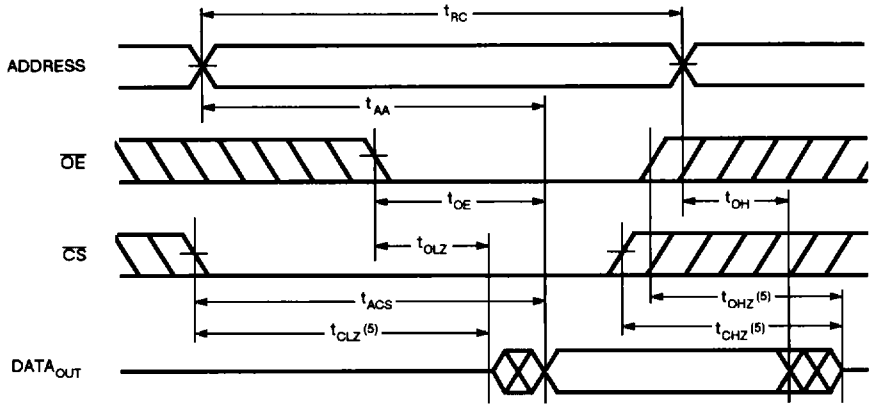


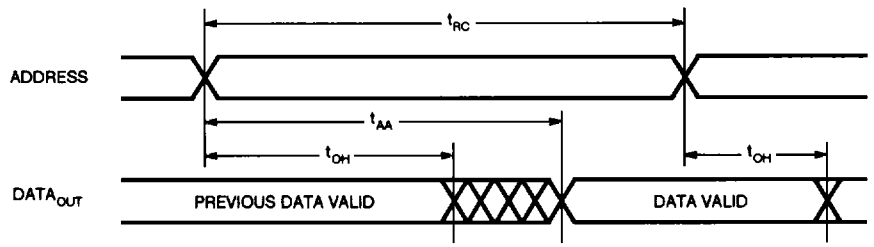
Figure 2. Output Load (for $t_{CLZ1,2}$, t_{OLZ}, $t_{CHZ1,2}$, t_{OHZ}, t_{OW} and t_{WHZ})

* Including scope and jig.

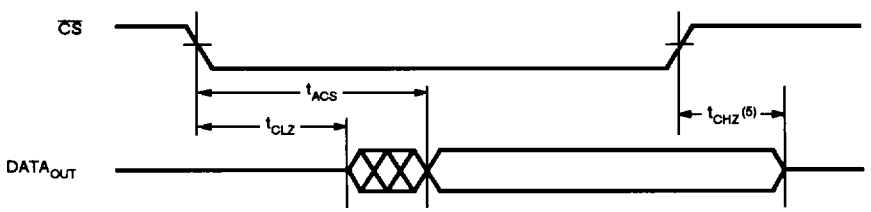
TIMING WAVEFORM OF READ CYCLE NO. 1 (1)



TIMING WAVEFORM OF READ CYCLE NO. 2 (1, 2, 4)



TIMING WAVEFORM OF READ CYCLE NO. 3 (1, 3, 4)



NOTES:

1. $\overline{WE}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

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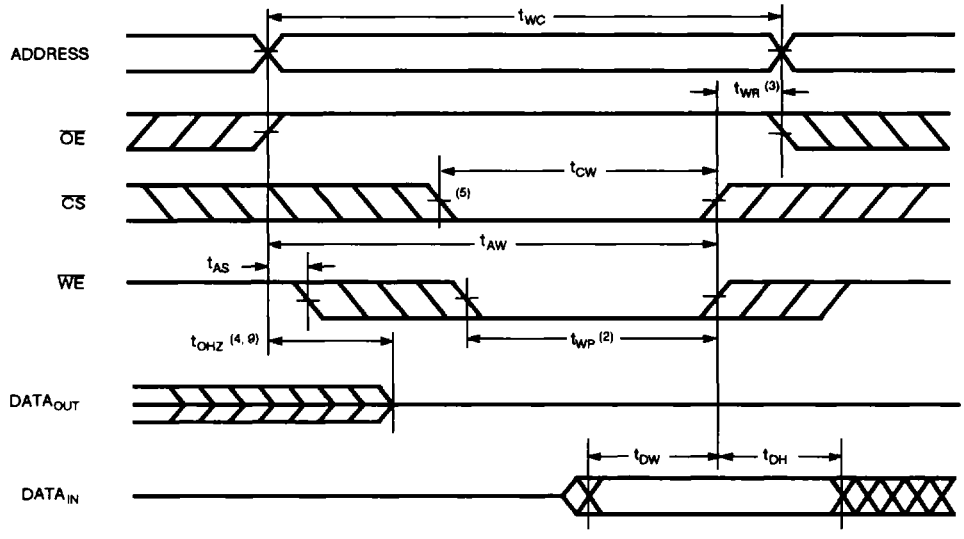
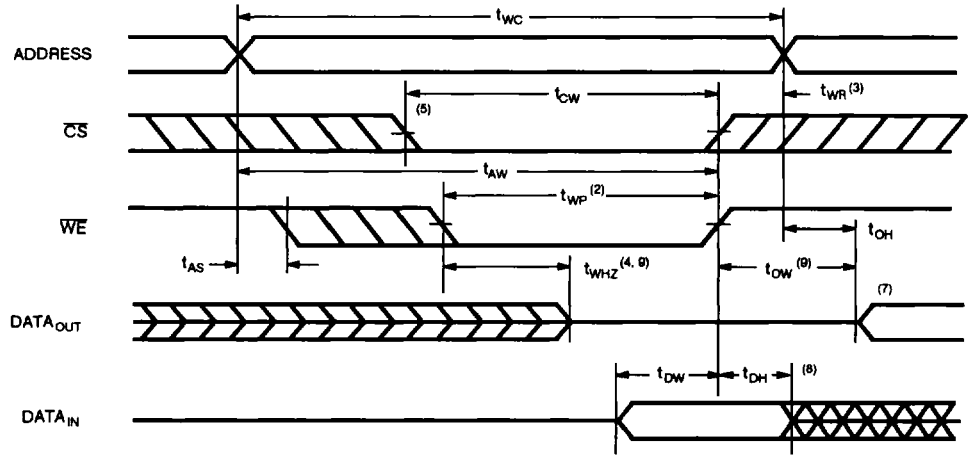
TIMING WAVEFORM OF WRITE CYCLE NO. 1 (1)



TIMING WAVEFORM OF WRITE CYCLE NO. 2 (1, 6)



NOTES:

1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$.
3. t_{WP} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
6. $\overline{OE}$ is continuously low ($\overline{OE}$ = V_{IL}).
7. D_{OUT} is the same phase of write data of this write cycle.
8. If $\overline{CS}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ±200mV from steady state. This parameter is sampled and not 100% tested.

TRUTH TABLE

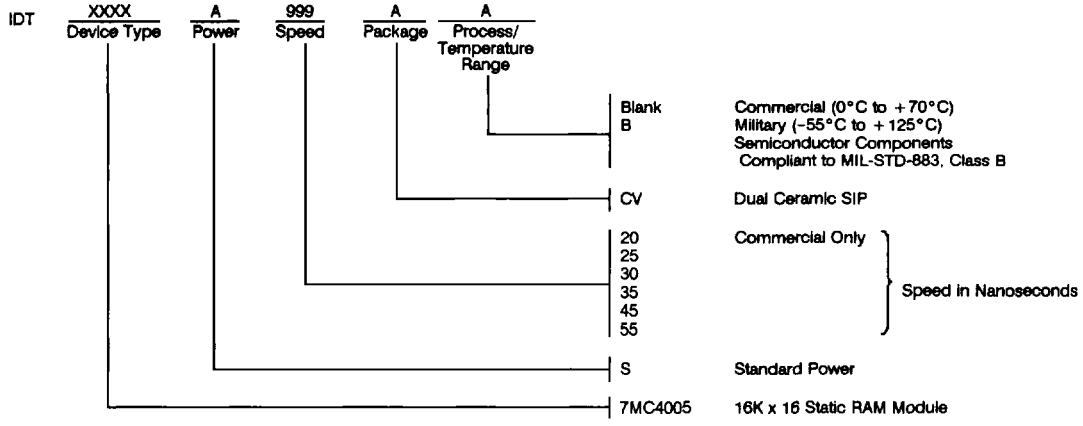
MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	OUTPUT	POWER
Standby	H	X	X	High Z	Standby
Read	L	L	H	D_{OUT}	Active
Write	L	X	L	D_{IN}	Active
Read	L	H	H	High Z	Active

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

SYMBOL	PARAMETER[1]	CONDITIONS	TYP.	UNIT
$C_{IN\ (D)}$	Input Capacitance (Data)	V_{IN} = 0V	20	pF
$C_{IN\ (A)}$	Input Capacitance Address and Control	V_{IN} = 0V	50	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	20	pF

NOTE:
1. This parameter is sampled and not 100% tested.

ORDERING INFORMATION



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