Applications Note:SY7104

High Efficiency 6V, 4A, 1MHz Step Up Regulator

General Description

SY7104 is a high efficiency, current-mode control Boost DC to DC regulator with an integrated 90mΩ $R_{DS(ON)}$ N-channel MOSFET. The fixed 1MHz switching frequency and internal compensation reduce external component count and save the PCB space. The build-in internal soft start circuitry minimizes the inrush current at start-up.

Ordering Information

SY7104□(□□)□

- Temperature Code
- Package Code
- Optional Spec Code

Temperature Range: -40°C to 85°C

Ordering Number	Package type	Note
SY7104DBC	DFN3×3-10	4A

Features

- Wide input range: 2-6V
- 1MHz switching frequency
- Minimum on time: 100ns typical
- Minimum off time: 100ns typical
- Max output voltage: 6V
- Internal 4A switch
- Internal soft start
- Over temperature protection
- Over current protection
- Low $R_{DS(ON)}$: 90mΩ typical
- RoHS Compliant and Halogen Free
- Compact package: DFN3x 3-10

Applications

- 1-cell Li-ion Battery powered applications
- Portable devices

Typical Applications

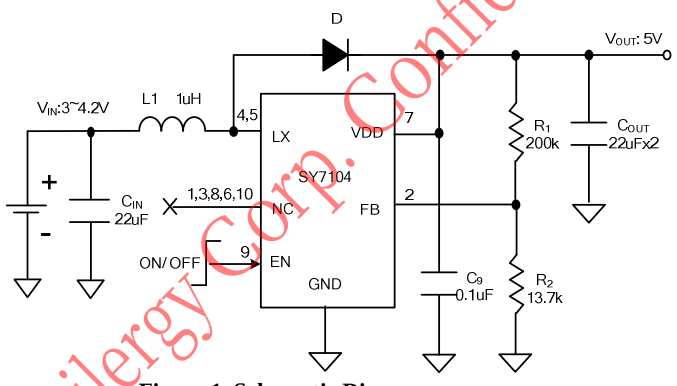


Figure 1. Schematic Diagram

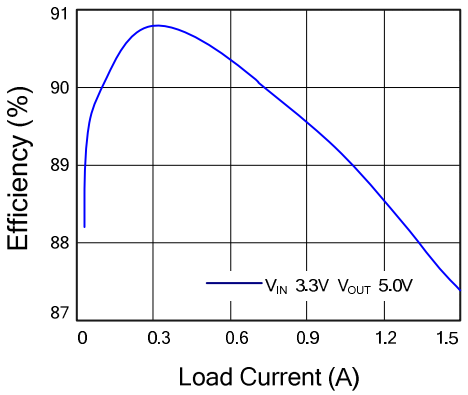
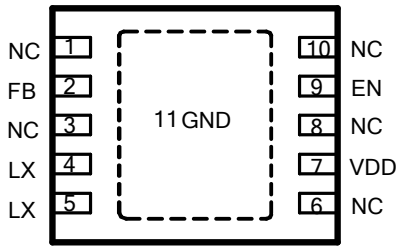


Figure 2. Efficiency vs Load Current

Pinout (top view)



(DFN3×3-10)

Top Mark: **EL*xyz*** (Device code: EL , ***x=year code, y=week code, z= lot number code***)

Pin Name	Pin Number	Pin Description
NC	1,3,6, 8,10	No connection.
GND	11	Ground pin.
LX	4,5	Phase node. Connect an inductor across the power input and this pin.
FB	2	Feedback pin. Connect a resistor R1 between V_{OUT} and FB, and a resistor R2 across FB and GND to program the output voltage: V_{OUT}=0.6V×(R1/R2+1)
EN	9	Enable control. Pull high to turn on. Do not leave it floating.
VDD	7	IC power supply input

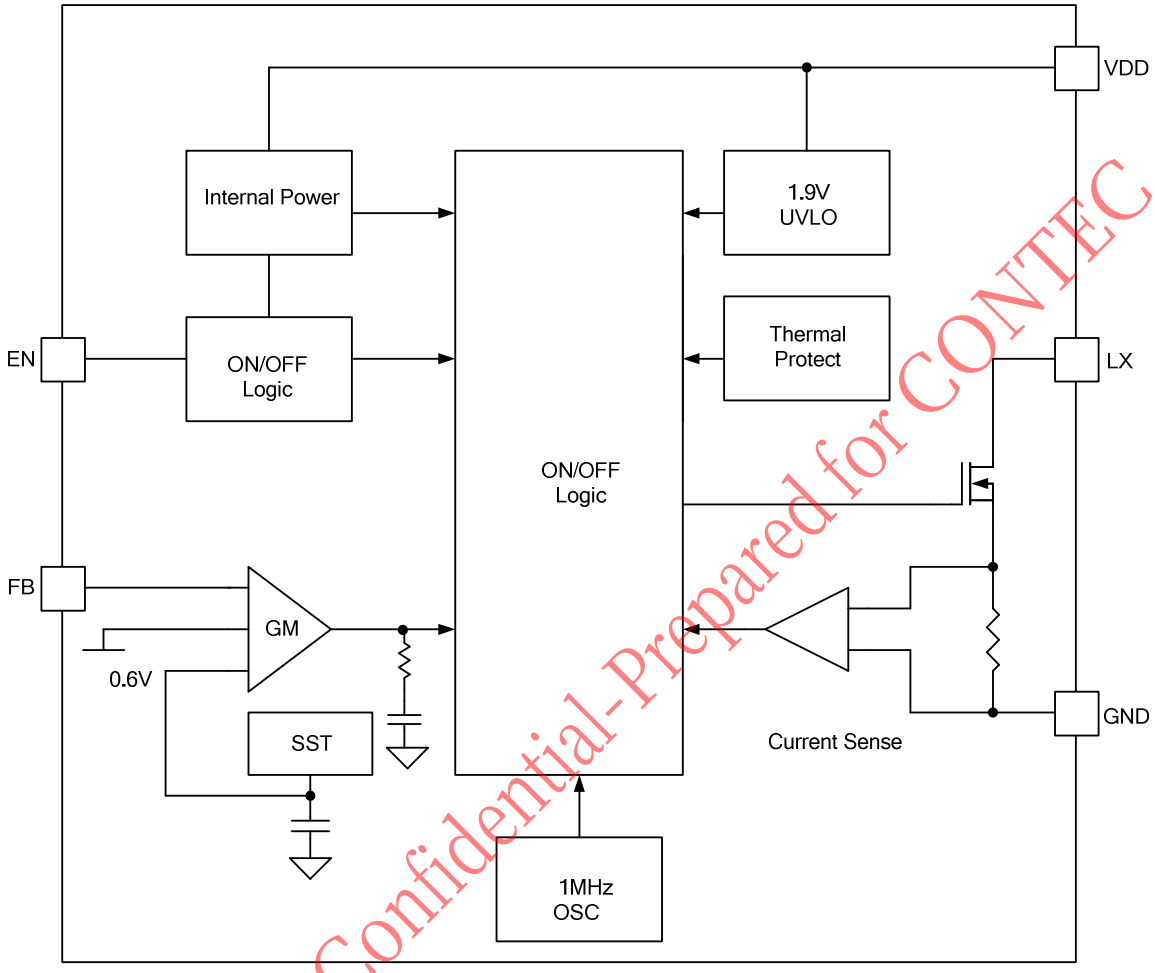
Absolute Maximum Ratings (Note 1)

FB pin---------- -0.3V to 4V
All other pins---------- -0.3V to 7V
Power Dissipation, P_D @ T_A = 25°C DFN3×3-10, ----------2.6W
Package Thermal Resistance (Note 2)
θ_{JA} ----------38°C/W
θ_{JC} ---------- 8°C/W
Junction Temperature Range ---------- -40 to 150°C
Lead Temperature (Soldering, 10 sec.) ---------- 260°C
Storage Temperature Range ---------- -65°C to 150°C
Dynamic LX voltage in 50ns duration ---------- VIN+3V

Recommended Operating Conditions (Note 3)

FB pin---------- -0.3V to 3.6V
VDD pin---------- ---------- 2V to 6V
All other pins---------- ---------- 0V to 6V
Junction Temperature Range ---------- -40°C to 125°C
Ambient Temperature Range ---------- -40°C to 85°C

Block Diagram



Electrical Characteristics

(V_{IN} = 3V, V_{OUT}=5V, I_{OUT}=1A, T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range	V_{IN}		2		6	V
Quiescent Current	I_Q	V_{FB}=0.66V		100		μA
Shutdown Current	I_{SHDN}	EN=0			10	μA
Low Side Main FET R_{ON}	$R_{DS(ON)}$			90		mΩ
Main FET Current Limit	I_{LIM}		4			A
Switching Frequency	F_{SW}			1		MHz
Feedback Reference Voltage	V_{REF}		0.588	0.6	0.612	V
VDD UVLO Rising Threshold	V_{IN_UVLO}				1.9	V
UVLO Hysteresis	V_{UVLO_HYS}			0.1		V
Thermal Shutdown Temperature	T_{SD}			150		°C
EN Rising Threshold	V_{ENH}		1.5			V
EN Falling Threshold	V_{ENL}				0.4	V
EN Pin Input Current	I_{EN}		0		100	nA

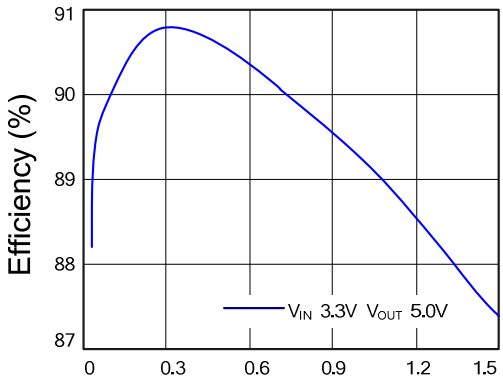
Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: θJA is measured in the natural convection at TA = 25°C on a low effective single layer thermal conductivity test board of JEDEC 51-3 thermal measurement standard. Test condition: Device mounted on 2" x 2" FR-4 substrate PCB, 2oz copper, with minimum recommended pad on top layer and thermal vias to bottom layer ground plane.

Note 3: The device is not guaranteed to function outside its operating conditions

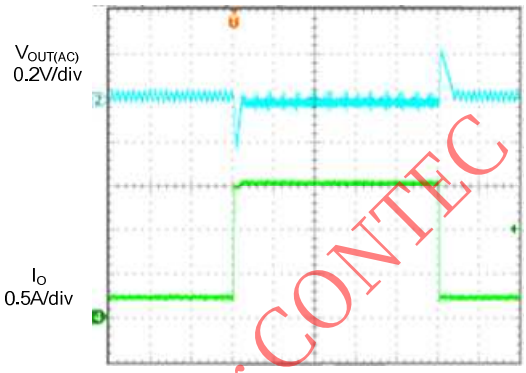
Typical Performance Characteristics

Efficiency vs Load Current



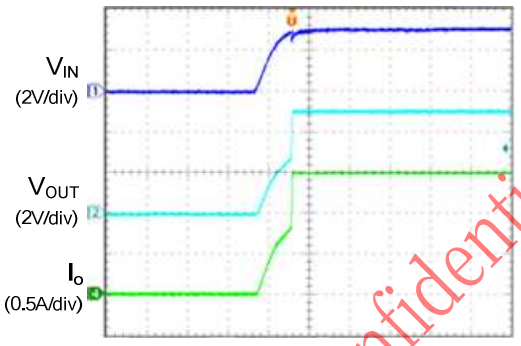
Load Transient

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=0.15~1.5A)



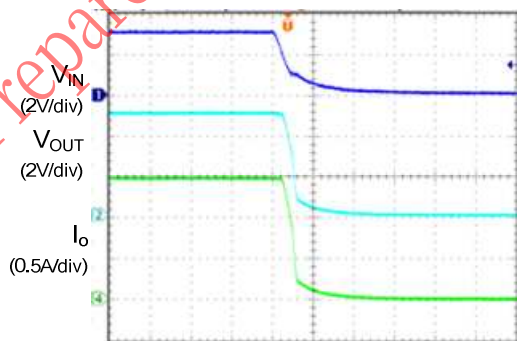
Startup from V_{IN}

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.5A)



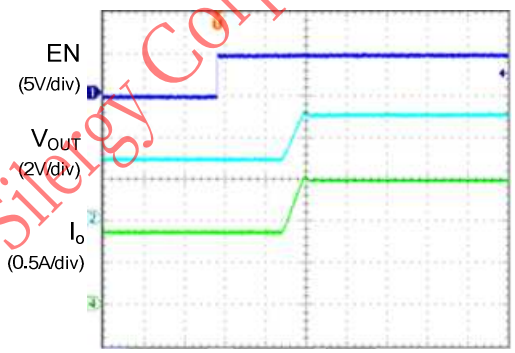
Shutdown from V_{IN}

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.5A)



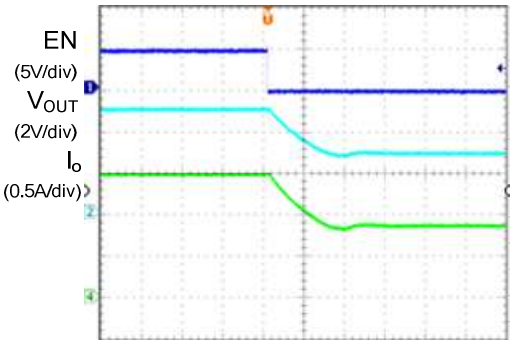
Startup from Enable

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.5A)

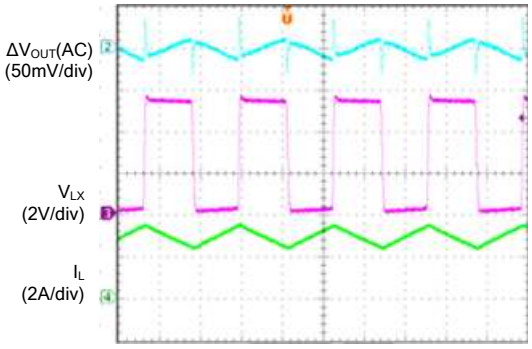


Shutdown from Enable

(V_{IN}=3.3V, V_{OUT}=5V,I_{load}=1.5A)

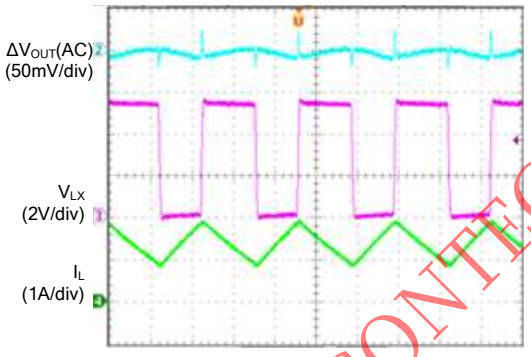


Output Ripple
(V_{IN}=3.3V, V_{OUT}=5V,I_O=1.5A)



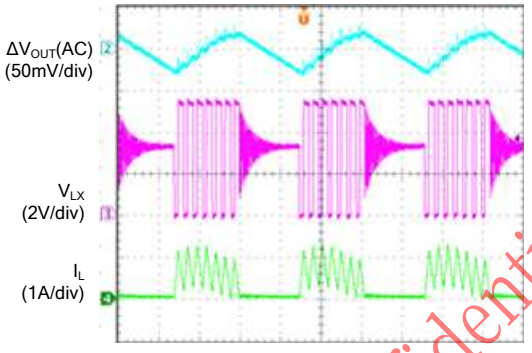
Time(400ns/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=5V,I_O=0.75A)



Time(400ns/div)

Output Ripple
(V_{IN}=3.3V, V_{OUT}=5V,I_O=0.15A)



Time(4us/div)

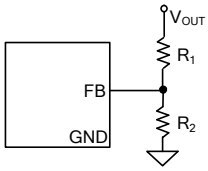
Applications Information

Because of the high integration in SY7104, the application circuit based on this regulator IC is rather simple. Only input capacitor C_{IN}, output capacitor C_{OUT}, inductor L and feedback resistors (R_1 and R_2) need to be selected for the targeted applications.

Feedback resistor divider R_1 and R_2

Choose R_1 and R_2 to program the proper output voltage. To minimize the power consumption under light load, it is desirable to choose large resistance values for both R_1 and R_2. A value between 10k and 1M is recommended for both resistors. If R_1=200k is chosen, then R_2 can be calculated to be:

$$R_2 = \frac{0.6R_1}{V_{OUT} - 0.6} (\Omega)$$



Input capacitor C_{IN}

The ripple current through input capacitor is calculated as:

$$I_{CIN\_RMS} = \frac{V_{IN} \cdot (V_{OUT} - V_{IN})}{2\sqrt{3} \cdot L \cdot F_{SW} \cdot V_{OUT}} (A)$$

To minimize the potential noise problem, place a typical X5R or better grade ceramic capacitor really close to the VDD and GND pins. Care should be taken to minimize the loop area formed by C_{IN}, and VDD/GND pins. In this case a 22uF low ESR ceramic capacitor is recommended.

Output capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into account when selecting this capacitor. For the best performance, it is recommended to use X5R or better grade ceramic capacitor with 10V rating and more than two 22uF capacitors.

Boost inductor L

There are several considerations in choosing this inductor.

1) Choose the inductance to provide the desired ripple current. It is suggested to choose the ripple current to be about 40% of the maximum average input current. The inductance is calculated as:

$$L = \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{F_{SW} \times I_{OUT\_MAX} \times 40\%} (H)$$

where F_{SW} is the switching frequency and I_{OUT_MAX} is the maximum load current.

SY7104 regulator IC is less sensitive to the ripple current variations. Consequently, the final choice of inductance can be slightly off the calculation value without significantly impacting the performance.

2) The saturation current rating of an inductor must be selected to guarantee an adequate margin to the peak inductor current under full load conditions.

$$I_{SAT\_MIN} > \left(\frac{V_{OUT}}{V_{IN}}\right) \times I_{OUT\_MAX} + \left(\frac{V_{IN}}{V_{OUT}}\right)^2 \frac{(V_{OUT} - V_{IN})}{2 \times F_{SW} \times L}$$

3) The DCR of the inductor and the core loss at the switching frequency must be low enough to achieve the desired efficiency requirement. It is desirable to choose an inductor with DCR<10mΩ to achieve a good overall efficiency.

Enable Operation

Pulling the EN pin low (<0.4V) will shut down the device. During the shut down mode, the SY7104 shut down current drops to lower than 10μA. Driving the EN pin high (>1.5V) will turn on the IC again.

Rectifier Diode Selection

Schottky diode is a good choice for high efficiency operation because of its low forward voltage drop and fast reverse recovery. The maximum current rating of the diode must be higher than maximum input current. And the average current rating of the diode must be higher than the output current.

Layout Design

The layout design of SY7104 regulator is highly simplified. To achieve a higher efficiency and better noise immunity, following components should be placed close to the IC: C_{IN}, L, R_1 and R_2.

1) It is desirable to maximize the PCB copper area connecting to GND pin to achieve a better thermal performance and noise immunity. If the board space allowed, a designated ground plane layer is highly recommended.

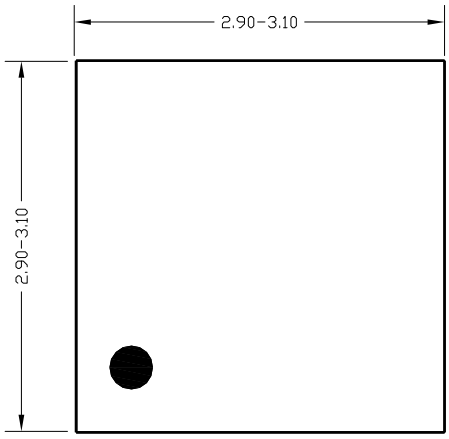
2) C_{IN} must be close to VDD and GND pins. The loop area formed by C_{OUT}, LX and GND pins must be minimized.

3) The PCB copper area associated with LX pin must be minimized to improve the noise immunity.

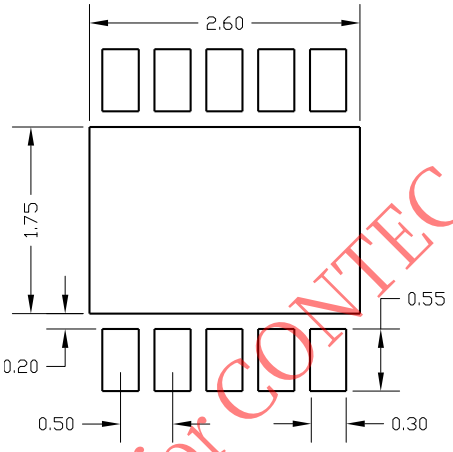
4) The components R_1 and R_2, and the trace connecting to the FB pin must NOT be adjacent to the LX node on the PCB layout to minimize the noise coupling to FB pin.

5) If the system chip interfacing with the EN pin has a high impedance state at shutdown mode and the VDD pin is connected directly to a power source such as a Li-Ion battery, it is desirable to add a pull down 1MΩ resistor across the EN and GND pins to prevent the noise from falsely turning on the regulator at shutdown mode.

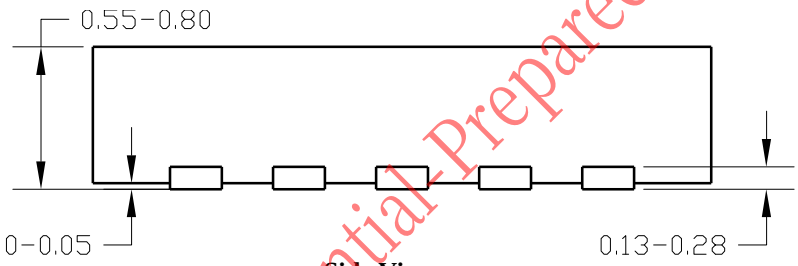
DFN3x3-10 Package outline



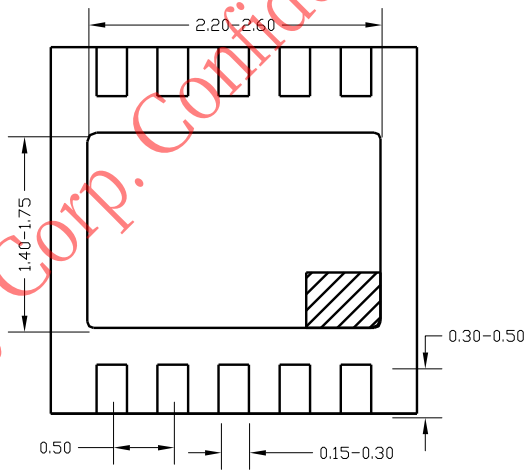
Top View

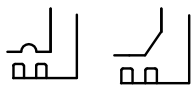


PCB layout (recommended)



Side View





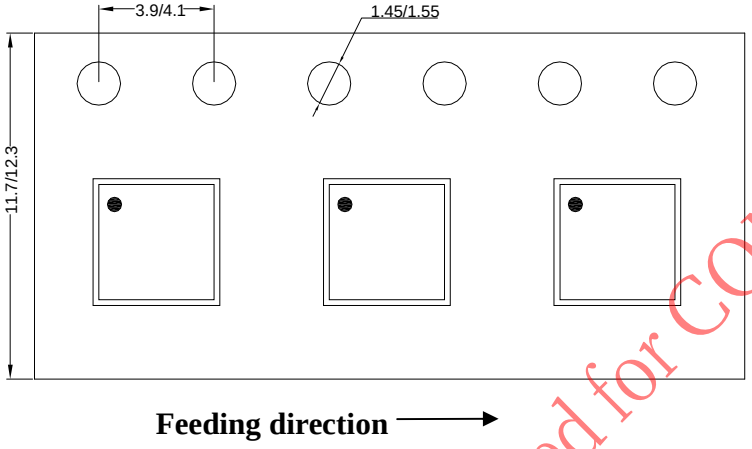
Detail A
Pin1 identifier: two options

Bottom View

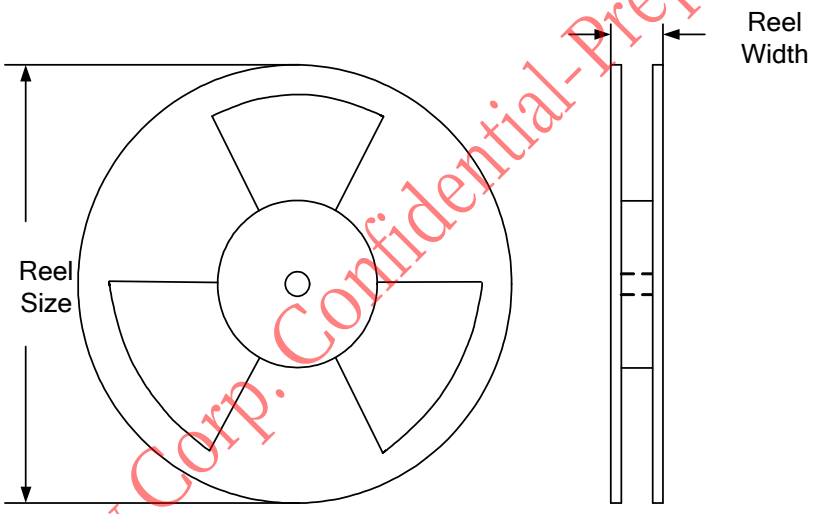
Notes: All dimensions are in millimeters and exclude mold flash & metal burr.

Taping & Reel Specification

1. DFN3x3-10 taping orientation



2. Carrier Tape & Reel specification for packages



Package types	Tape width (mm)	Pocket pitch(mm)	Reel size (Inch)	Reel width(mm)	Trailer length(mm)	Leader length (mm)	Qty per reel
DFN3x3	10	8	13"	12.4	400	400	5000

3. Others: NA