

Small Signal Schottky (double) diodes

BAR40S3/BAR40AS3

BAR40CS3/BAR40SS3

Description

Planar silicon Schottky barrier diodes encapsulated in a SOT-323 small plastic SMD package. Single diodes and double diodes with different pinning are available.

Features

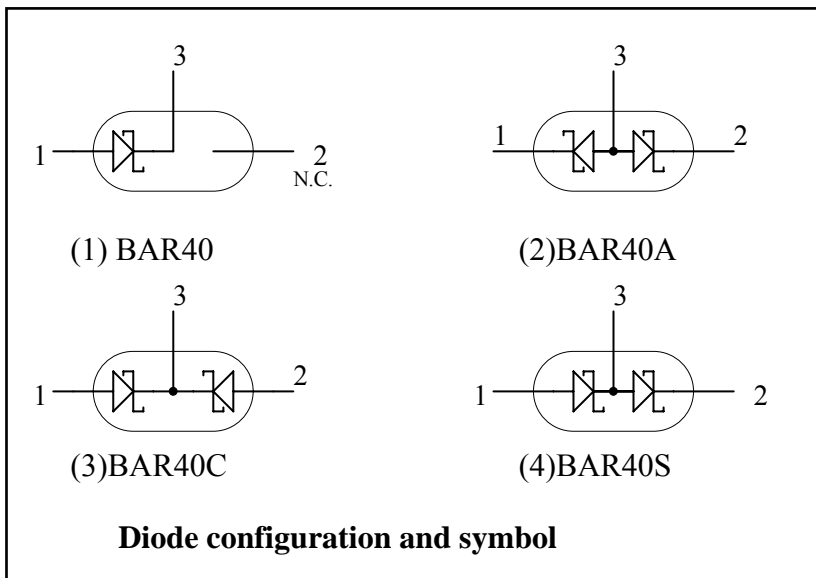
- Very small conduction losses
- Low forward voltage drop
- Small plastic SMD package
- Pb-free package

Applications

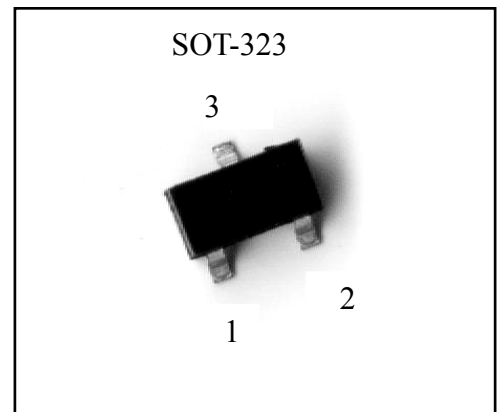
- Ultra high-speed switching
- Voltage clamping
- Protection circuits
- Blocking diodes

Pinning

Pin	Description			
	BAR40	BAR40A	BAR40C	BAR40S
1	A	K1	A1	A1
2	NC	K2	A2	K2
3	K	A1,A2	K1,K2	K1,A1



Outline



Marking:

Type	Marking Code
BAR40 S3	B4
BAR40AS3	B7
BAR40CS3	5C
BAR40SS3	B8



Absolute Maximum Ratings

- Maximum Temperatures
Storage Temperature Tstg..... -65~+150 °C
Junction Temperature Tj-55~ +125°C
- Maximum Power Dissipation
Total Power Dissipation (Ta=25°C) Ptot (Note) 200 mW
- Maximum Voltages and Currents (Ta=25°C)
Repetitive Peak Reverse Voltage VRRM..... 40 V
Continuous Forward Current IF 200 mA
Repetitive Peak Forward Current(tp≤1s,duty cycle≤0.5)..... 300mA
Non-repetitive Peak Forward Current (tp<10ms, sinusoidal) IFSM 600 mA

Note: for double diodes, Ptot is the total power dissipation of both diodes.

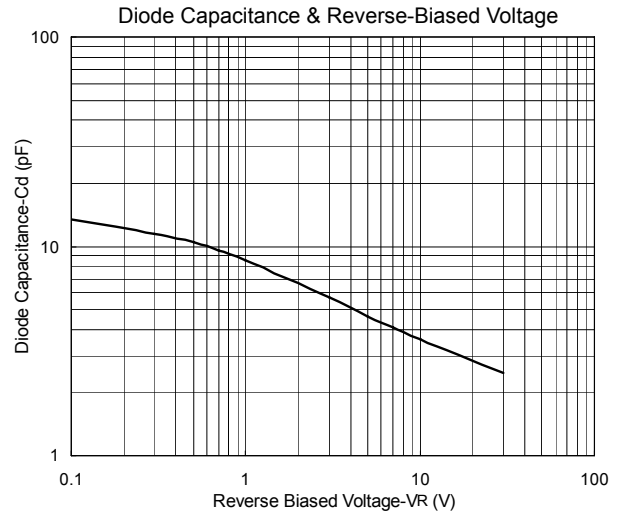
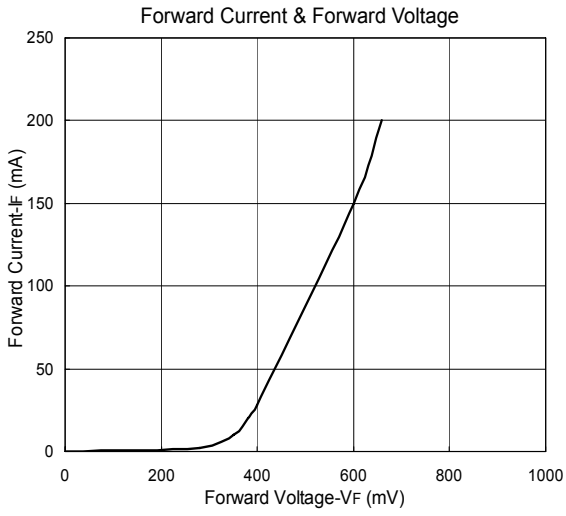
Characteristics (Ta=25°C)

Characteristic	Symbol	Condition	Min.	Max.	Unit
Reverse Breakdown Voltage	VBR	IR=100μA	40	-	V
Forward Voltage (Note 1)	VF(1)	IF=1mA	-	320	mV
	VF(2)	IF=40mA	-	500	mV
	VF(3)	IF=100mA	-	550	mV
Reverse Leakage Current (Note 2)	IR	VR=30V, Tj=25°C	-	200	nA
Diode Capacitance	CD	VR=1V, f=1MHz	-	10	pF
Reverse Recovery Time	trr	IF=IR=10mA RL=100Ω measured at IR=1mA	-	5	ns

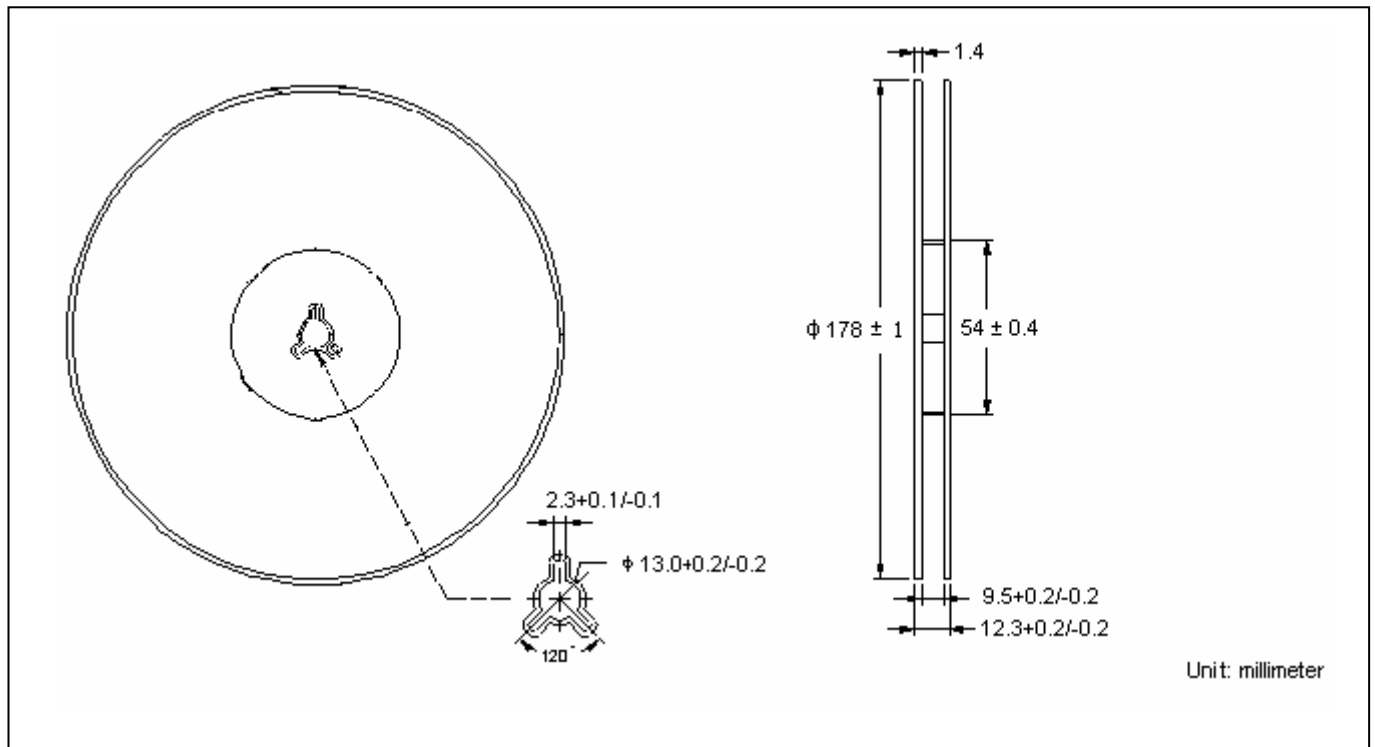
Notes: 1.pulse test, tp=380μs,duty cycle<2%.
2.pulse test, tp=5ms,duty cycle<2%.



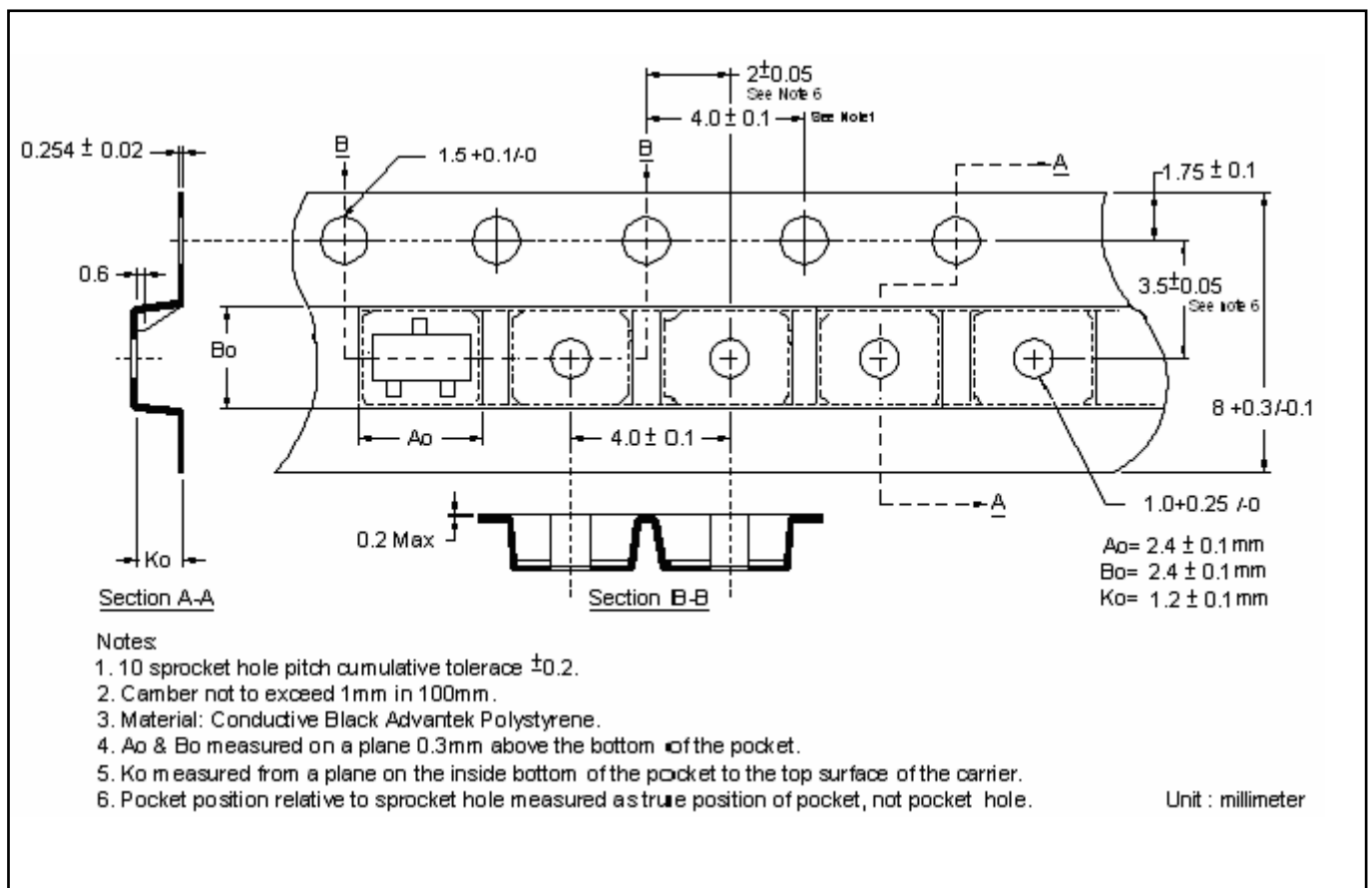
Characteristic Curves



Reel Dimension



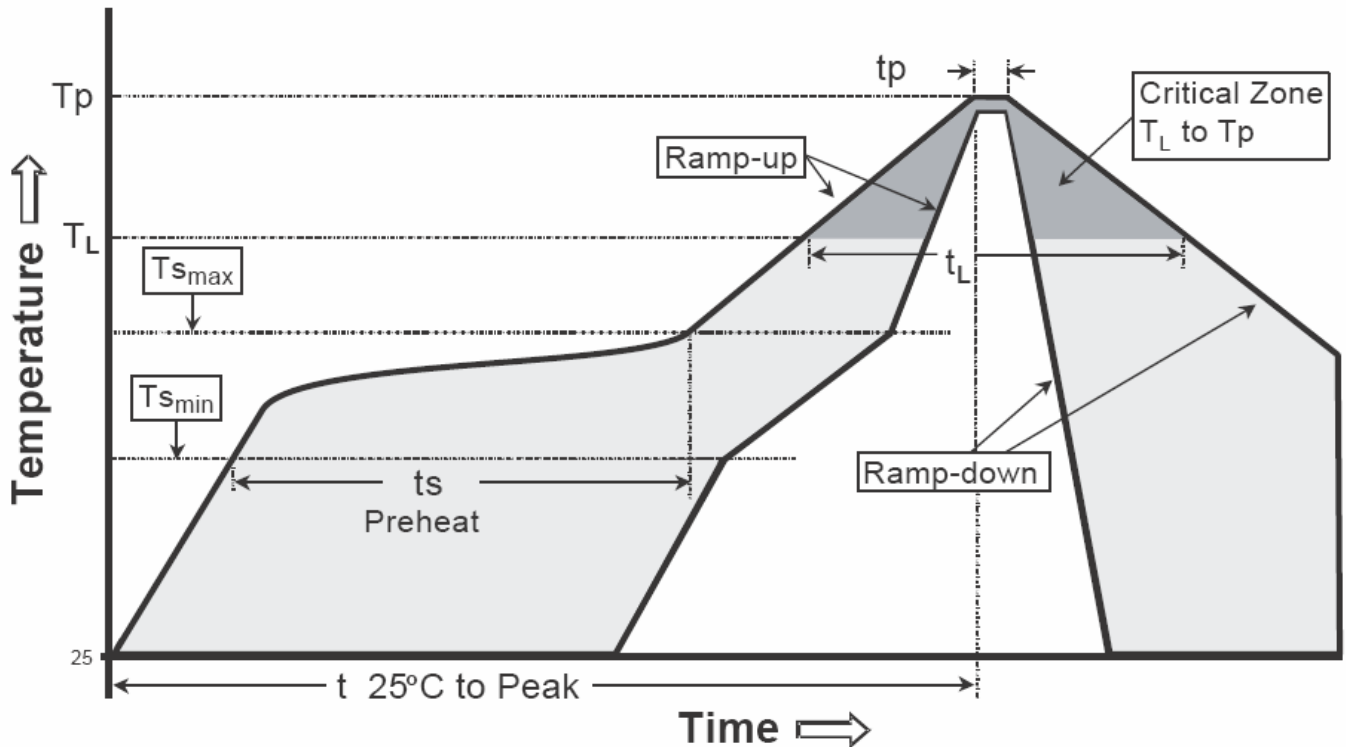
Carrier Tape Dimension



Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

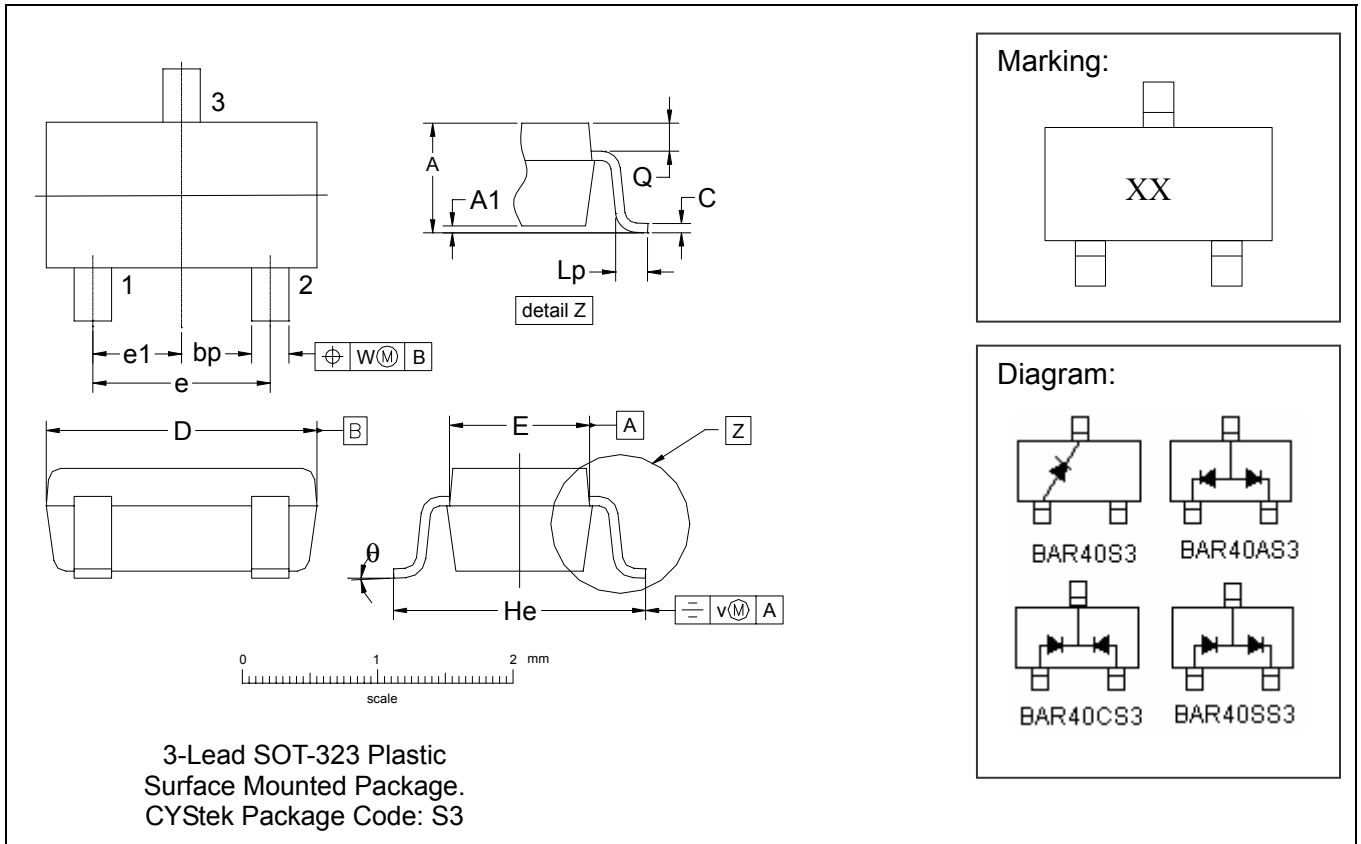
Recommended temperature profile for IR reflow



Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (T _{smax} to T _p)	3°C/second max.	3°C/second max.
Preheat		
-Temperature Min(T _{s min})	100°C	150°C
-Temperature Max(T _{s max})	150°C	200°C
-Time(t _{s min} to t _{s max})	60-120 seconds	60-180 seconds
Time maintained above:		
-Temperature (T _L)	183°C	217°C
- Time (t _L)	60-150 seconds	60-150 seconds
Peak Temperature(T _P)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-323 Dimension



- BAR40 S3 : Single Diode (Marking Code B4)
- BAR40AS3 : Common Anode. (Marking Code B7)
- BAR40CS3 : Common Cathode. (Marking Code 5C)
- BAR40SS3 : Series Connected. (Marking Code B8)

*: Typical

DIM	Inches		Millimeters		DIM	Inches		Millimeters	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	0.0315	0.0433	0.80	1.10	e1	0.0256	-	0.65	-
A1	0.0000	0.0039	0.00	0.10	He	0.0787	0.0886	2.00	2.25
bp	0.0118	0.0157	0.30	0.40	Lp	0.0059	0.0177	0.15	0.45
C	0.0039	0.0098	0.10	0.25	Q	0.0051	0.0091	0.13	0.23
D	0.0709	0.0866	1.80	2.20	v	0.0079	-	0.2	-
E	0.0453	0.0531	1.15	1.35	w	0.0079	-	0.2	-
e	0.0512	-	1.3	-	θ	-	-	10°	0°

- Notes: 1.Controlling dimension: millimeters.
 2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
 3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material:

- Lead: Pure tin plated.
- Mold Compound: Epoxy resin family, flammability solid burning class: UL94V-0.

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