Document Title

128Kx36-Bit Synchronous Pipelined Burst SRAM

Revision History

Rev. No	History	Draft Date	Remark
0.0	Initial draft	April . 14. 1998	Preliminary
0.1	Change Undershoot spec from -3.0V(pulse width≤20ns) to -2.0V(pulse width≤t_{CYC}/2) Add Overshoot spec 4.6V(pulse width≤t_{CYC}/2) Change V_{IH} max from 5.5V to V_{DD}+0.5V	April . 20. 1998	Preliminary
0.2	Change t_{CD} from 3.2ns to 3.1ns at bin -50. Change t_{OE} from 3.2ns to 3.1ns at bin -50. Change setup from 1.5ns to 1.4ns at bin -50. Change t_{CYC} from 5.5ns to 5.4ns at bin -55.	May . 23. 1998	Preliminary
0.3	Change t_{CD} from 3.5ns to 3.1ns at bin -55. Change t_{OE} from 3.5ns to 3.1ns at bin -55. Change setup from 1.5ns to 1.4ns at bin -55.	May . 25. 1998	Preliminary
0.4	Add t_{CYC} 175Mhz. Change I_{SB2} from 20mA to 30mA.	May . 30. 1998	Preliminary
0.5	Modify DC characteristics(Input Leakage Current test Conditions) form V_{DD}=V_{SS} to V_{DD} to Max.	June. 08. 1998	Preliminary
1.0	Final Release.	June. 15 . 1998	Final
2.0	Add t_{CYC} 225Mhz.	July. 10 . 1998	Final
3.0	Add V_{DDQ} Supply voltage(2.5V)	Dec. 02. 1998	Final
4.0	Change t_{CD} , t_{OE} from 3.1ns to 2.8ns at bin -44. Change t_{HZC} max , t_{HZOE} max from 3.0ns to 2.8ns at bin -44.	Mar. 04. 1999	Fianl
5.0	Add t_{CYC} 250Mhz.	April. 10. 1999	Final
6.0	Change t_{AH}, t_{SH}, t_{DH}, t_{WH}, t_{ADVH}, t_{CSH} from 0.5ns to 0.4ns at bin -40.	May. 03. 1999	Final
7.0	1. Change t_{AS}, t_{SS}, t_{DS}, t_{WS}, t_{ADVS}, t_{CSS} from 1.4ns to 1.2ns at bin -44. 2. Change t_{AH}, t_{SH}, t_{DH}, t_{WH}, t_{ADVH}, t_{CSH} from 0.5ns to 0.4ns at bin -44. 3. Change t_{AS}, t_{SS}, t_{DS}, t_{WS}, t_{ADVS}, t_{CSS} from 1.2ns to 0.8ns at bin -40. 4. Change t_{AH}, t_{SH}, t_{DH}, t_{WH}, t_{ADVH}, t_{CSH} from 0.4ns to 0.3ns at bin -40.	May. 10. 1999	Final
8.0	1. Change I_{SB} value from 120mA to 130mA at -57	June. 24. 1999	Final
9.0	Remove 119BGA(7x17 Ball Grid Array Package) .	Nov. 26. 1999	Final

128Kx36-Bit Synchronous Pipelined Burst SRAM

FEATURES

- Synchronous Operation.
- 2 Stage Pipelined operation with 4 Burst.
- On-Chip Address Counter.
- Self-Timed Write Cycle.
- On-Chip Address and Control Registers.
- V_{DD}= 3.3V+0.165V/-0.165V Power Supply.
- V_{DDQ} Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O.
- 5V Tolerant Inputs Except I/O Pins.
- Byte Writable Function.
- Global Write Enable Controls a full bus-width write.
- Power Down State via ZZ Signal.
- LBO Pin allows a choice of either a interleaved burst or a linear burst.
- Three Chip Enables for simple depth expansion with No Data Contention ; 2cycle Enable, 1cycle Disable.
- Asynchronous Output Enable Control.
- ADSP, ADSC, ADV Burst Control Pins.
- TTL-Level Three-State Output.
- 100-TQFP-1420A Package .

FAST ACCESS TIMES

PARAMETER	Symbol	-40	-44	-50	-55	-57	Unit
Cycle Time	t_{CYC}	4.0	4.4	5.0	5.4	5.7	ns
Clock Access Time	t_{CD}	2.5	2.8	3.1	3.1	3.3	ns
Output Enable Access Time	t_{OE}	2.8	2.8	3.1	3.1	3.3	ns

GENERAL DESCRIPTION

The KM736V799 is a 4,718,592-bit Synchronous Static Random Access Memory designed for high performance second level cache of Pentium and Power PC based System.

It is organized as 128K words of 36bits and integrates address and control registers, a 2-bit burst address counter and added some new functions for high performance cache RAM applications; GW, BW, LBO, ZZ. Write cycles are internally self-timed and synchronous.

Full bus-width write is done by GW, and each byte write is performed by the combination of WEx and BW when GW is high. And with CS_1 high, ADSP is blocked to control signals.

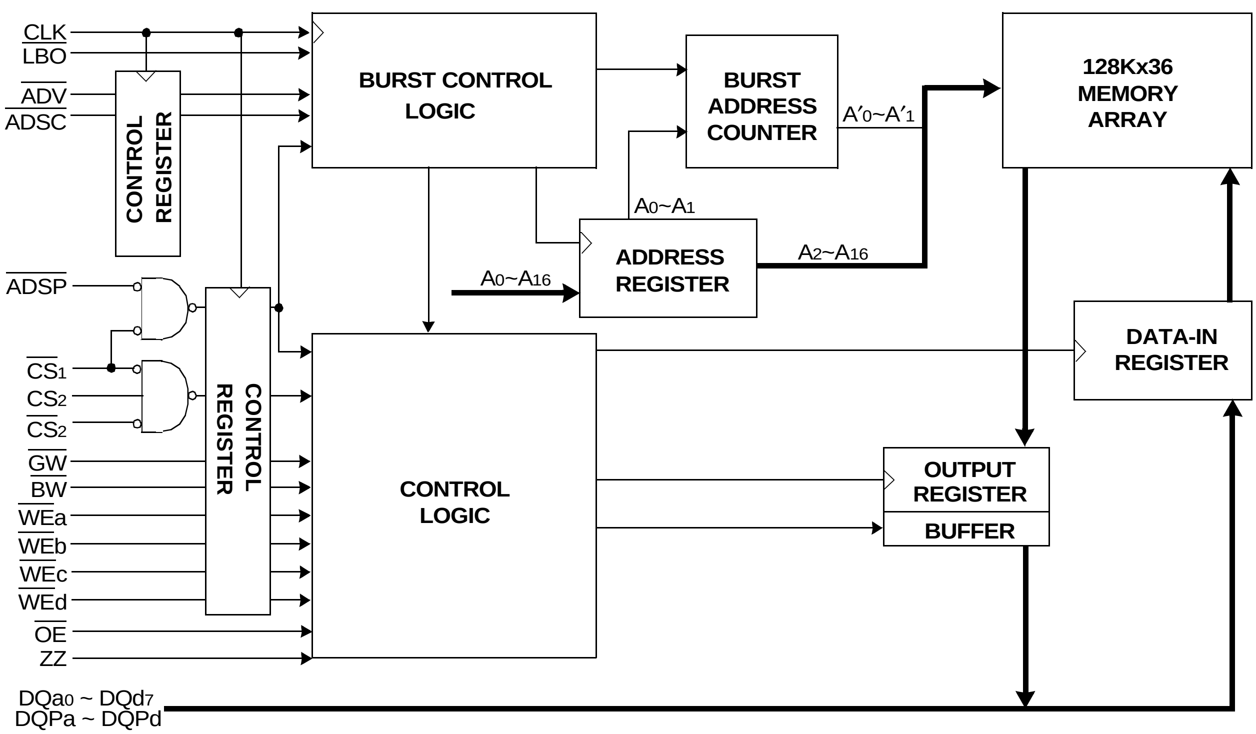
Burst cycle can be initiated with either the address status processor(ADSP) or address status cache controller(ADSC) inputs. Subsequent burst addresses are generated internally in the system′s burst sequence and are controlled by the burst address advance(ADV) input.

LBO pin is DC operated and determines burst sequence(linear or interleaved).

ZZ pin controls Power Down State and reduces Stand-by current regardless of CLK.

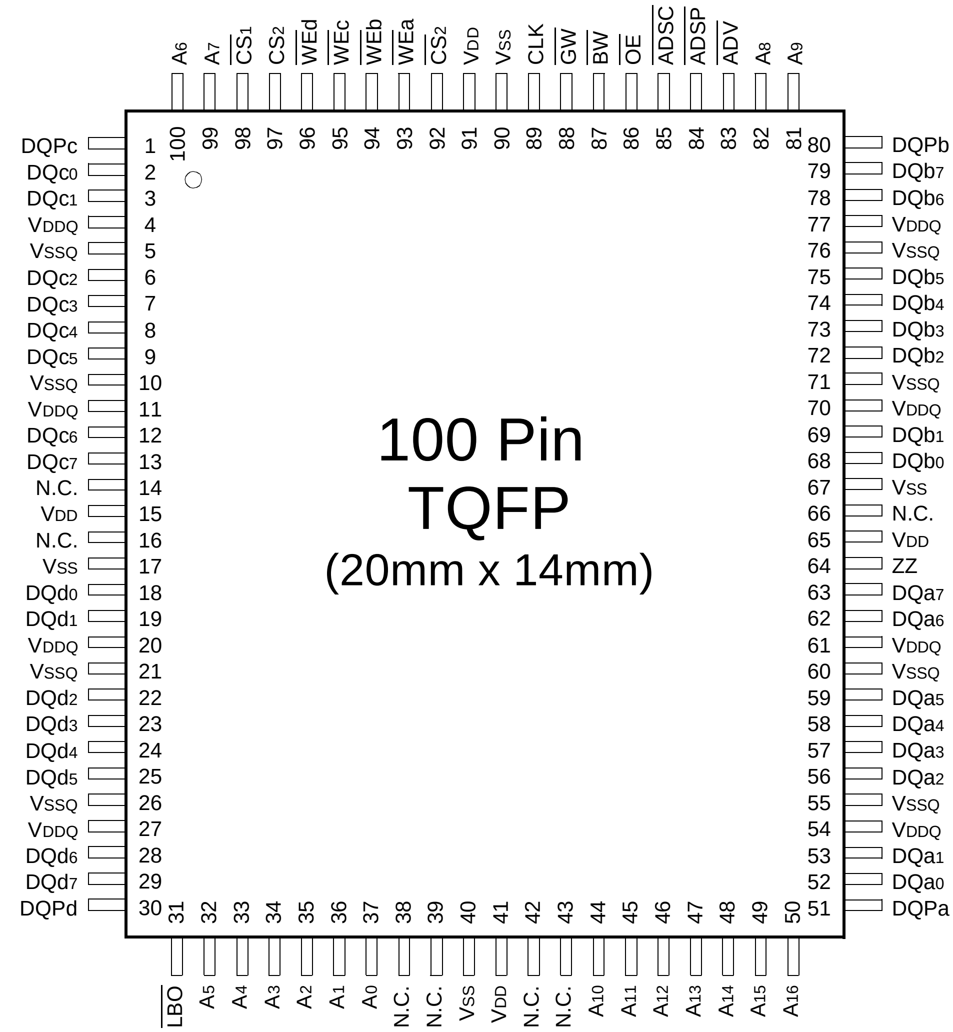
The KM736V799 is fabricated using SAMSUNG′s high performance CMOS technology and is available in a 100pin TQFP package. Multiple power and ground pins are utilized to minimize ground bounce.

LOGIC BLOCK DIAGRAM



SAMSUNG ELECTRONICS

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A_0 - A_{16}	Address Inputs	32,33,34,35,36,37 44,45,46,47,48,49 50,81,82,99,100	V_{DD} V_{SS}	Power Supply(+3.3V) Ground	15,41,65,91 17,40,67,90
ADV ADSP ADSC	Burst Address Advance Address Status Processor Address Status Controller	83 84 85	N.C.	No Connect	14,16,38,39,42,43,66
CLK CS_1 CS_2 CS_2	Clock Chip Select Chip Select Chip Select	89 98 97 92	DQa_0~a_7 DQb_0~b_7 DQc_0~c_7 DQd_0~d_7 $DQPa$~P_d	Data Inputs/Outputs	52,53,56,57,58,59,62,63 68,69,72,73,74,75,78,79 2,3,6,7,8,9,12,13 18,19,22,23,24,25,28,29 51,80,1,30
WEx(x=a,b,c,d) OE GW	Byte Write Inputs Output Enable Global Write Enable	93,94,95,96 86 88	V_{DDQ}	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
BW ZZ LBO	Byte Write Enable Power Down Input Burst Mode Control	87 64 31	V_{SSQ}	Output Ground	5,10,21,26,55,60,71,76

SAMSUNG ELECTRONICS

FUNCTION DESCRIPTION

The KM736V799 is a synchronous SRAM designed to support the burst address accessing sequence of the P6 and Power PC based microprocessor. All inputs (with the exception of OE, LBO and ZZ) are sampled on rising clock edges. The start and duration of the burst access is controlled by ADSC, ADSP and ADV and chip select pins.
The accesses are enabled with the chip select signals and output enabled signals. Wait states are inserted into the access with ADV.

When ZZ is pulled high, the SRAM will enter a Power Down State. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2cycles of wake up time. ZZ pin is pulled down internally.

Read cycles are initiated with ADSP(regardless of WEx and ADSC)using the new external address clocked into the on-chip address register whenever ADSP is sampled low, the chip selects are sampled active, and the output buffer is enabled with OE. In read operation the data of cell array accessed by the current address, registered in the Data-out registers by the positive edge of CLK, are carried to the Data-out buffer by the next positive edge of CLK. The data, registered in the Data-out buffer, are projected to the output pins. ADV is ignored on the clock edge that samples ADSP asserted, but is sampled on the subsequent clock edges. The address increases internally for the next access of the burst when WEx are sampled High and ADV is sampled low. And ADSP is blocked to control signals by disabling CS_1.

All byte write is done by GW(regaedless of BW and WEx.), and each byte write is performed by the combination of BW and WEx when GW is high.
Write cycles are performed by disabling the output buffers with OE and asserting WEx. WEx are ignored on the clock edge that samples ADSP low, but are sampled on the subsequent clock edges. The output buffers are disabled when WEx are sampled Low(regaedless of OE). Data is clocked into the data input register when WEx sampled Low. The address increases internally to the next address of burst, if both WEx and ADV are sampled Low. Individual byte write cycles are performed by any one or more byte write enable signals(WEa, WEb, WEc or WEd) sampled low. The WEa control DQa_0 ~ DQa_7 and DQPa, WEb controls DQb_0 ~ DQb_7 and DQPb, WEc controls DQc_0 ~ DQc_7 and DQPc, and WEd control DQd_0 ~ DQd_7 and DQPd. Read or write cycle may also be initiated with ADSC, instead of ADSP. The differences between cycles initiated with ADSC and ADSP as are follows;

ADSP must be sampled high when ADSC is sampled low to initiate a cycle with ADSC.
WEx are sampled on the same clock edge that sampled ADSC low(and ADSP high).

Addresses are generated for the burst access as shown below, The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion. The burst sequence is determined by the state of the LBO pin. When this pin is Low, linear burst sequence is selected. When this pin is High, Interleaved burst sequence is selected.

BURST SEQUENCE TABLE

(Interleaved Burst)

LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	0	0	1	1	1	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	1	0	0	1	0	0

(Linear Burst)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A_1	A_0	A_1	A_0	A_1	A_0	A_1	A_0
First Address		0	0	0	1	1	0	1	1
↓		0	1	1	0	1	1	0	0
		1	0	1	1	0	0	0	1
Fourth Address		1	1	0	0	0	1	1	0

Note : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{CS_2}$	$\overline{ADSP}$	$\overline{ADSC}$	$\overline{ADV}$	$\overline{WRITE}$	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	X	L	X	X	↑	N/A	Not Selected
L	L	X	L	X	X	X	↑	N/A	Not Selected
L	X	H	L	X	X	X	↑	N/A	Not Selected
L	L	X	X	L	X	X	↑	N/A	Not Selected
L	X	H	X	L	X	X	↑	N/A	Not Selected
L	H	L	L	X	X	X	↑	External Address	Begin Burst Read Cycle
L	H	L	H	L	X	L	↑	External Address	Begin Burst Write Cycle
L	H	L	H	L	X	H	↑	External Address	Begin Burst Read Cycle
X	X	X	H	H	L	H	↑	Next Address	Continue Burst Read Cycle
H	X	X	X	H	L	H	↑	Next Address	Continue Burst Read Cycle
X	X	X	H	H	L	L	↑	Next Address	Continue Burst Write Cycle
H	X	X	X	H	L	L	↑	Next Address	Continue Burst Write Cycle
X	X	X	H	H	H	H	↑	Current Address	Suspend Burst Read Cycle
H	X	X	X	H	H	H	↑	Current Address	Suspend Burst Read Cycle
X	X	X	H	H	H	L	↑	Current Address	Suspend Burst Write Cycle
H	X	X	X	H	H	L	↑	Current Address	Suspend Burst Write Cycle

Notes : 1. X means "Don't Care". 2. The rising edge of clock is symbolized by ↑.
3. $\overline{WRITE}$ = L means Write operation in WRITE TRUTH TABLE.
$\overline{WRITE}$ = H means Read operation in WRITE TRUTH TABLE.
4. Operation finally depends on status of asynchronous input pins(ZZ and $\overline{OE}$).

WRITE TRUTH TABLE

$\overline{GW}$	$\overline{BW}$	$\overline{WEa}$	$\overline{WEb}$	$\overline{WEc}$	$\overline{WEd}$	OPERATION
H	H	X	X	X	X	READ
H	L	H	H	H	H	READ
H	L	L	H	H	H	WRITE BYTE a
H	L	H	L	H	H	WRITE BYTE b
H	L	H	H	L	L	WRITE BYTE c and d
H	L	L	L	L	L	WRITE ALL BYTEs
L	X	X	X	X	X	WRITE ALL BYTEs

Notes : 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

(See Notes 1 and 2):

OPERATION	ZZ	$\overline{OE}$	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. ZZ pin is pulled down internally
3. For write cycles that following read cycles, the output buffers must be disabled with $\overline{OE}$, otherwise data bus contention will occur.
4. Sleep Mode means power down state of which stand-by current does not depend on cycle time.
5. Deselected means power down state of which stand-by current depends on cycle time.

PASS-THROUGH TRUTH TABLE

PREVIOUS CYCLE		PRESENT CYCLE				NEXT CYCLE
OPERATION	$\overline{\text{WRITE}}$	OPERATION	$\overline{\text{CS}}_1$	$\overline{\text{WRITE}}$	$\overline{\text{OE}}$	
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	Initiate Read Cycle Address=An Data=Qn-1 for all bytes	L	H	L	Read Cycle Data=Qn
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=Qn-1 for all bytes	H	H	L	No carryover from previous cycle
Write Cycle, All bytes Address=An-1, Data=Dn-1	All L	No new cycle Data=High-Z	H	H	H	No carryover from previous cycle
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	Initiate Read Cycle Address=An Data=Qn-1 for one byte	L	H	L	Read Cycle Data=Qn
Write Cycle, One byte Address=An-1, Data=Dn-1	One L	No new cycle Data=Qn-1 for one byte	H	H	L	No carryover from previous cycle

Notes : 1. This operation makes written data immediately available at output during a read cycle preceded by a write cycle.s

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V_{DD} Supply Relative to V_{SS}	V_{DD}	-0.3 to 4.6	V
Voltage on V_{DDQ} Supply Relative to V_{SS}	V_{DDQ}	V_{DD}	V
Voltage on Input Pin Relative to V_{SS}	V_{IN}	-0.3 to 6.0	V
Voltage on I/O Pin Relative to V_{SS}	V_{IO}	-0.3 to V_{DDQ}+0.5	V
Power Dissipation	P_D	2.2	W
Storage Temperature	T_{STG}	-65 to 150	°C
Operating Temperature	T_{OPR}	0 to 70	°C
Storage Temperature Range Under Bias	T_{BIAS}	-10 to 85	°C

***Note :** Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C≤ T_A≤70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	3.135	3.3	3.465	V
Ground	V_{SS}	0	0	0	V

OPERATING CONDITIONS at 2.5V I/O(0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	Max	Unit
Supply Voltage	V_{DD}	3.135	3.3	3.465	V
	V_{DDQ}	2.375	2.5	2.9	V
Ground	V_{SS}	0	0	0	V

CAPACITANCE*(T_A=25°C, f=1MHz)

PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN}=0V	-	6	pF
Output Capacitance	C_{OUT}	V_{OUT}=0V	-	8	pF

***Note :** Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V+0.165V/-0.165V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	MAX	UNIT
Input Leakage Current(except ZZ)	I_{IL}	V_{DD} = Max ; V_{IN}=V_{SS} to V_{DD}		-2	+2	µA
Output Leakage Current	I_{OL}	Output Disabled, V_{OUT}=V_{SS} to V_{DDQ}		-2	+2	µA
Operating Current	I_{CC}	Device Selected, I_{OUT}=0mA, ZZ≤V_{IL}, All Inputs=V_{IL} or V_{IH} , Cycle Time ≥cyc Min	-40	-	570	mA
			-44	-	520	
			-50	-	480	
			-55	-	450	
			-57	-	430	
Standby Current	I_{SB}	Device deselected, I_{OUT}=0mA,ZZ≤V_{IL}, f=Max, All Inputs≤0.2V or ≥ V_{DD}-0.2V	-40	-	160	mA
			-44	-	150	
			-50	-	140	
			-55	-	130	
			-57	-	130	
	I_{SB1}	Device deselected, I_{OUT}=0mA, ZZ≤0.2V, f = 0, All Inputs=fixed (V_{DD}-0.2V or 0.2V)		-	30	mA
	I_{SB2}	Device deselected, I_{OUT}=0mA, ZZ≥V_{DD}-0.2V, f=Max, All Inputs≤V_{IL} or ≥V_{IH}		-	30	mA
Output Low Voltage(3.3V I/O)	V_{OL}	I_{OL} = 8.0mA		-	0.4	V
Output High Voltage(3.3V I/O)	V_{OH}	I_{OH} = -4.0mA		2.4	-	V
Output Low Voltage(2.5V I/O)	V_{OL}	I_{OL} = 1.0mA		-	0.4	V
Output High Voltage(2.5V I/O)	V_{OH}	I_{OH} = -1.0mA		2.0	-	V
Input Low Voltage(3.3V I/O)	V_{IL}			-0.5*	0.8	V
Input High Voltage(3.3V I/O)	V_{IH}			2.0	V_{DD}+0.5**	V
Input Low Voltage(2.5V I/O)	V_{IL}			-0.3*	0.7	V
Input High Voltage(2.5V I/O)	V_{IH}			1.7	V_{DD}+0.5**	V

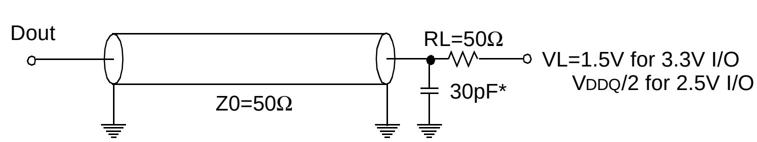
* V_{IL}(Min)=-2.0(Pulse Width ≤ t_{CYC}/2)
** V_{IH}(Max)=4.6(Pulse Width ≤ t_{CYC}/2)
** In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.5V

TEST CONDITIONS

(V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=3.3V+0.165/-0.165V or V_{DD}=3.3V+0.165V/-0.165V,V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0 to 70°C)

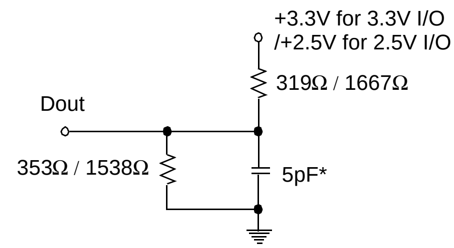
PARAMETER	VALUE
Input Pulse Level(for 3.3V I/O)	0 to 3V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 0.3V and 2.7V for 3.3V I/O)	1ns
Input Rise and Fall Time(Measured at 0.3V and 2.1V for 2.5V I/O)	1ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V_{DDQ}/2
Output Load	See Fig. 1

Output Load(A)



* Capacitive Load consists of all components of the test environment.

Output Load(B)
(for t_{LZC}, t_{LZOE}, t_{HZOE} & t_{HZC})



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS(T_A=0 to 70°C, V_{DD}=3.3V+0.165V/-0.165V)

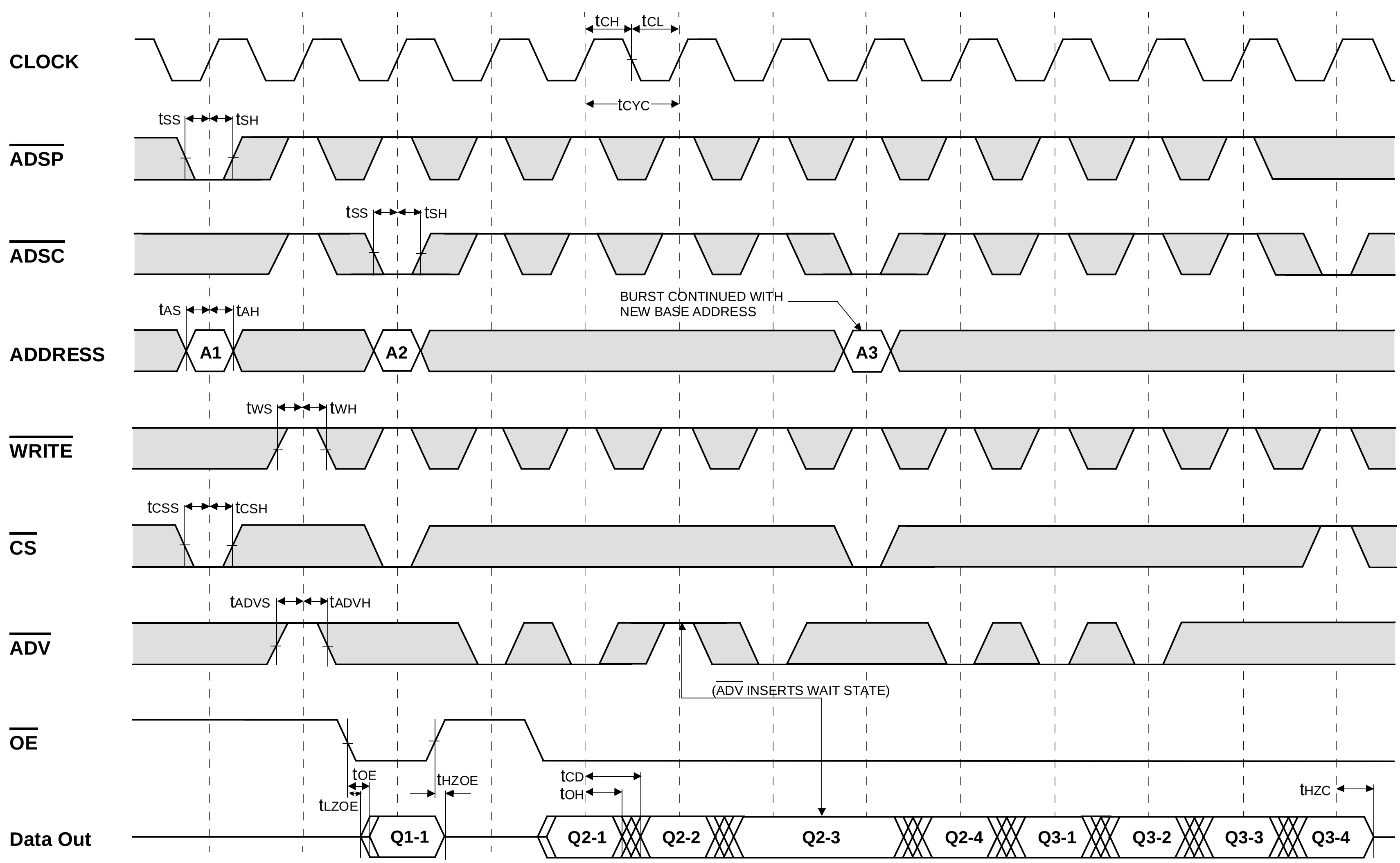
PARAMETER	SYMBOL	-40		-44		-50		-55		-57		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CYC}	4.0	-	4.4	-	5.0	-	5.4	-	5.7	-	ns
Clock Access Time	t_{CD}	-	2.5	-	2.8	-	3.1	-	3.1	-	3.3	ns
Output Enable to Data Valid	t_{OE}	-	2.8	-	2.8	-	3.1	-	3.1	-	3.3	ns
Clock High to Output Low-Z	t_{LZC}	0	-	0	-	0	-	0	-	0	-	ns
Output Hold from Clock High	t_{OH}	1.0	-	1.0	-	1.0	-	1.0	-	1.3	-	ns
Output Enable Low to Output Low-Z	t_{LZOE}	0	-	0	-	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t_{HZOE}	-	2.8	-	2.8	-	3.0	-	3.0	-	3.0	ns
Clock High to Output High-Z	t_{HZC}	1.0	2.5	1.0	2.8	1.0	3.0	1.0	3.0	1.3	3.0	ns
Clock High Pulse Width	t_{CH}	1.7	-	2.0	-	2.0	-	2.0	-	2.0	-	ns
Clock Low Pulse Width	t_{CL}	1.7	-	2.0	-	2.0	-	2.0	-	2.0	-	ns
Address Setup to Clock High	t_{AS}	0.8	-	1.2	-	1.4	-	1.4	-	1.5	-	ns
Address Status Setup to Clock High	t_{SS}	0.8	-	1.2	-	1.4	-	1.4	-	1.5	-	ns
Data Setup to Clock High	t_{DS}	0.8	-	1.2	-	1.4	-	1.4	-	1.5	-	ns
Write Setup to Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t_{WS}	0.8	-	1.2	-	1.4	-	1.4	-	1.5	-	ns
Address Advance Setup to Clock High	t_{ADVS}	0.8	-	1.2	-	1.4	-	1.4	-	1.5	-	ns
Chip Select Setup to Clock High	t_{CSS}	0.8	-	1.2	-	1.4	-	1.4	-	1.5	-	ns
Address Hold from Clock High	t_{AH}	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	ns
Address Status Hold from Clock High	t_{SH}	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t_{DH}	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High ($\overline{GW}$, $\overline{BW}$, $\overline{WE}$x)	t_{WH}	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t_{ADVH}	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t_{CSH}	0.3	-	0.4	-	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t_{PDS}	2	-	2	-	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t_{PUS}	2	-	2	-	2	-	2	-	2	-	cycle

Notes : 1. All address inputs must meet the specified setup and hold times for all rising clock edges whenever $\overline{ADSC}$ and/or $\overline{ADSP}$ is sampled low and $\overline{CS}$ is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.

2. Both chip selects must be active whenever $\overline{ADSC}$ or $\overline{ADSP}$ is sampled low in order for the this device to remain enabled.

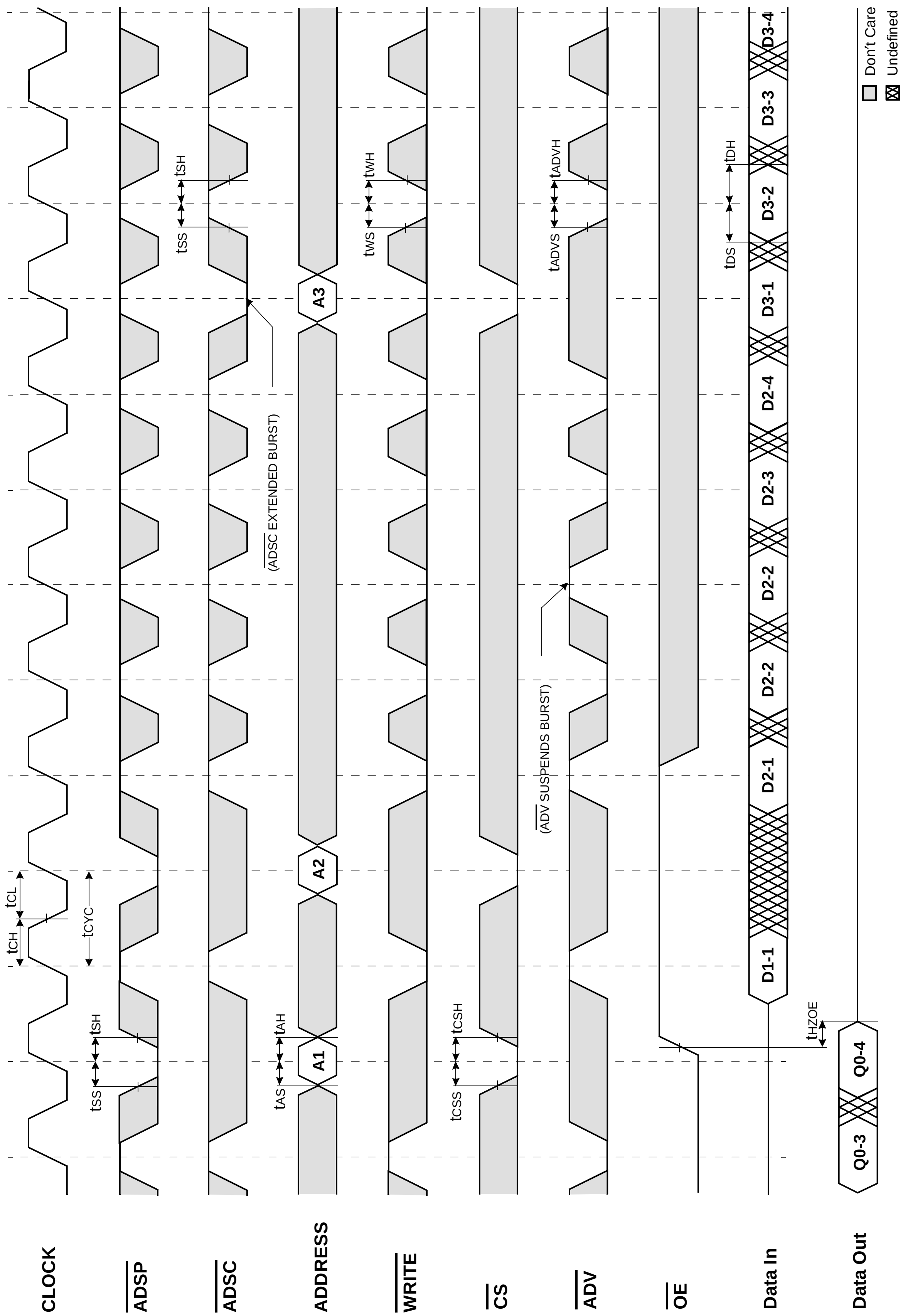
3. $\overline{ADSC}$ or $\overline{ADSP}$ must not be asserted for at least 2 Clock after leaving ZZ state.

TIMING WAVEFORM OF READ CYCLE



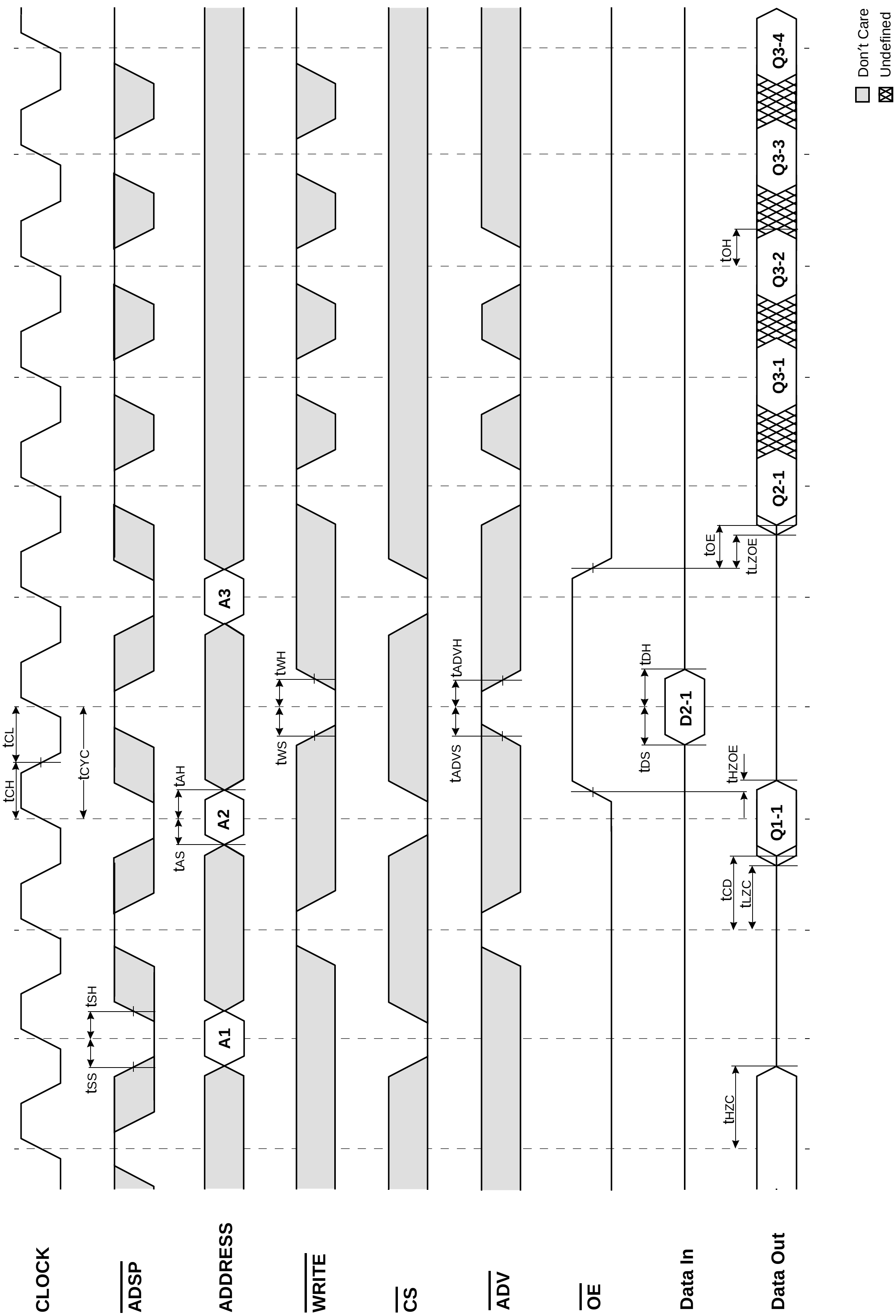
NOTES : $\overline{WRITE}$ = L means $\overline{GW}$ = L, or $\overline{GW}$ = H, $\overline{BW}$ = L, $\overline{WE_x}$ = L
$\overline{CS}$ = L means $\overline{CS_1}$ = L, CS_2 = H and $\overline{CS_2}$ = L
$\overline{CS}$ = H means $\overline{CS_1}$ = H, or $\overline{CS_1}$ = L and $\overline{CS_2}$ = H, or $\overline{CS_1}$ = L, and CS_2 = L

TIMING WAVEFORM OF WRTE CYCLE



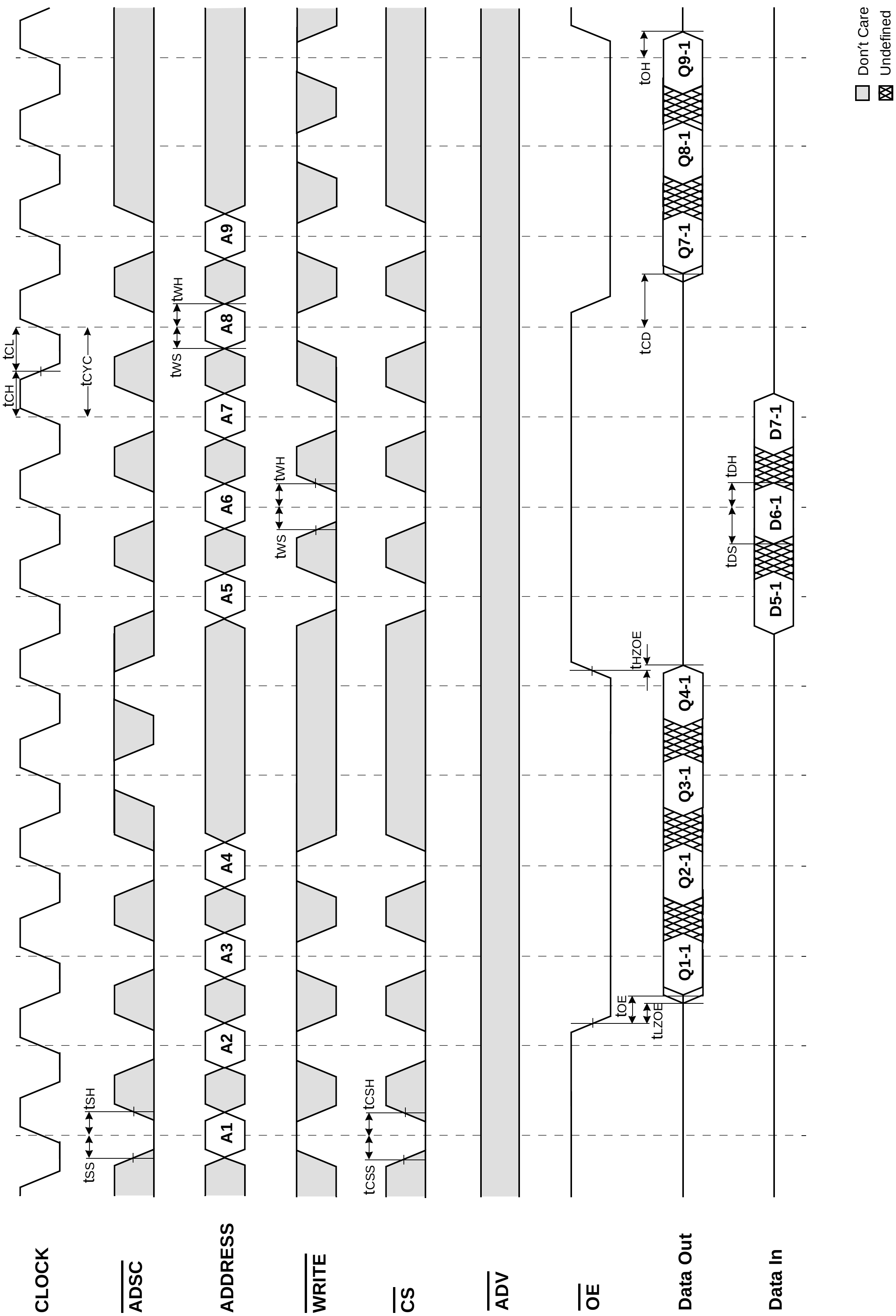
SAMSUNG ELECTRONICS

TIMING WAVEFORM OF COMBINATION READ/WRTE CYCLE(ADSP CONTROLLED , ADSC=HIGH)

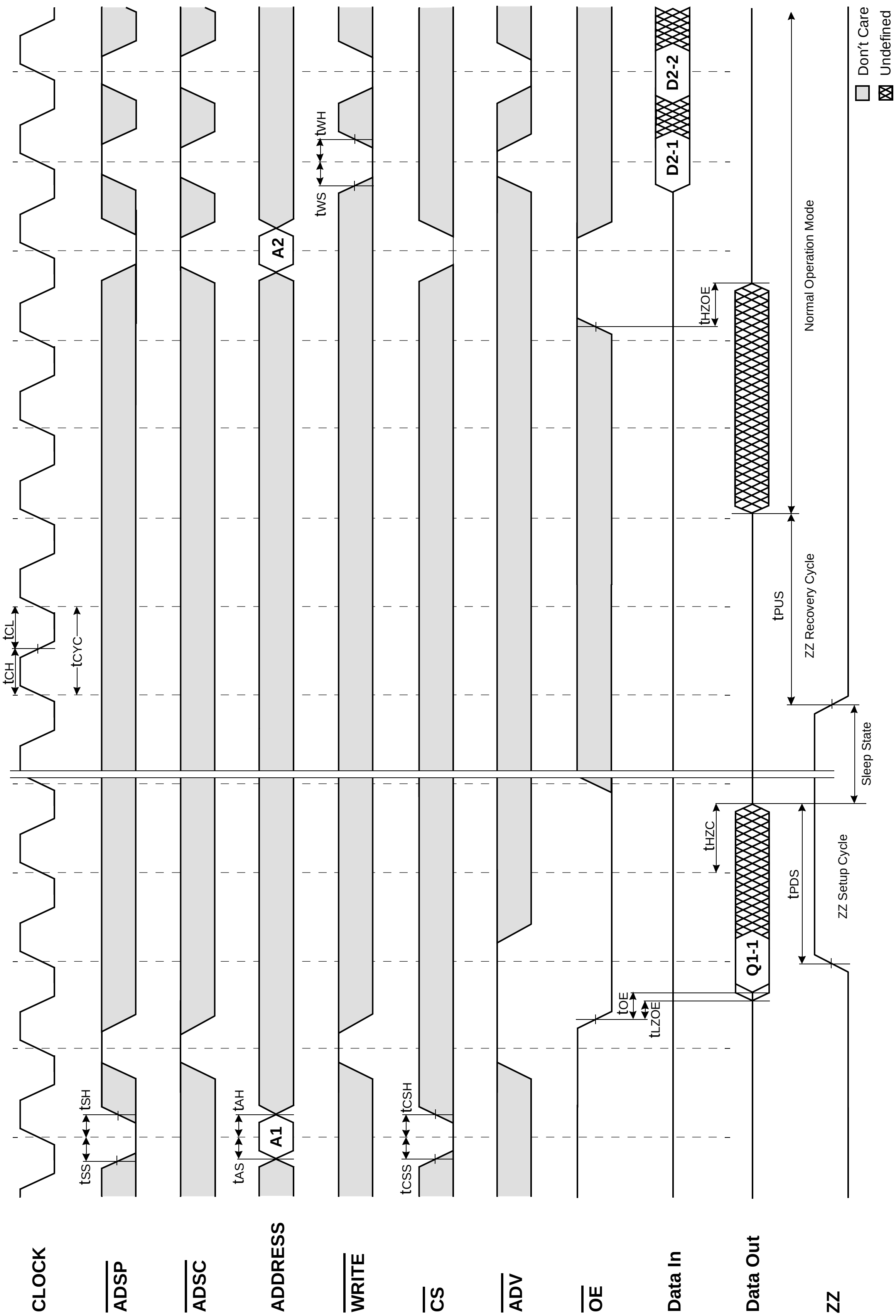


SAMSUNG ELECTRONICS

TIMING WAVEFORM OF SINGLE READ/WRITE CYCLE(ADSC CONTROLLED , ADSP=HIGH)



TIMING WAVEFORM OF POWER DOWN CYCLE

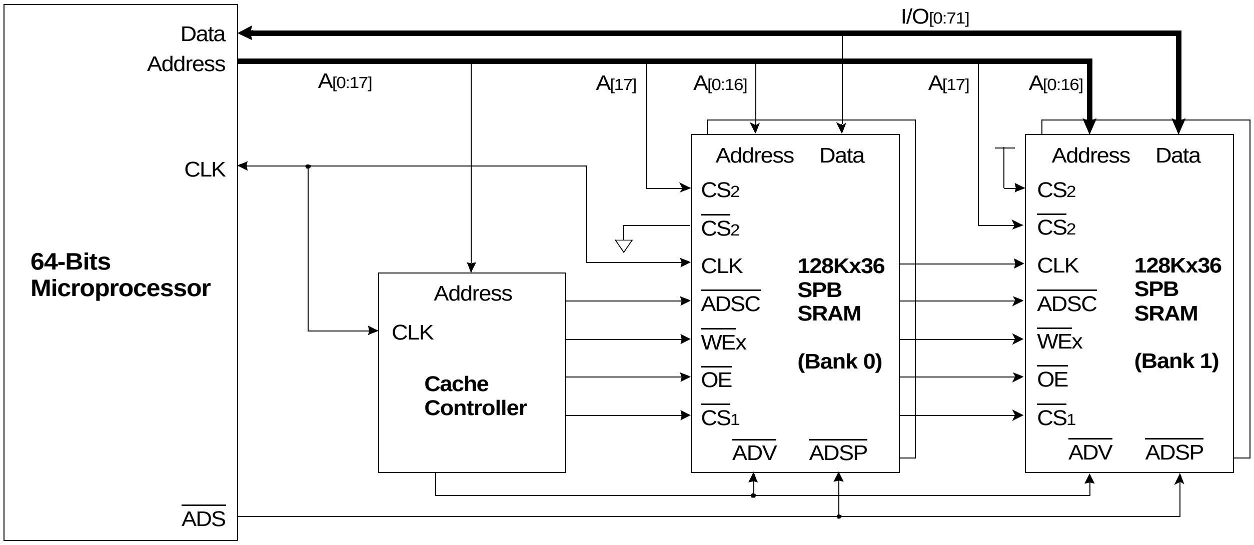


SAMSUNG ELECTRONICS

APPLICATION INFORMATION

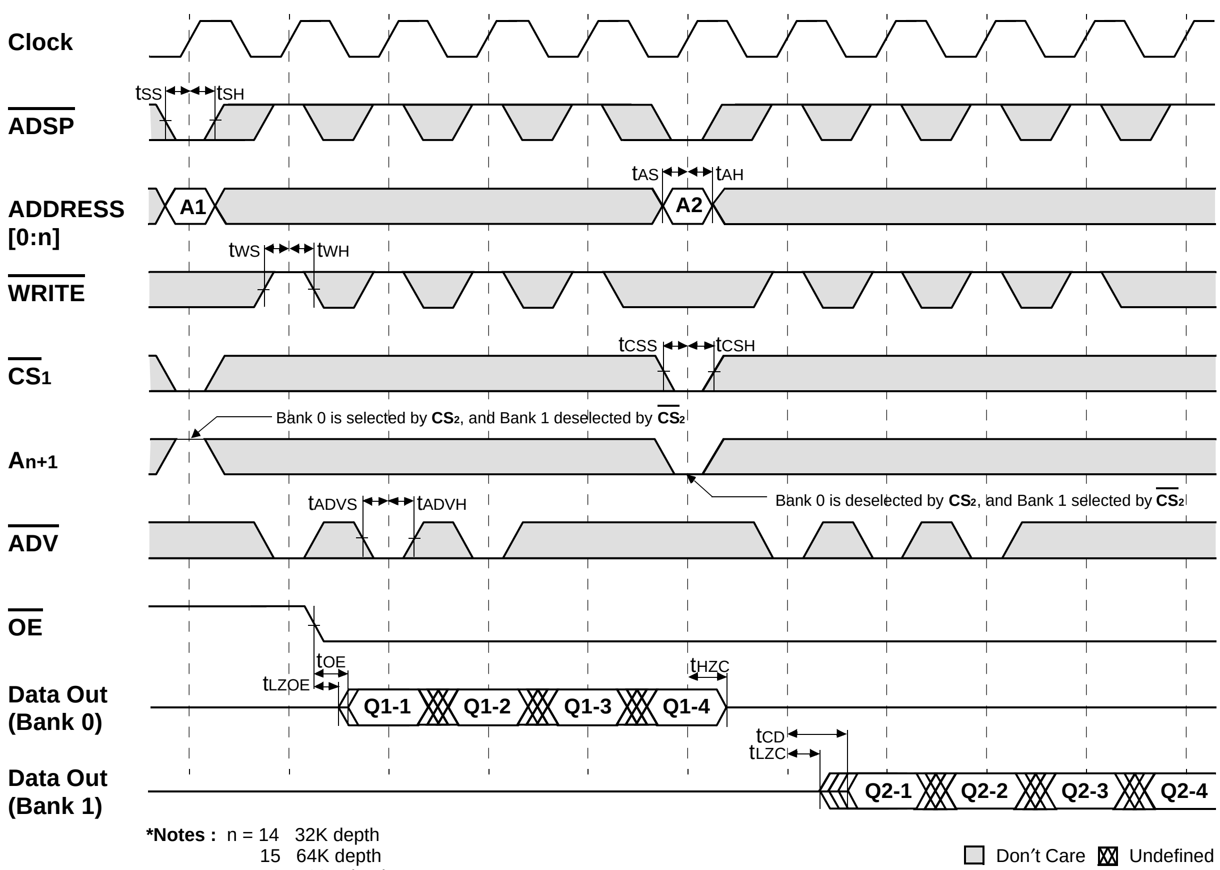
DEPTH EXPANSION

The Samsung 128Kx36 Synchronous Pipelined Burst SRAM has two additional chip selects for simple depth expansion. This permits easy secondary cache upgrades from 128K depth to 256K depth without extra logic.



INTERLEAVE READ TIMING (Refer to non-interleave write timing for interleave write timing)

(ADSP CONTROLLED , ADSC=HIGH)



***Notes :** n = 14 32K depth
15 64K depth
16 128K depth
17 256K depth

PACKAGE DIMENSIONS

100-TQFP-1420A

Units ; millimeters/Inches