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PT2201

Current Mode PWM Controller

GENERAL DESCRIPTION

PT2201 is a highly integrated current mode PWM controller, with the features of extreme low start up current, low operating current plus green mode operation and built-in protection functions allows the design of SMPS become easier to meet the high performance, high reliability and low standby power requirements.

The start-up current is very small typically 3uA so that a large start up resistor can be used in the start-up circuit to minimize standby power. Under the light load or no load conditions the PT2201 automatically decreases PWM frequency and enters burst mode operation thus the power loss on power MOSFET is reduced. With a programmable oscillator the PWM frequency is easily set via an external resistor.

Synchronized slope compensation has been implemented in the PT2201 to avoid potential sub harmonic oscillation caused by peak current control mode when operating under Continuous Conduct Mode. Moreover, the internal LEB on the current sense input removes the signal glitch due to snubber circuit diode reverse recovery and greatly reduces the external component count and system cost in the design.

The PT2201 also features multi-level protections to enhance SMPS reliability including cycle by cycle Over Current Protection, Over Load Protection, programmable Over Temperature Protection, Over Voltage Protection on VDD and VDD Under Voltage Lock-out. The gate drive output is clamped at 18V to protect the power MOSFET. The burst mode frequency is limited above 20 KHz thus the potential audible noise is avoid while the system is under light or no load conditions.

The PT2201 is available in SOP8 and DIP8 packages.

FEATURES

- Frequency Jittering For Better EMI Performance
- Frequency automatically decrease to minimize standby power
- Noise Free Operation
- Programmable PWM Frequency
- Current Mode Operation, Built-in Slope Compensation
- Low Start-up Current
- Constant Power Limit For Universal AC Input
- Leading Edge Blanking on Current Sense
- Gate Output 18V Clamp
- Protection Functions：
  - Auto Recovery Programmable Over Temperature Protection（OTP）
  - Auto Recovery Over Voltage Protection on VDD (OVP) and UVLO
  - Line Compensated Cycle By Cycle Current Limit (OCP)
  - Locked Over Load Protection (OLP)

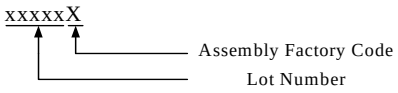
APPLICATIONS

- Open-frame SMPS
- Fly-back Switching Power Supplier
- Power Adaptor
- Battery Charger

ORDERING INFORMATION

PACKAGE	TEMPERATURE RANGE	ORDERING PART NUMBER	TRANSPORT MEDIA	MARKING
SOP-8	-40℃ to 85℃	PT2201BSOH	Tape and Reel	PT2201 xxxxxX
DIP-8	-40℃ to 85℃	PT2201BDIH	Tube	PT2201 xxxxxX

Note:



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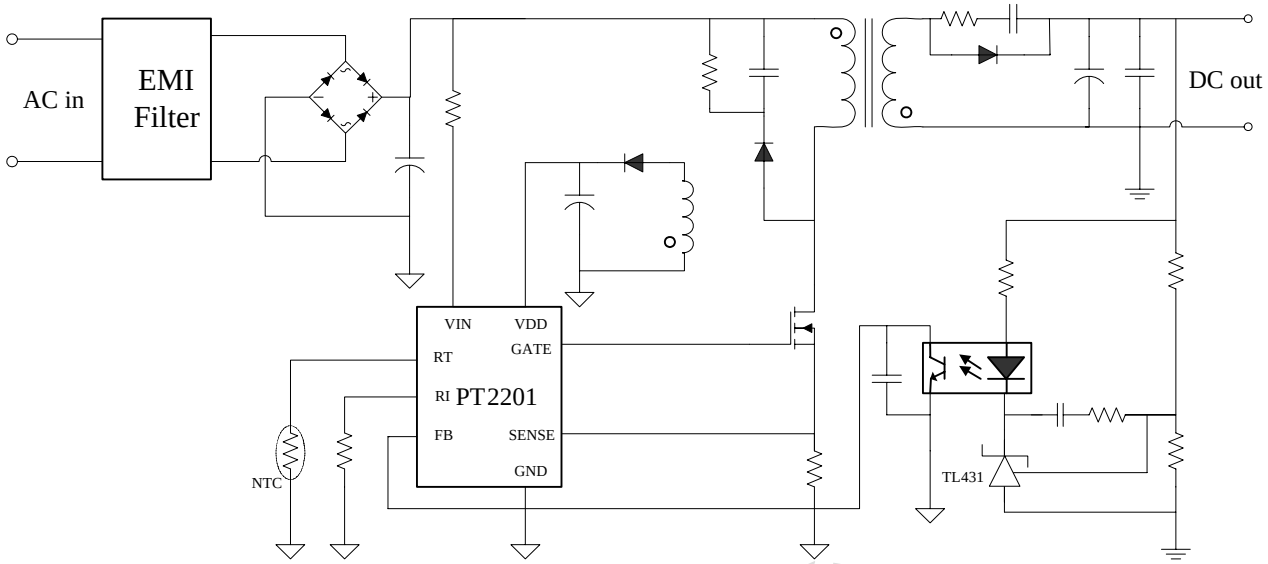
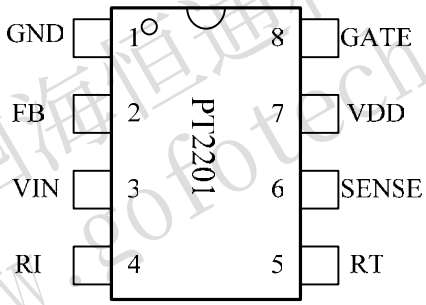
TYPICAL APPLICATION CIRCUIT



PIN ASSIGNMENT



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PIN DESCRIPTIONS

PIN No.	PIN NAMES	DESCRIPTION
1	GND	Ground
2	FB	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and SENSE pin voltage level.
3	VIN	Rectified line input for startup and line voltage sensing
4	RI	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	Temperature sensing input pin, connecting to an NTC resistor
6	SENSE	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	DC power supply pin.
8	GATE	Totem-pole gate drive output for power MOSFET.

ABSOLUTE MAXIMUM RATINGS (note1)

SYM	PARAMETER	VALUE	UNIT
VIN/VDD	VIN/VDD DC Supply Voltage	30	V
VDD_{CLAMP}	VDDClamp Voltage	33	V
IDD_{CLAMP}	VDD Clamp Continuous Cuurrent	10	mA
V_{FB}	FB Input Voltage	-0.3-7	V
V_{SENSE}	SENSE Input Voltage	-0.3-7	V
V_{RT}	RT Input Volatage	-0.3-7	V
V_{RI}	RI Input Voltage	-0.3-7	V
Topt	Min/Max Operating Junction Temp.	-40 to 150	℃
Tstg	Min/Max Storage Temp.	-55 to 150	℃
HBM	ESD Capability, HBM	2000(note2)	V
RΘJA	SOP-8 DIP-8	150 90	℃/W

RECOMMENDED OPERATING RANGE

SYM	PARAMETER	VAULE	UNIT
VDD	V_{DD} Supply Voltage	10～30	V
RI	RI Resistor Value	100	Kohm
TA	Operating Ambient Temperature	-20～85	℃

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Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Recommended Operating Range indicates conditions for which the device is functional, but do not guarantee specific performance limits. Electrical Characteristics state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Range. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 2: Human body model, 100pF discharged through a 1.5kΩ resistor.

ELECTRICAL CHARACTERISTICS

(T_{OPT}=25℃, VDD=16V，unless specified otherwise)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VDD)						
V_{DD_ON}	V_{DD} Start-up voltage	V_{DD} rising	14.0	15.0	16.0	V
V_{DD_MIN}	V_{DD} minimum operating level	V_{DD} falling	6.5	7.5	8.5	V
V_{DD_OVP}	V_{DD} Over Voltage Protection Level	V_{DD} rising	24.5	26	27.5	V
$V_{DD\_OVP\_OFF}$	V_{DD} Over Voltage Protection Release Level	V_{DD} falling	22.5	24	25.5	V
V_{OVP_HYS}	V_{DD} Over Voltage Hysteresis	V_{DD_OVP}-$V_{DD\_OVP\_OFF}$		2		V
V_{ZENER}	V_{DD} Pin Zener Diode Clamp Voltage	I(V_{DD})=5mA		33		V
Current Into VDD						
I_{VDD_START}	V_{DD} Start-up Current	V_{DD}=15V Measuring Current into V_{DD}		3	20	uA
I_{VDD_OPER}	V_{DD} Operating Current	V_{DD}=16V, RI=100Kohm V_{FB}=3V, Gate Floating		1		mA
FEED BACK PIN (FB)						
V_{OFB}	V_{FB} Open Loop Voltage	V_{DD}=16V,		6.0		V
V_{PL}	FB Over Load Protection level			4.4		V
V_{GM}	Green Mode FB Threshold			1.7		V
V_{BM}	Burst Mode Entering Threshold			0.9		V
V_{ZD}	Zero Duty Cycle FB Threshold	V_{DD}=16V, RI=100Kohm			0.75	V
T_{PL_DELAY}	Over Load Protection Delay Time	RI=100Kohm		80		ms
Z_{FB}	FB Pin Input Impendence			9.0		Kohm
I_{FB}	FB Pin Supply Current	FB Short To GND, Measuring Current Flowing From FB Pin		0.6		mA
OSCILLATOR (OSC)						
F_{osc}	Oscillator Frequency	RI=100Kohm	60	65	70	kHz
$\triangle F_{JIT}$	△Fosc/Fosc	RI=100Kohm	-3		3	%
$T_{JITTRING}$	Frequency Modulation Period	RI=100Kohm		32		mS
F_{MIN}	Minimum PWM Frequency	V_{DD}=16V, RI=100Kohm		22		kHz
RI	Acceptable RI Range		50	100	250	Kohm

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ELECTRICAL CHARACTERISTICS (CONTINUE)

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
F_{DT}	Oscillator Frequency Stability At Different Temperature	V_{DD}=16V, RI=100Kohm -20°C 到 100°C		2		%
F_{DV}	Oscillator Frequency Stability At Different VDD Input Level	V_{DD}=12~25V, RI=100Kohm		2		%
PWM SECTION						
A_V	PWM Input GAIN	$\triangle V_{FB}/\triangle V_{CS}$		3.0		V/V
T_{BLK}	Leading Edge Blanking Time			300		ns
D_{MAX}	PWM Maximum Duty Cycle			80		%
D_{MIN}	PWM Minimum Duty Cycle				0	%
OVER TEMP PROTECTION (RT)						
I_{RT}	RT Pin Supply Current	VDD=16V，RI=100Kohm		70		uA
V_{OTP}	RT Pin Over Temp Protection Threshold	VDD=16V，RI=100Kohm	1.015	1.065	1.115	V
V_{OTP_HYS}	RT Pin Over Temp Protection Hysteresis			100		mV
V_{RT_Open}	RT Pin Floating Voltage	VDD=16V，RI=100Kohm		6		V
CURRENT SENSE INPUT (SENSE)						
Z_{CS}	SENSE Input Impendence			30		Kohm
V_{TH_OC}	OCP Threshold at Ivin=0	FB=4V, I(VIN)=0	0.85	0.90	0.95	V
$\triangle V_{OC}/\triangle I_{VIN}$	OCP I_{VIN} Compensation Coefficient			-0.87		mV/uA
$V_{TH\_OC\_1}$	OCP Threshold With Compensation	FB=4V, I(VIN)=150uA		0.77		V
T_{OC_DELAY}	Delay Time From OCP to Gate Output OFF	V_{DD}=16V, CS>V_{TH}_OC，C_{GATE}=1000pF		100		nS
GATE OUTPUT						
V_{OL}	GATE Output Low Level	V_{DD}=16V, Io=-20mA			0.3	V
V_{OH}	GATE Output High Level	V_{DD}=16V, Io=20mA	11			V
T_r	GATE Output Rising time	V_{DD}=16V, CL=1000pF		120		nS
T_f	GATE Output Falling Time	V_{DD}=16V, CL=1000pF		50		nS
V_{GMAX}	GATE Output Clamp Voltage			18		V

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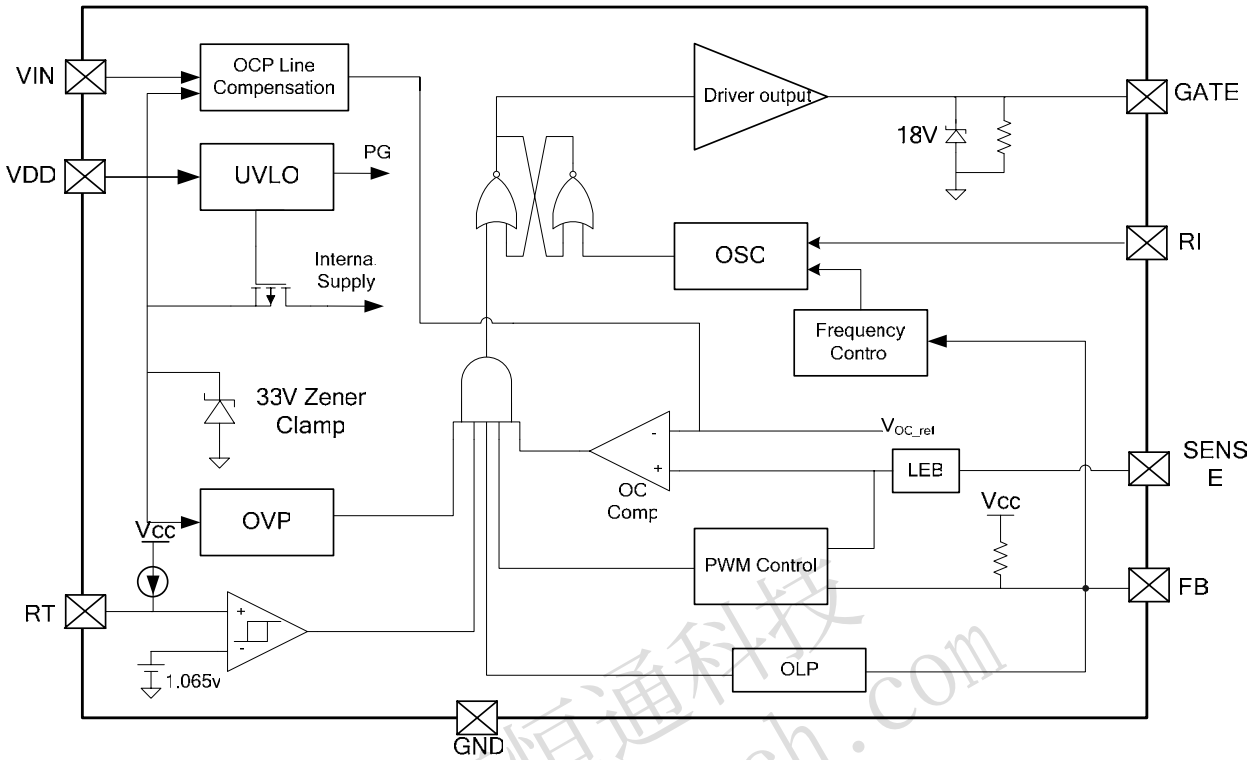
SIMPLIFIED BLOCK DIAGRAM



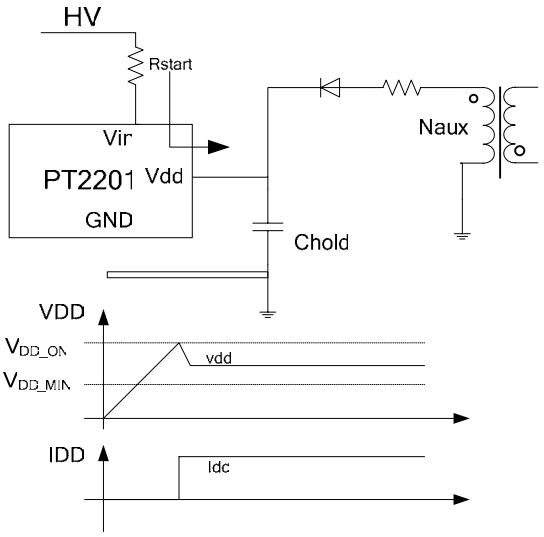
OPERATION DESCRIPTION

With enhanced functions and extremely low start up current and low operating current together with optimized controlling mode, the PT2201 is easy to meet the high performance as well as low standby power requirement in the SMPS application. Its detail features are described as below:

STARTUP AND UVLO:

The start up of PT2201 is realized through the current provided by a resistor connecting to HV line charges the capacitor connecting to VDD pin to the start up threshold voltage. As shown below, as long as the voltage on Chold is below the start up threshold the PT2201 stays in UVLO status. The current supplied by Rstart charges the Chold through VDD pin thus the voltage on VDD increases. The PT2201 starts to operate when the voltage level on VDD reaches V_{DD_ON} start up threshold. After startup the PT2201 begins to deliver drive signal on GATE and the operating current is supplied by the auxiliary winding of the transformer.

Since the PT2201 sinks a few macro amperes of current before start up, a large start up resistor could be used in the start up circuit to minimize standby power. As for the applications with general AC input range a 2Mohm 1/8W resistor and a 10uF/50V capacitor compose a simple and reliable start up circuit.



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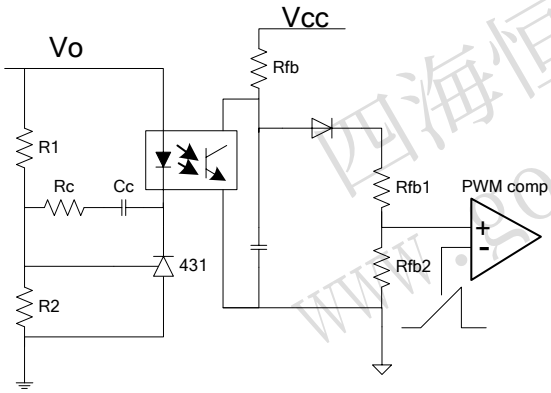
OPERATING CURRENT：

The PT2201 is fabricated with BiCMOS process, the operating current has been reduced to less 1mA when GATE is floating, thus the system efficiency is improved and at the same time, a smaller hold up capacitor can be used to speed up start up progress.

FEEDBACK AND PWM：

The PT2201 adopts current mode control scheme. the voltage feedback loop is closed by the TL431 and an opto-coupler connected between output node and FB pin, as shown below: A 2.5V reference voltage has been implemented in the TL431, if the divided voltage of R1 and R2 is less than 2.5V TL431will sink current from Vo and the current is transferred to the FB pin by the opto-coupler. The transferred current is loaded by a resistor connected to the internal regulator output so FB pin voltage is determined and thus PWM signal is generated.



ENERGY SAVE OPERATION AT LIGHT LOAD:

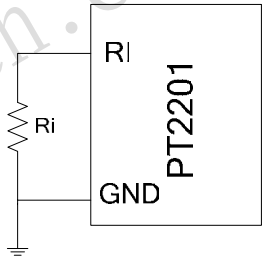
Generally he SMPS switching loss is proportional to switching frequency of power MOSFET. In order to achieve high conversion efficiency when the load decrease the PT2201 automatically debase PWM frequency to reduce switching loss. The reduction of the load current results in the decrease of voltage on FB pin, when the voltage on FB pin is lower than 1.7V the PWM frequency will linearly decrease with V_{FB} until touch bottom which is 1/3 normal operating frequency. If the FB pin voltage drops below the preset level the PT2201 enters burst mode operation, some PWM cycles is skipped to minimize switching loss. Moreover if the FB pin voltage falls below Zero-Duty level which is set to be 0.75V the PWM is disabled immediately until it recovers to above Zero-Duty threshold.

OSCILLATOR AND FREQUENCY JITTERING：

The operating frequency can be easily set via a resistor connected to the RI pin and GND. The relationship between operating frequency and RI follows the expression: Fosc=6500/RI. Which Fosc represents normal operating frequency with unit in KHz, and RI with unit in Kohm.

The frequency jittering is implemented in the PT2201. The oscillation frequency is modulated so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore reduces system design challenge.

Care should be considered that the PWM frequency will be reduced to one third of normal operating frequency so a large RI is not recommended because the audible noise maybe exists when the load is too light.



CURRENT SENSE AND LEB:

One function of the SENSE pin is sensing the current of the power MOSFET to generate a current slope and the other function is providing cycle by cycle current limit. PT2201 senses power MOSFET's current through a resistor connected between source terminal of the power MOSFET and GND. The voltage on SENSE and FB determines duty cycle of the PWM signal.

As for cycle by cycle current limit, at each PWM cycle when the voltage of SENSE input excess the internal threshold the PWM signal is terminated after a short delay to protect the power MOSFET. The relationship between the OCP threshold and the current of power MOSFET follows below expression: I_{OC}=Voc/Rcs; Ioc is the current of power MOSFET, Voc is the threshold of OCP and Rcs represents sensing resistor. The internal OCP threshold is modulated by the current into VIN pin,

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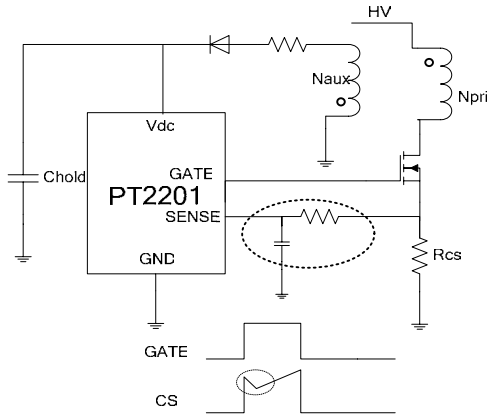
with zero current flowing into VIN the threshold is 0.9V. A spike is inevitable on the sensed signal on Rcs at the instance when the power MOSFET is turned on due to the recovery time of the secondary rectifier and the snubber circuit. The LEB has been implemented in PT2201, during the LEB time the OCP comparator is disabled so the PWM signal can not be terminated by the turn-on spike on the sensed signal so the external RC filter can be removed.

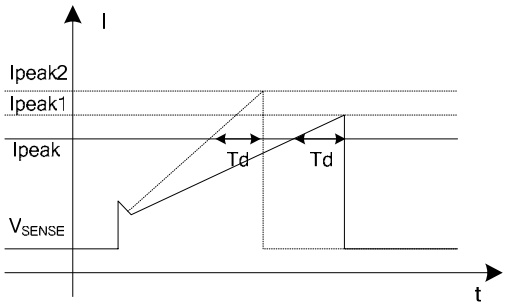


INTERNAL SLOPE COMPENSATION:

To eliminate the potential sub-harmonic oscillation problem when the duty cycle excess 0.5, the slope compensation has been implemented in the PT2201. At each PWM duty cycle a constant slope is added to the sensed current ramp so that the system stability is improved.

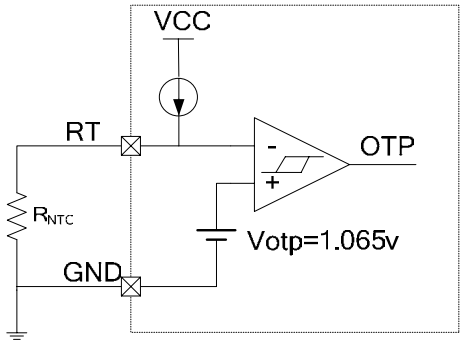
UNIVERSAL INPUT OCP COMPENSATION:

Because there is always a constant delay time Td from OCP is triggered to the power MOSFET is turned off, the actual current of the MOSFET at the instance it is turned off is different from the setting value. Taking the below figure as reference, considering the delay time of Td the actual current is: Ipeak1=Ipeak+Islope1*Td. Islope1=Vindc/Lpri. With a higher input level the actual OCP current is Ipeak2=Ipeak+Islope2*Td, Islope2=Vindc2/Lpri. Which Lpri represents primary winding inductance of transformer, Td is a constant delay time and does not vary with Vin. From above equations it can be derived that the actual OCP threshold of the power MOSFET is always larger than setting value due to the OCP delay time and the difference increases with the increase of Vin. In order to compensate the difference at different input level the OCP threshold in PT2201 has been designed to vary with the current into VIN pin, it means that a larger Ivin results in a lower OCP threshold thus the actual OCP threshold of power MOSFET maintains unchanged in the universal input range.



OVER TEMPERATURE PROTECTION:

The ambient temperature sense and protection is realized via a NTC resistor connected between the RT pin and GND. The PT2201 provides a temperature free constant current via the RT pin. When the ambient temperature rise the NTC resistor value gets small thus the voltage on RT pin decreases, when the voltage on the RT pin drops below the internal threshold the OTP protection is trigged and PT2201 stops delivering PWM signal to MOSFET. The current flowing out of the RT pin is determined by the following equation: I_{RT}=6.5×1.065/Ri. With the Ri=100Kohm the I_{RT}=70uA.



VDD OVER VOLTAGE PROTECTION:

When open loop occurs the opto-coupler does not sink current thus the voltage on FB rise and current limit will be triggered. If the load is not large enough the output voltage will increase because of redundant power is delivered to the load. Under this condition if the OLP is not triggered the output voltage will lost control so that the load is in danger of damaged of over voltage. Because the voltage on auxiliary winding is proportional to the output voltage the VDD rises with the output.

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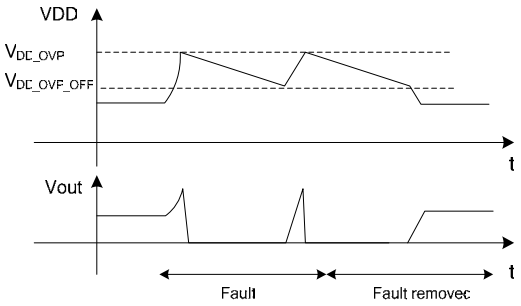
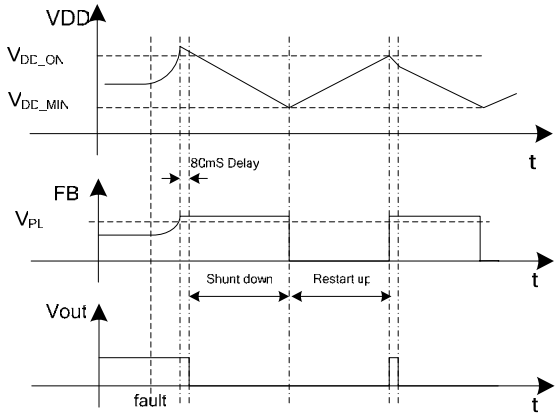
When the voltage on VDD reaches the OVP threshold the PT2201 stops delivering PWM signal to the power MOSFET, voltage on VDD begins to drop due to the internal power consumption, the PT2201 will recover from OVP state when voltage on VDD drops below the OVP release threshold. The OVP cycle will repeat after recovery until if the fault condition is removed.



OVER LOAD PROTECTION:

The Over Load Protection function (OLP) provides another protection to the system from damage when load short circuit or over load occurs. In that condition the voltage on the FB rise, when the V_{FB} excesses 4.4V the PT2201 starts a timer, after a delay time T_{PL_DELAY} if the fault condition still exists the PWM signal is blocked. VDD will then drops due to internal power consumption. When VDD drops below the V_{DD_MIN} threshold, the PT2201 will be totally shut down. When this happens, the start up sequence will kick in and VDD is charging up again.



GATE OUTPUT:

The output drives the GATE of the power MOSFET. The optimized totem-pole type driver offers a good tradeoff between driving ability and EMI. Additionally the output high level is clamped to 18V by an internal clamp so that power MOSFET transistor can be protected against undesirable gate over voltage. A resistor between GATE and GND initials the gate voltage to zero at the off state.

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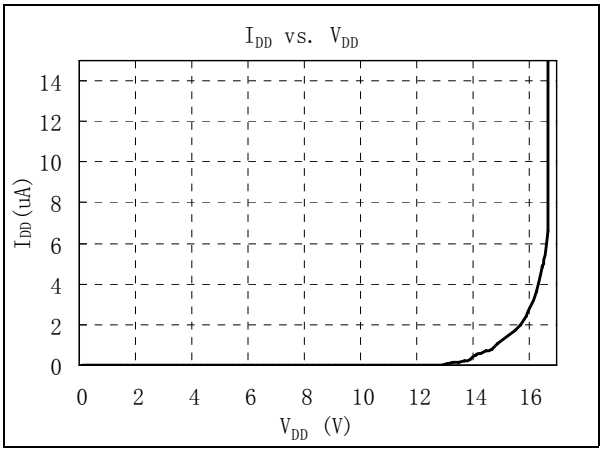
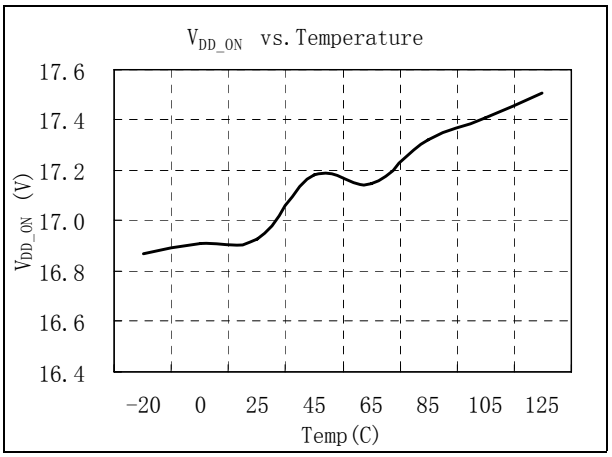
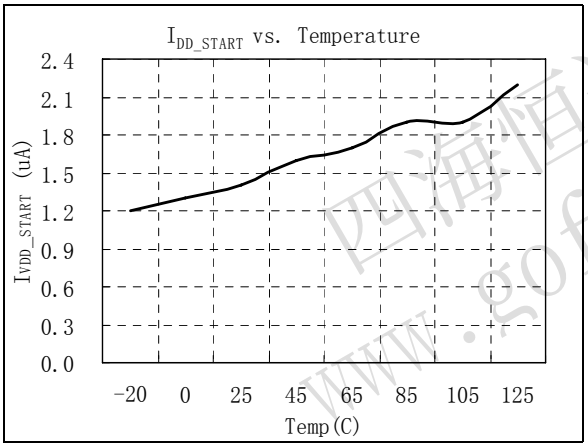
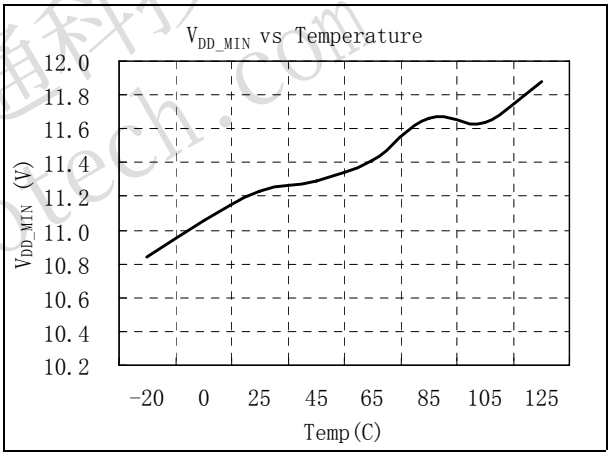
TYPICAL PERFORMANCE CHARACTERISTICS

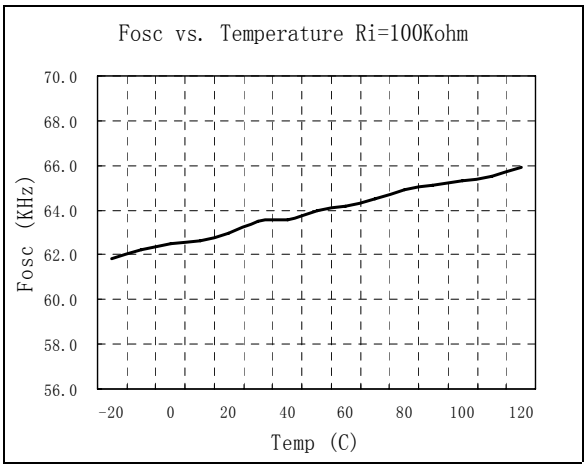
V_{DD}=16V, RI=100Kohm, T_A=25℃ if not otherwise noted

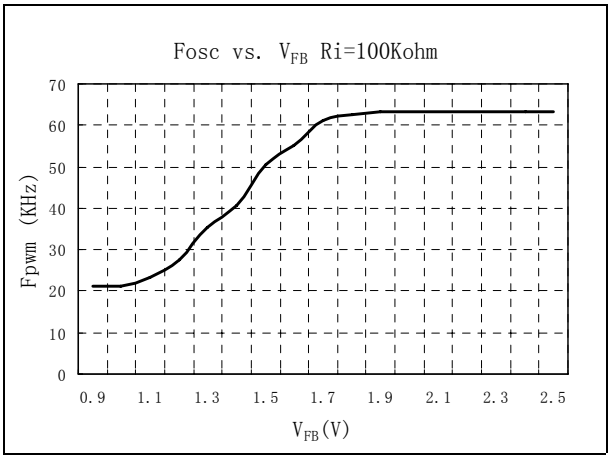












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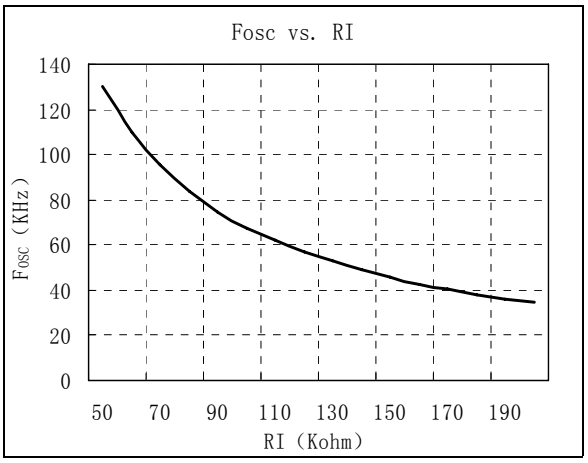

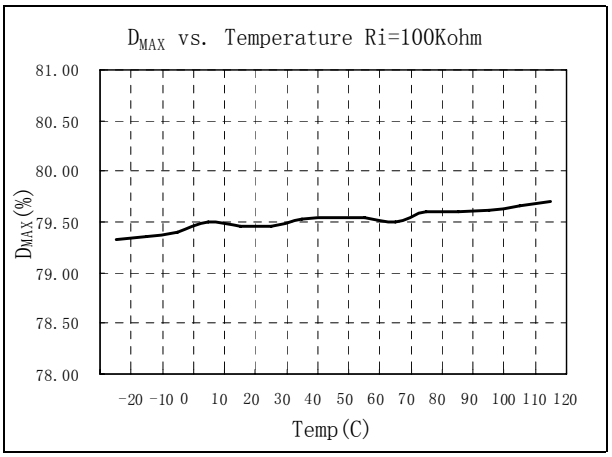

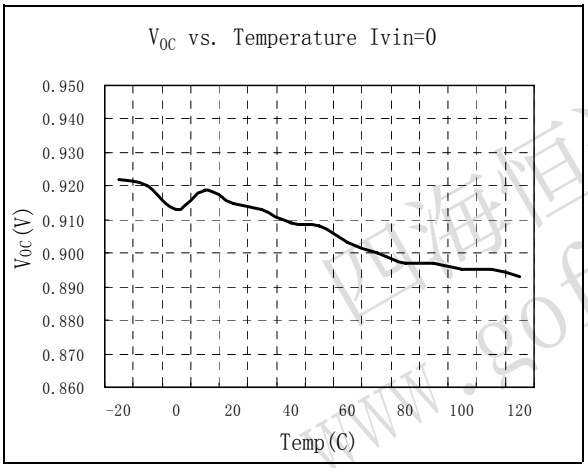

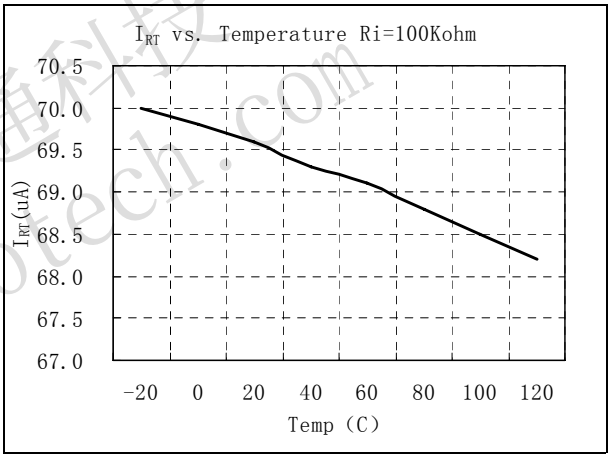

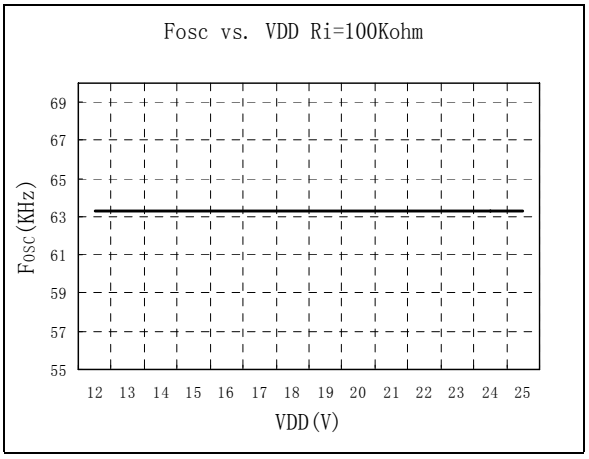

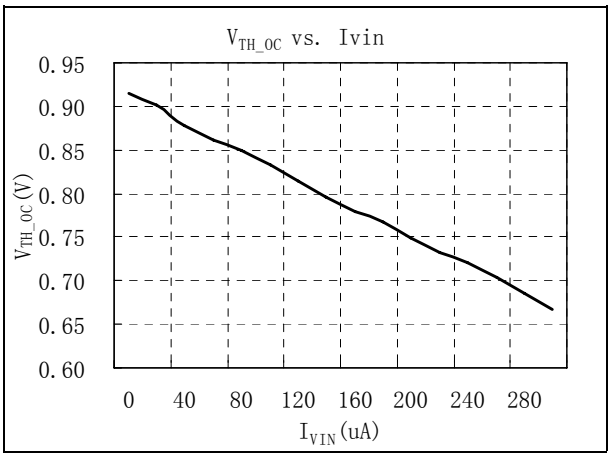

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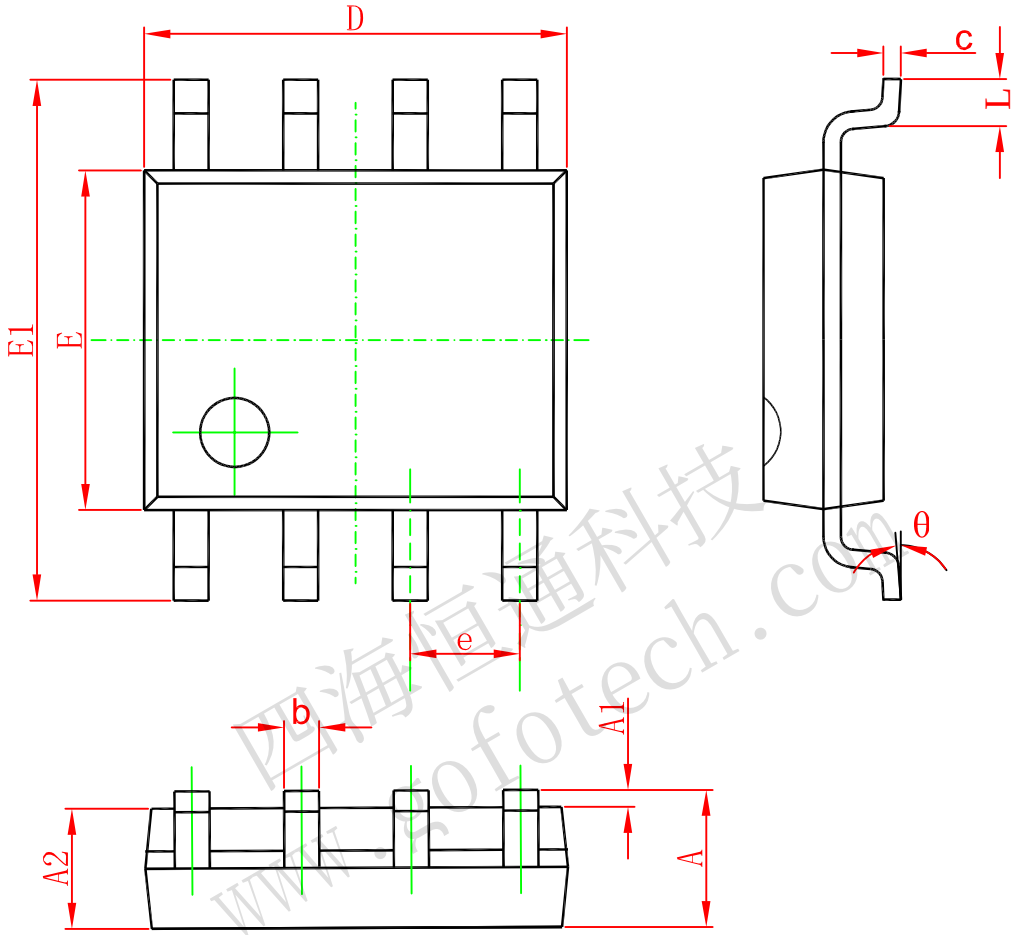
PACKAGE INFORMATION

(1) SOP8



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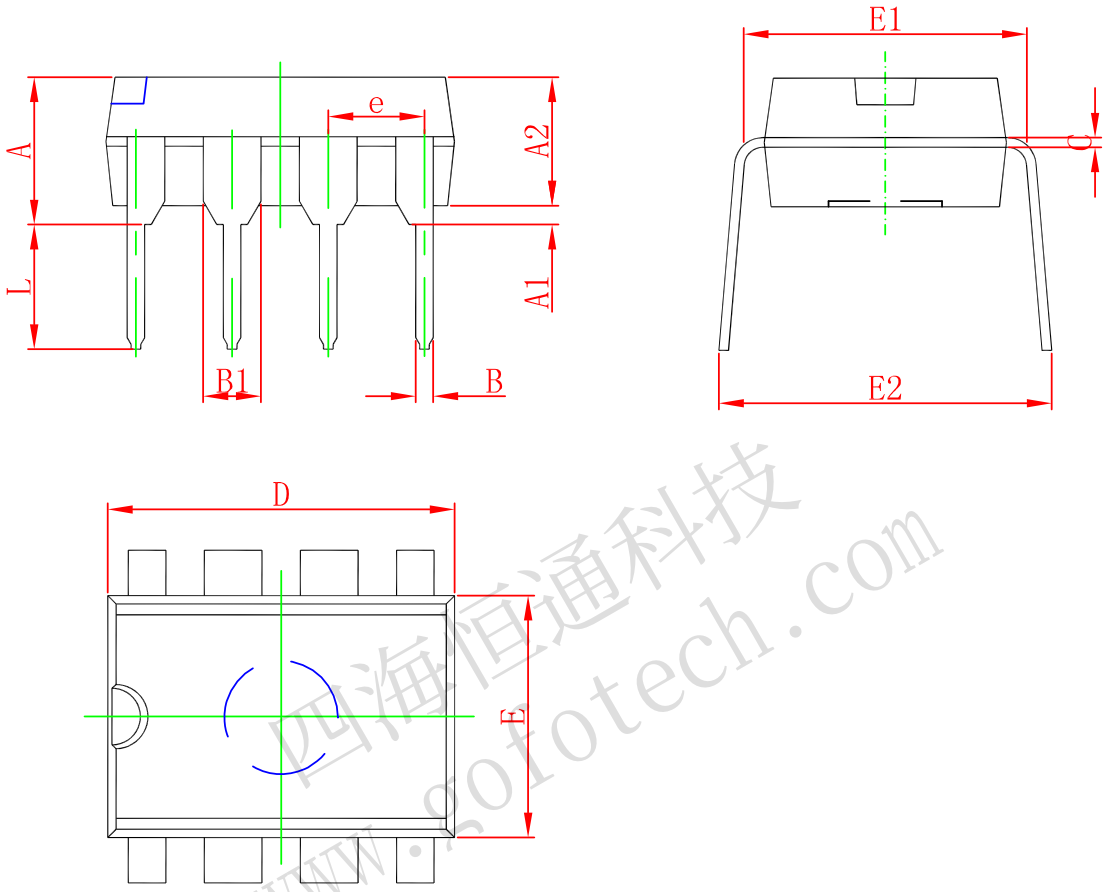
SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCH	
	MIN	MAX	MIN	MAX
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

PACKAGE INFORMATION

(2) DIP8



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SYMBOL	DIMENSIONS IN MILLIMETERS		DIMENSIONS IN INCHES	
	MIN	MAX	MIN	MAX
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.380	0.570	0.015	0.022
B1	1.524 (BSC)		0.060 (BSC)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.26
E1	7.320	7.920	0.288	0.312
e	2.540(BSC)		0.100(BSC)	
L	3.000	3.600	0.118	0.142
E2	8.400	9.000	0.331	0.354