

J174, J175

P-Channel Silicon Junction Field-Effect Transistor

- Choppers
- Commutators
- Analog Switches

Absolute maximum ratings at $T_A = 25^\circ\text{C}$

Reverse Gate Source & Reverse Gate Drain Voltage	- 30 V
Continuous Forward Gate Current	50 mA
Continuous Device Power Dissipation	360 mW
Power Derating	3.27 mW/°C

At 25°C free air temperature:

Static Electrical Characteristics

		J174		J175		Unit	Process PJ99	
		Min	Max	Min	Max		Test Conditions	
Gate Source Breakdown Voltage	$V_{(BR)GSS}$	30		30		V	$I_G = 1\ \mu\text{A}, V_{DS} = 0\text{V}$	
Gate Reverse Current	I_{GSS}		1		1	nA	$V_{GS} = 20\text{V}, V_{DS} = 0\text{V}$	
Gate Source Cutoff Voltage	$V_{GS(OFF)}$	5	10	3	6	V	$V_{DS} = -15\text{V}, I_D = -10\ \text{nA}$	
Drain Saturation Current (Pulsed)	I_{DSS}	- 20	- 125	- 7	- 70	mA	$V_{DS} = -15\text{V}, V_{GS} = 0\text{V}$	
Drain Cutoff Current	$I_{D(OFF)}$		- 1		- 1	nA	$V_{DS} = -15\text{V}, V_{GS} = 10\text{V}$	

Dynamic Electrical Characteristics

		Max	Max			
Drain Source ON Resistance	$r_{ds(on)}$	85	85	Ω	$V_{GS} = 0, V_{DS} \leq 0.1\text{V}$	$f = 1\ \text{kHz}$

Dynamic Electrical Characteristics

		Typ	Typ			
Drain Gate Capacitance	C_{gd}	5.5	5.5	pF	$V_{DS} = 0\text{V}, V_{GS} = 10\text{V}$	$f = 1\ \text{MHz}$
Source Gate Capacitance	C_{gs}	5.5	5.5	pF	$V_{DS} = 0\text{V}, V_{GS} = 10\text{V}$	$f = 1\ \text{MHz}$
Drain Gate + Source Gate Capacitance	$C_{gd} + C_{gs}$	32	32	pF	$V_{DS} = V_{GS} = 0\text{V}$	$f = 1\ \text{MHz}$

Switching Characteristics

						J174	J175	
Turn ON Delay Time	$t_{d(on)}$	2	5	ns	V_{DD}	- 10	- 6	V
Rise Time	t_r	5	10	ns	$V_{GS(OFF)}$	12	8	V
Turn OFF Delay Time	$t_{d(off)}$	5	10	ns	R_L	560	1.2k	Ω
Fall Time	t_f	10	20	ns	$V_{GS(ON)}$	0	0	V

TO-226AA Package

Dimensions in Inches (mm)

Pin Configuration

1 Drain, 2 Gate, 3 Source

Surface Mount

SMPJ174, SMPJ175



1000 N. Shiloh Road, Garland, TX 75042
(972) 487-1287 FAX (972) 276-3375

www.interfet.com