SRM20256L10/12

CMOS 256K-BIT STATIC RAM

- **Low Supply Current**
- **Access Time 100ns/120ns**
- **32,768 Words x 8-Bit Asynchronous**

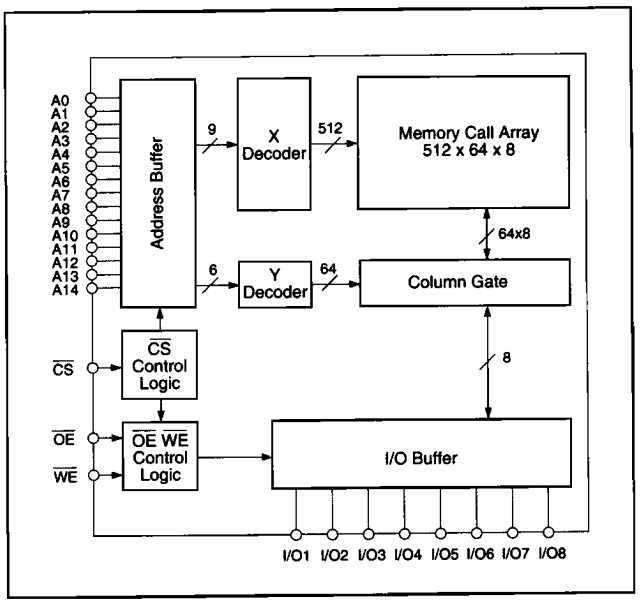
■ DESCRIPTION

The SRM20256L10/12 is a 32,768 word x 8-bit asynchronous, static, random access memory fabricated using an advanced CMOS technology. Its very low standby power requirement makes it ideal for applications requiring non-volatile storage with back-up batteries. The asynchronous and static nature of the memory requires no external clock or refresh circuit. Input and output ports are TTL compatible and the 3-state output allows easy expansion of memory capacity.

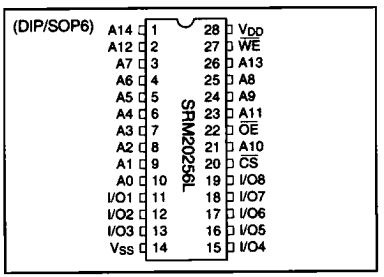
■ FEATURES

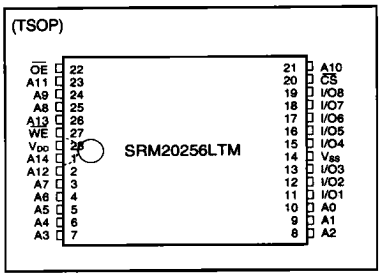
- Fast access time ..... SRM20256L10 ..... 100ns (Max)
  SRM20256L12 ..... 120ns (Max)
- Low supply current ..... standby : 2μA (Typ)
  operation : 13mA/1MHz (Typ)
- Completely static ..... no clock required
- Single power supply ... 5V ± 10%
- TTL compatible inputs and outputs
- 3-state output
- Battery back-up operation
- Package ..... SRM20256LC10/12 28-pin DIP (plastic)
  SRM20256LM10/12 28-pin SOP2 (plastic)
  SRM20256LTM10/12 28-pin TSOP(1) (plastic)
  SRM20256LRM10/12 28-pin-R1 TSOP(1) (plastic)

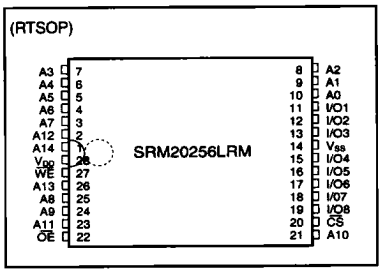
■ BLOCK DIAGRAM



■ PIN CONFIGURATION







■ PIN DESCRIPTION

A0 to A14	Address Input
$\overline{WE}$	Write enable
$\overline{OE}$	Output Enable
$\overline{CS}$	Chip Select
I/O1 to 8	Data I/O
VDD	Power Supply (+5V)
Vss	Power Supply (0V)

■ ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V)

Parameter	Symbol	Ratings	Unit
Supply voltage	V_{DD}	-0.5 to 7.0	V
Input voltage	V_I	-0.5* to 7.0	V
Input/Output voltage	$V_{I/O}$	-0.5* to V_{DD}+0.3	V
Power dissipation	P_D	1.0	W
Operating temperature	T_{opr}	0 to 70	°C
Storage temperature	T_{stg}	-65 to 150	°C
Soldering temperature and time	T_{sol}	260°C, 10s (Lead only)	—

* V_I, $V_{I/O}$ (Min) = –3V when pulse width is less than or equal to 50ns

■ DC RECOMMENDED OPERATING CONDITIONS

(V_{SS}=0V, Ta = 0 to 70°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{DD}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	V_{DD} + 0.3	V
	V_{IL}	-0.3 *	0	0.8	V

* V_{IL} (Min) = –3.0V when pulse width is less than or equal to 50ns

■ ELECTRICAL CHARACTERISTICS

● DC Electrical Characteristics

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	SRM20256L10			SRM20256L12			Unit
			Min	Typ*	Max	Min	Typ*	Max	
Input leakage	I_{LI}	V_I = 0 to V_{DD}	-1	—	1	-1	—	1	µA
Standby supply current	I_{DDS}	$\overline{CS}$ = V_{IH}	—	0.5	3.0	—	0.5	3.0	mA
	I_{DDS1}	$\overline{CS}$ ≥ V_{DD} -0.2V	—	2	100	—	2	100	µA
Average operating current	I_{DDA}	V_I=V_{IL}, V_{IH}, $I_{I/O}$ = 0mA, tcyc=Min	—	40	70	—	37	70	mA
	I_{DDA1}	V_I=V_{IL}, V_{IH}, $I_{I/O}$ = 0mA, tcyc=1µs	—	13	—	—	13	—	mA
Operating supply current	I_{DDO}	V_I=V_{IL}, V_{IH}, $I_{I/O}$ = 0mA	—	25	45	—	25	45	mA
Output leakage	I_{LO}	$\overline{CS}$ = V_{IH}, or $\overline{WE}$ = V_{IL}, or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{DD}	-1	—	1	-1	—	1	µA
High level output voltage	V_{OH}	I_{OH}= -1.0mA	2.4	V_{DD}-0.1	—	2.4	V_{DD}-0.1	—	V
Low level output voltage	V_{OL}	I_{OL}= 2.1mA	—	0.2	0.4	—	0.2	0.4	V

* Typical values are measured at T_a=25°C and V_{DD}=5.0V.

● Terminal Capacitance

(f = 1MHz, Ta = 25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Address capacitance	C_{ADD}	V_{ADD} = 0V	—	—	8	pF
Input capacitance	C_I	V_I = 0V	—	—	8	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$ = 0V	—	—	8	pF

● AC Electrical Characteristics

O Read Cycle

(V_{DD} = 5V ± 10%, V_{SS} = 0V, Ta = 0 to 70°C)

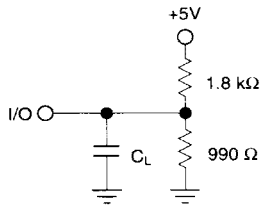
Parameter	Symbol	Conditions	SRM20256L10		SRM20256L12		Unit
			Min	Max	Min	Max	
Read cycle time	t_{RC}	*1	100	—	120	—	ns
Address access time	t_{ACC}		—	100	—	120	ns
$\overline{CS}$ access time	t_{ACS}		—	100	—	120	ns
$\overline{OE}$ access time	t_{OE}		—	50	—	60	ns
$\overline{CS}$ output set time	t_{CLZ}	*2	10	—	10	—	ns
$\overline{CS}$ output floating	t_{CHZ}		—	35	—	40	ns
$\overline{OE}$ output set time	t_{OLZ}		5	—	5	—	ns
$\overline{OE}$ output floating	t_{OHZ}		—	35	—	40	ns
Output hold time	t_{OH}	*1	10	—	10	—	ns

O Write Cycle

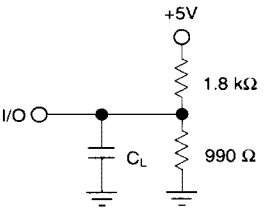
Parameter	Symbol	Conditions	SRM20256L10		SRM20256L12		Unit
			Min	Max	Min	Max	
Write cycle time	t_{WC}	*1	100	—	120	—	ns
Chip select time	t_{CW}		80	—	85	—	ns
Address valid to end of write	t_{AW}		80	—	85	—	ns
Address setup time	t_{AS}		0	—	0	—	ns
Write pulse width	t_{WP}		70	—	80	—	ns
Address hold time	t_{WR}		0	—	0	—	ns
Input data set time	t_{DW}		45	—	50	—	ns
Input data hold time	t_{DH}		0	—	0	—	ns
Write to Output floating	t_{WHZ}	*2	—	35	—	40	ns
Output Active from end of write	t_{OW}		10	—	10	—	ns

*1 Test conditions
1. Input pulse level: 0.6V to 2.4V
2. tr = tf = 5ns
3. Input and output timing reference levels: 1.5V
4. Output load C_L = 100pF

*2 Test conditions
1. Input pulse level : 0.6V to 2.4V
2. tr = tf = 5ns
3. Input timing reference levels: 1.5V
4. Output timing reference levels: ±200mV (the level displaced from stable output voltage level)
5. Output load C_L = 5pF



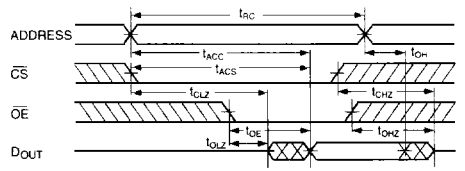
C_L = 100pF (Includes Jig Capacitance)



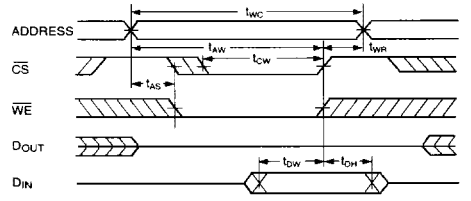
C_L = 5pF (Includes Jig Capacitance)

● Timing Chart

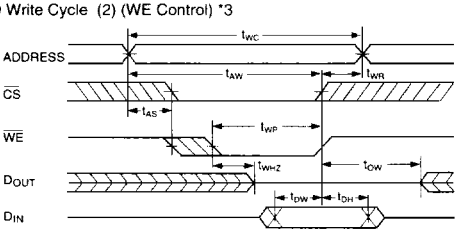
O Read Cycle *1



O Write Cycle (1) (CS Control) *2



O Write Cycle (2) (WE Control) *3



Note : *1. During read cycle time, WE is to be "H" level.
*2. During write cycle time that is controlled by CS, Output Buffer is in high impedance state whether OE level is "H" or "L".
*3. During write cycle time that is controlled by WE, Output Buffer is in high impedance state if OE is "H" level.

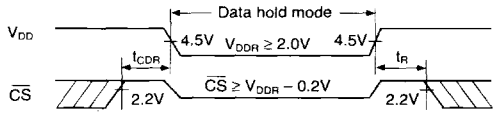
■ DATA RETENTION CHARACTERISTICS WITH LOW VOLTAGE POWER SUPPLY

(V_{SS}=0V, Ta = 0 to 70°C)

Parameter	Symbol	Conditions	Min	Typ*1	Max	Unit
Data retention supply voltage	V_{DDR}		2.0	—	5.5	V
Data retention current	I_{DDR}	V_{DD} = 3V, $\overline{CS} \geq V_{DDR}$-0.2V	—	1	50	µA
Chip select data hold time	t_{CDR}		0	—	—	ns
Operation recovery time	t_R		t_{RC}*2	—	—	ns

*1 Typical values are measured at 25°C
*2 tRC = Read cycle time

Data Retention Timing



■ FUNCTIONS

● Truth Table

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	A0 to A14	DATA I/O	MODE	I_{DD}
H	—	—	—	Hi-Z	Standby	I_{DDS}, I_{DDS1}
L	X	L	Stable	D_{IN}	Write	I_{DDA}, I_{DDA1}
L	L	H	Stable	D_{OUT}	Read	I_{DDA}, I_{DDA1}
L	H	H	Stable	Hi-Z	Output disable	I_{DDA}, I_{DDA1}

X : "H" or "L", —: "H", "L" or "Hi-Z"

● Read Mode

The Data appear when the address is setted while holding $\overline{CS}$="L", $\overline{OE}$="L" and $\overline{WE}$="H". When $\overline{OE}$="H", Data I/O terminals are in high impedance state, that makes circuit design and bus control easy.

● Write Mode

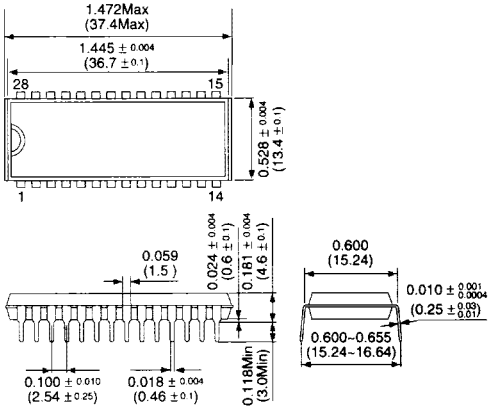
There are the following 3 ways of writing data into memory.
(1) Hold $\overline{CS}$="L" and $\overline{WE}$="L", set address.
(2) Hold $\overline{CS}$="L", then set address and give "L" pulse to $\overline{WE}$.
(3) After setting addresses, give "L" pulse to both $\overline{CS}$ and $\overline{WE}$.
In above any case data on the DATA I/O terminals are latched up into the SRM20256L10/12 when $\overline{CS}$ or $\overline{WE}$ is in positive-going. Since DATA I/O terminals are high impedance when $\overline{CS}$ or $\overline{OE}$="H", bus contention between data driver and memory outputs can be avoided.

● Standby Mode

When $\overline{CS}$ is "H" the SRM20256L10/12 become in the stand-by mode. In this mode, data I/O terminals are Hi-Z, and all inputs of addresses, $\overline{WE}$ and data can be any "H" or "L". When $\overline{CS}$ is over than V_{DD}-0.2V, the SRM20256L10/12 is in the data retention battery back-up mode, in this case, there is a small current in the SRM20256L10/12 which flow through the high resistance of the memory cells.

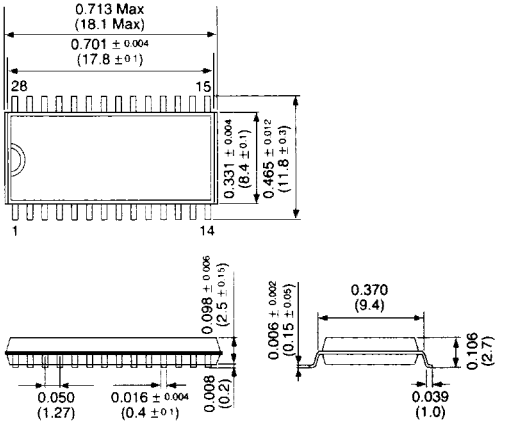
■ PACKAGE DIMENSIONS

Plastic DIP-28pin



unit : inch (mm)

Plastic SOP2-28pin*

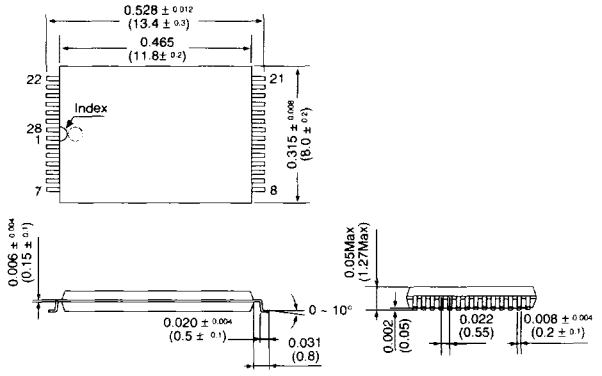


unit : inch (mm)

* Represents SRM20256LM10/12 that has the same electrical characteristics as SRM20256LC10/12.

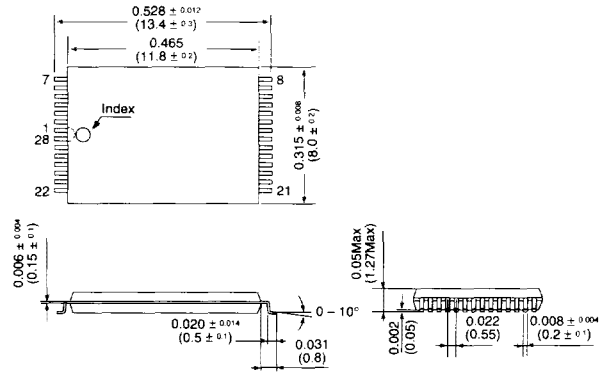
■ PACKAGE DIMENSIONS

Plastic TSOP (1)-28 pin



unit : inch (mm)

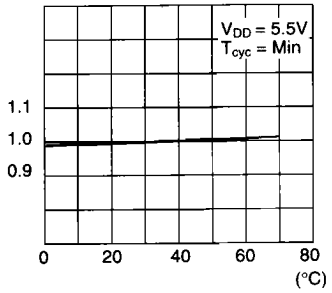
Plastic RTSOP (1)-28 pin-R1



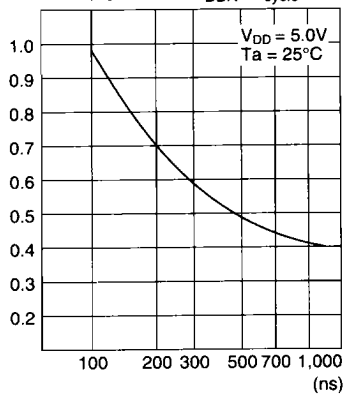
unit : inch (mm)

■ CHARACTERISTICS CURVES

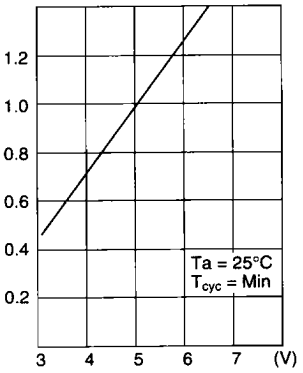
Normalized I_{DDA}—Ta



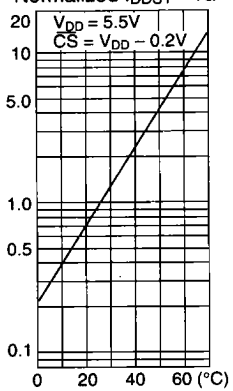
Normalized I_{DDA}—t_{cycle}



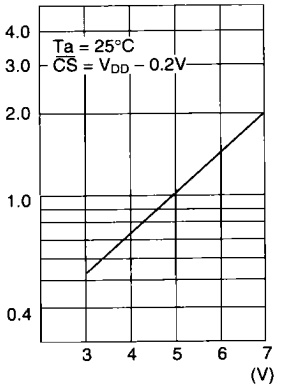
Normalized I_{DDA}—V_{DD}



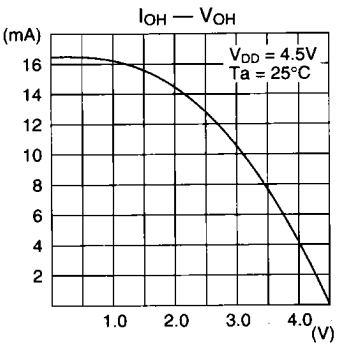
Normalized I_{DDS1}—Ta



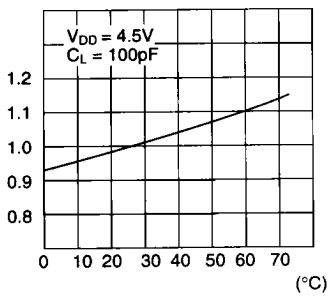
Normalized I_{DDS1}—V_{DD}



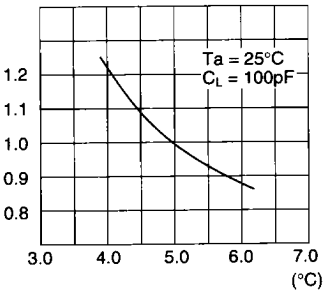
I_{OH} — V_{OH}



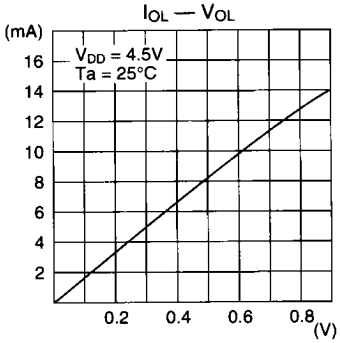
Normalized t_{ACC}·t_{ACS}—Ta



Normalized t_{ACC}·t_{ACS}—V_{DD}



I_{OL} — V_{OL}



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