

RoHS Compliant Product
A suffix of "-C" specifies halogen free

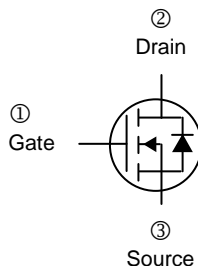
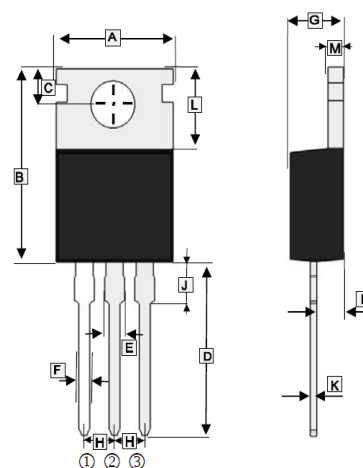
DESCRIPTION

The SSE04N65SL is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent $R_{DS(on)}$ and gate charge for most of the synchronous buck converter applications .

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

TO-220P



| REF. | Millimeter | | REF. | Millimeter | |
|------|------------|------|------|------------|------|
| | Min. | Max. | | Min. | Max. |
| A | 9.3 | 10.6 | H | 2.54 | BCS. |
| B | 14.2 | 16.5 | I | 1.8 | 2.9 |
| C | 2.7 BSC. | | J | 2.6 | 3.95 |
| D | 12.6 | 14.7 | K | 0.3 | 0.6 |
| E | 1.0 | 1.8 | L | 5.8 | 7.0 |
| F | 0.4 | 1.0 | M | 1.2 | 1.45 |
| G | 3.6 | 4.8 | | | |

ABSOLUTE MAXIMUM RATINGS ($T_A=25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Rating | Unit |
|--|-----------------|---------------------------------|-----------------------------|
| Drain-Source Voltage | V_{DS} | 650 | V |
| Gate-Source Voltage | V_{GS} | ± 30 | V |
| Continuous Drain Current | I_D | $T_C=25^\circ\text{C}$ | 4 |
| | | $T_C=100^\circ\text{C}$ | 2.8 |
| Pulsed Drain Current | I_{DM} | 16 | A |
| Total Power Dissipation | P_D | $T_C=25^\circ\text{C}$ | 100 |
| | | Derate above 25°C | 0.8 |
| Single Pulse Avalanche Energy ¹ | E_{AS} | 202 | mJ |
| Operating Junction and Storage Temperature Range | T_J, T_{STG} | -55~150 | $^\circ\text{C}$ |
| Thermal Resistance Rating | | | |
| Maximum Thermal Resistance Junction-Ambient | $R_{\theta JA}$ | 62.5 | $^\circ\text{C} / \text{W}$ |
| Maximum Thermal Resistance Junction-Case | $R_{\theta JC}$ | 1.25 | $^\circ\text{C} / \text{W}$ |

Notes:

1. $L=30\text{mH}, I_{AS}=3.36\text{A}, V_{DD}=150\text{V}, R_G=25\Omega$, Starting $T_J = 25^\circ\text{C}$

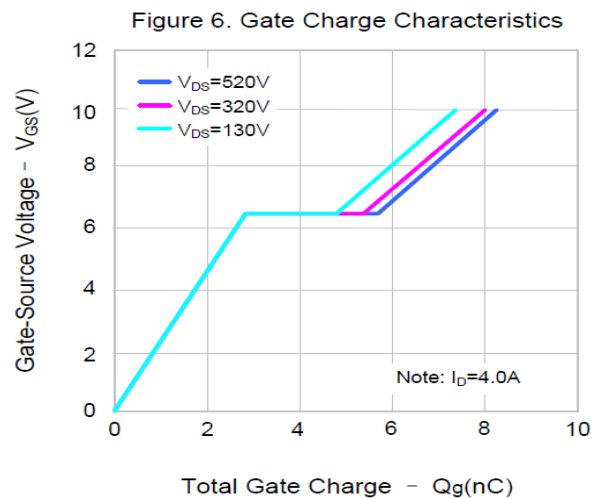
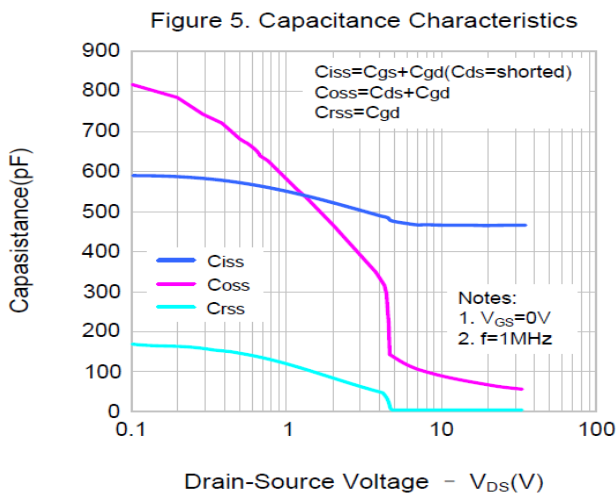
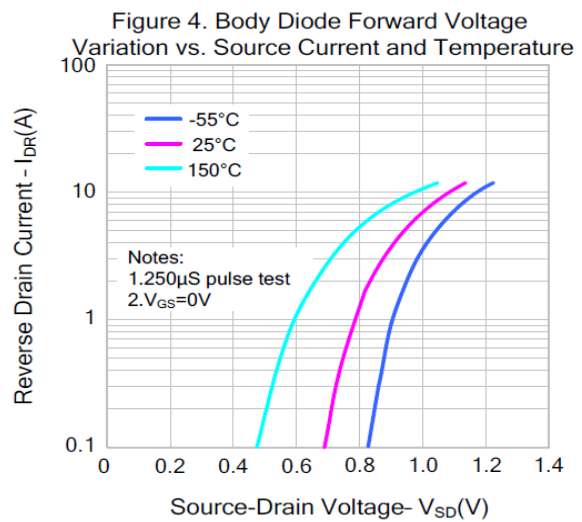
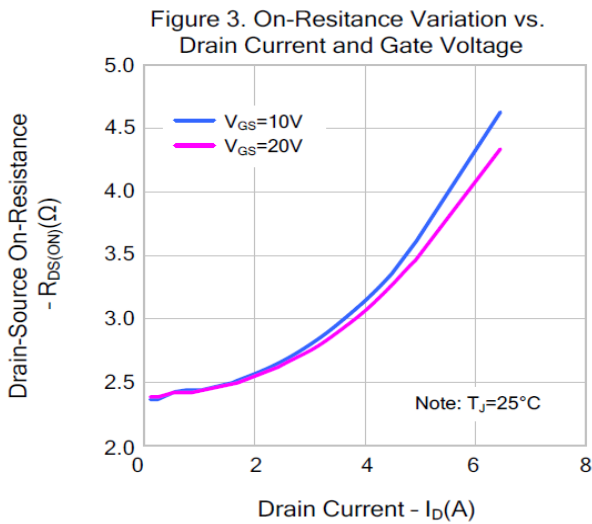
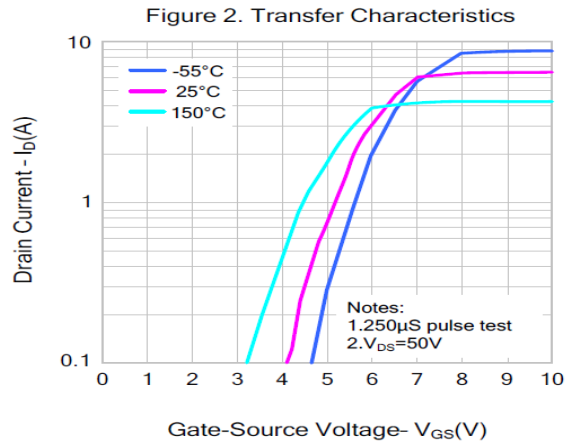
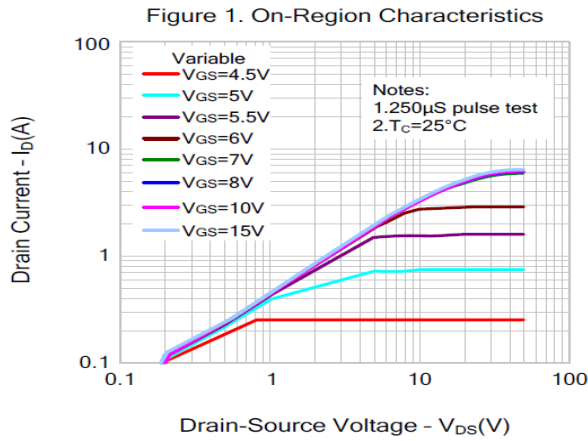
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Teat Conditions |
|------------------------------------|--------------|------|--------|-----------|---------------|---|
| Static | | | | | | |
| Drain-Source Breakdown Voltage | BV_{DSS} | 650 | - | - | V | $V_{GS}=0, I_D=250\mu\text{A}$ |
| Gate-Threshold Voltage | $V_{GS(th)}$ | 2 | - | 4 | V | $V_{DS}=V_{GS}, I_D=250\mu\text{A}$ |
| Gate-Source Leakage Current | I_{GSS} | - | - | ± 100 | nA | $V_{GS}= \pm 30\text{V}$ |
| Drain-Source Leakage Current | I_{DSS} | - | - | 1 | μA | $V_{DS}=650\text{V}, V_{GS}=0$ |
| Static Drain-Source On-Resistance | $R_{DS(ON)}$ | - | 2.3 | 2.7 | Ω | $V_{GS}=10\text{V}, I_D=2\text{A}$ |
| Total Gate Charge ^{1,2} | Q_g | - | 8.03 | - | nC | $I_D=4\text{A}$ $V_{DS}=520\text{V}$ $V_{GS}=10\text{V}$ |
| Gate-Source Charge ^{1,2} | Q_{gs} | - | 2.57 | - | | |
| Gate-Drain Change ^{1,2} | Q_{gd} | - | 3.03 | - | | |
| Turn-on Delay Time ^{1,2} | $T_{d(on)}$ | - | 16.6 | - | nS | $V_{DD}=325\text{V}$ $I_D=4\text{A}$ $R_G=25\Omega$ |
| Rise Time ^{1,2} | T_r | - | 37.33 | - | | |
| Turn-off Delay Time ^{1,2} | $T_{d(off)}$ | - | 18 | - | | |
| Fall Time ^{1,2} | T_f | - | 19.2 | - | | |
| Input Capacitance | C_{iss} | - | 464 | - | pF | $V_{GS}=0$ $V_{DS}=25\text{V}$ $f=1.0\text{MHz}$ |
| Output Capacitance | C_{oss} | - | 54 | - | | |
| Reverse Transfer Capacitance | C_{rss} | - | 1.32 | - | | |
| Source-Drain Diode | | | | | | |
| Diode Forward Voltage | V_{SD} | - | - | 1.4 | V | $I_S=4\text{A}, V_{GS}=0$ |
| Continuous Source Current | I_S | - | - | 4 | A | Integral Reverse P-N Junction Diode in the MOSFET |
| Pulsed Source Current | I_{SM} | - | - | 16 | A | |
| Reverse Recovery Time | T_{rr} | - | 455.23 | - | ns | $I_S=4\text{A}, V_{GS}=0,$ $di_f/dt=100\text{A}/\mu\text{S}$ |
| Reverse Recovery Charge | Q_{rr} | - | 2.01 | - | μC | |

Notes:

1. Pulse Test: Pulse width $\leq 300\mu\text{S}$, Duty cycle $\leq 2\%$
2. Essentially independent of operating temperature.

CHARACTERISTIC CURVES



CHARACTERISTIC CURVES

Figure 7. Breakdown Voltage Variation vs. Temperature

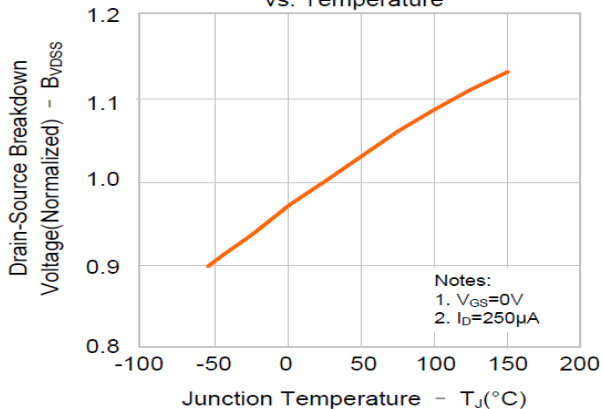


Figure 8. On-resistance Variation vs. Temperature

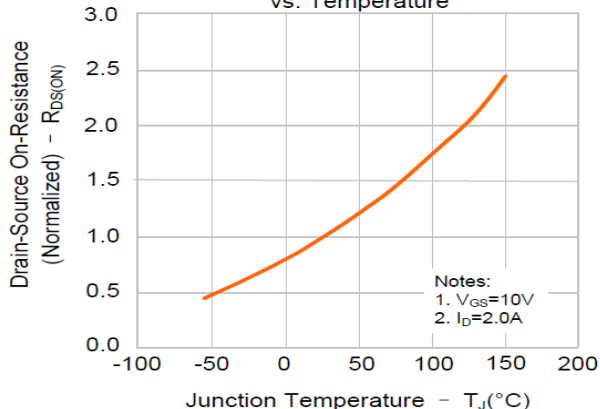


Figure 9 Max. Safe Operating Area

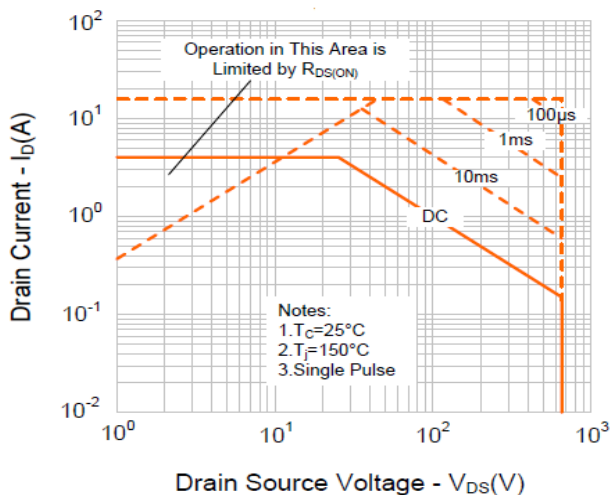
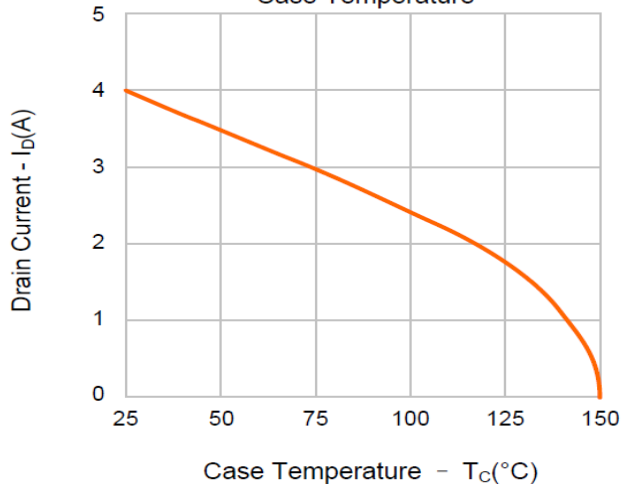
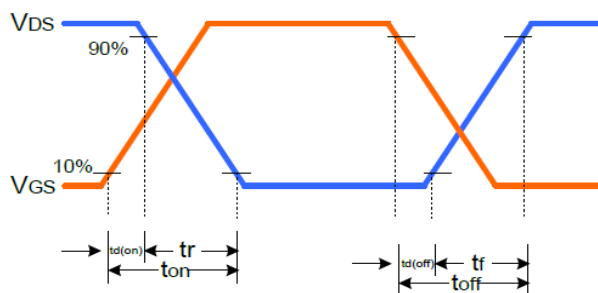
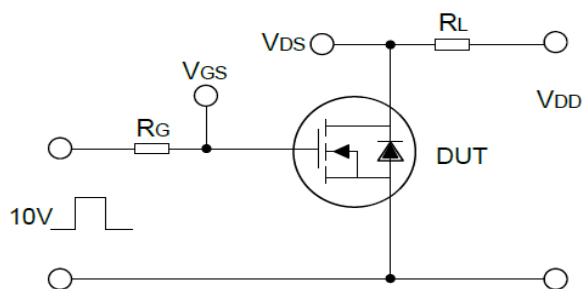


Figure 10. Maximum Drain Current vs. Case Temperature

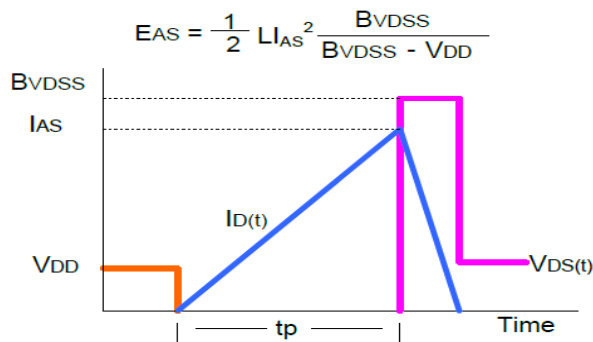
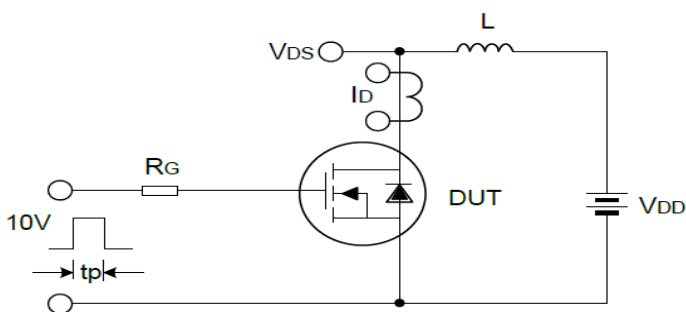


TYPICAL TEST CURVES

Resistive Switching Test Circuit & Waveform



Unclamped Inductive Switching Test Circuit & Waveform



Gate Charge Test Circuit & Waveform

