System Power PWM Controller for Notebook Computers

Features

- **Built in 2 PWM Controller into single chip**
- **High Input Battery Voltage Range from 5.5V to 28V**
- **Fixed 1.0MHz Switching Frequency for Individual Channel**
- **Built in Programmable Inductor DCR Sense For Inductor Current Sense Function**
- **Built in Current Mode Control with fully Support MLCC Output Capacitor**
- **Built in 180 degrees Phase Shift Function**
- **Built in PWM/PSM/Ultra Sonic PFM (25kHz) Control Schemes**
- **Built in Internal 5V/175mA and 3.3V/50mA Linear Regulators**
- **0.5V Reference Voltage**
- **Built in Digital Soft-start**
- **Latch Off Mode for Both Channels**
- **Over-Temperature Protection**
- **Built in SYSPOK Report function for 2 PWM Channels**
- **Available in TQFN4x4-24 and QFN3x3-20 Package**
- **Halogen and Lead Free Available (RoHS Compliant)**

Applications

- **NB**

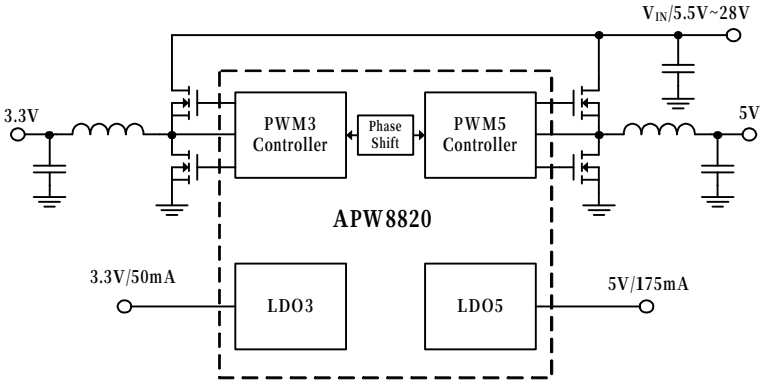
General Description

The APW8820 offers a compact power supply solution to provide 2 voltages required by notebook application. The 2 PWM controllers use current-mode scheme with phase shift 180 degrees control scheme allow to use MLCC output capacitors. The higher fixed 1MHz switching frequency allows to use thin and small filtered components. The APW8820 provides good transient response and accurate DC output voltage in either PSM or PWM Mode. In Pulse Skipping Modulation Mode (PSM), the APW8820 provides high efficiency over light to heavy loads with loading modulated switching frequencies. The unique ultrasonic mode maintains the switching frequency above 25kHz, which eliminates noise in audio applications. The APW8820 built in individual enable control input on 2 channels for flexible power sequence adjustment. The power-good outputs (SYSPOK) indicate the operating mode of the PWMx.

The APW8820 has been equipped with excellent protection functions: Power-on-RESET (POR), over-current protection (OCP), over-voltage protection OVP, under-voltage protection (UVP) and over-temperature protection (OTP) to prevent the device operate under abnormal condition or adjacent pin shortage.

The APW8820 is available in TQFN4x4-24 and QFN3x3-20 package.

Simplified Application Circuit



Ordering and Marking Information

APW8820 □□□-□□□

- Assembly Material
- Handling Code
- Temperature Range
- Package Code

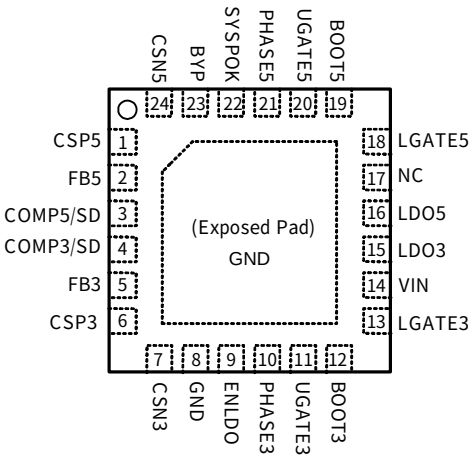
Package Code
QB: TQFN4x4-24 QA: QFN3x3-20
Operating Ambient Temperature Range
I : -40 to 85°C
Handling Code
TR : Tape & Reel
Assembly Material
G : Halogen and Lead Free Device

APW8820 QB: APW8820 XXXXX XXXXX - Date Code

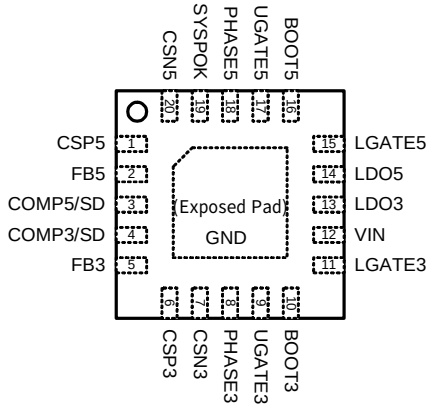
APW8820 QA: APW 8820 XXXXX XXXXX - Date Code

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J-STD-020D for MSL classification at lead-free peak reflow temperature. ANPEC defines "Green" to mean lead-free (RoHS compliant) and halogen free (Br or Cl does not exceed 900ppm by weight in homogeneous material and total of Br and Cl does not exceed 1500ppm by weight).

Pin Configuration



TQFN4x4-24
Top View



QFN3x3-20
Top View

Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Rating	Unit
V_{IN}	Input Bias Supply Voltage (VIN to GND)		-0.3 ~ 30	V
V_{LDOx}	LDOx Supply Voltage (LDOx to GND)		-0.3 ~ 7	V
V_{BOOTx}	VBOOTx Supply Voltage	V_{BOOTx} to V_{PHASEx}	-0.3 ~ 7	V
		V_{BOOTx} to GND	-0.3 ~ 37	V
	UGATEx to PHASEx Voltage	<20ns pulse width	-5 ~ V_{BOOTx}+5	V
		>20ns pulse width	-0.3 ~ V_{BOOTx}+0.3	V
	LGATEx to GND Voltage	<20ns pulse width	-5 ~ 9	V
		>20ns pulse width	-0.3 ~ 7	V
	PHASEx to GND Voltage	<20ns pulse width	-10 ~ 37	V
		>20ns pulse width	-0.3 ~ V_{IN} +0.3	V
	Input/Output to GND Voltage (FBx, CSNx, CSPx, COMPx, BYP, SYSPOK, ENLDO)		-0.3 ~ 7	V
P_D	Power Dissipation		Internally Limit	W
T_J	Maximum Junction Temperature		150	°C
T_{STG}	Storage Temperature		-65 ~ 150	°C
T_{SDR}	Maximum Lead Soldering Temperature (10 Seconds)		260	°C

Note1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

Thermal Characteristics

Symbol	Parameter		Typical Value	Unit
θ_{JA}	Junction-to-Ambient Resistance in free air (Note 2)	TQFN4x4-24 QFN3x3-20	41 50	°C/W
θ_{JC}	Case-to-Ambient Resistance in free air (Note 2)	TQFN4x4-24 QFN3x3-20	9 12	°C/W

Note 2: θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air.

Recommended Operating Conditions (Note 3)

Symbol	Parameter	Range	Unit
V_{IN}	Input Bias Supply Voltage (VIN to GND)	5.5 ~ 28	V
V_{OUT5}	5V PWM Converter Output Voltage	0.5 ~ 5.5	V
V_{OUT3}	3.3V PWM Converter Output Voltage	0.5 ~ 5.5	V
C_{IN}	Input Power Capacitor	4.7 ~	µF
C_{LDO5}	LDO5 Output Capacitor	4.7 ~	µF
T_A	Ambient Temperature	-40 ~ 85	°C
T_J	Junction Temperature	-40 ~ 125	°C

Note 3: Refer to the typical application circuit.

Electrical Characteristics

Unless otherwise specified, these specifications apply over V_{IN}=19V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW8820			Unit
			Min	Typ	Max	
SUPPLY CURRENT						
V_{IN}	Input Voltage Range		5.5	-	28	V
I_{VIN}	VIN Supply Current	UGATEx and LGATEx open	-	200	400	μA
	VIN Shutdown Input Current	COMPx=GND, ENLDO=GND	-	30	50	μA
POWER-ON-RESET (POR) THRESHOLDS						
V_{IN}	Rising VIN Voltage		4.1	4.2	4.3	V
	VIN POR Hysteresis		0.05	0.1	0.15	V
	Rising LDO5 Voltage		4.1	4.2	4.3	V
	LDO5 POR Hysteresis		0.05	0.1	0.15	V
REFERENCE VOLTAGE (FB5, FB3)						
V_{FBx}	Regulated Voltage	V_{IN}=5.5V~28V	-	0.5	-	V
		Over temperature range	-1.5	-	+1.5	%
	Output Voltage Accuracy (Note 4)	I_{OUT} = 0.3A ~ 8A, V_{IN}=6V~28V	-0.2	-	+0.2	%
I_{FBx}	FBx Input Current		-50	-	50	nA
LDO5 AND LDO3						
	LDO5 Voltage	VIN=5.5V ~ 28V, BYP=GND	4.90	5.00	5.10	V
	LDO5 Current Limit	VIN=5.5V ~ 28V, BYP=GND	175	-	330	mA
	BYP Threshold Voltage	V_{BYP} Rising	4.53	4.68	4.83	V
	LDO5 to BYP Switch ON Resistor		-	1.5	2.5	Ω
	LDO3 Voltage	V_{IN}>4.5V, I_{LOAD}=0mA	3.235	3.300	3.365	V
		V_{IN}<4.0V, I_{LOAD}=0mA	3.220	3.300	3.380	V
	LDO3 Load Regulation	I_{LOAD}=0 ~ 50mA	-	30	-	mV
OSCILLATOR						
F_{OSC}	Switching Frequency at PWM Mode (PWM5 & PWM3)	V_{IN}=5.5V ~ 28V, T_A= 25°C	0.9	1.0	1.1	MHz
		V_{IN}=5.5V ~ 28V, T_A= -40~85 °C	-15	-	15	%
F_{OSC_MI}	Switching Frequency at Ultra-sonic Mode	V_{IN}=5.5V ~ 28V	20	25	-	kHz
	Dead-time (Note 4)		-	25	-	ns
PWM GATE DRIVER						
	UGATEx Source Current	V_{BOOTx} = 5V, $V_{UGATEx-PHASEx}$=2.5V	-	0.5	-	A
	UGATEx Sink Current	V_{BOOTx} = 5V, $V_{UGATEx-PHASEx}$=2.5V	-	0.5	-	A
	LGATEx Source Current	V_{PVCC}=5V, V_{LGATEx}=2.5V	-	0.5	-	A
	LGATEx Sink Current	V_{PVCC}=5V, V_{LGATEx}=2.5V	-	0.5	-	A
	Duty Cycle		0	-	100	%
	Minimum on-time		-	100	-	ns
	Zero Crossing Voltage Threshold		-5	-	+5	mV

Electrical Characteristics (Cont.)

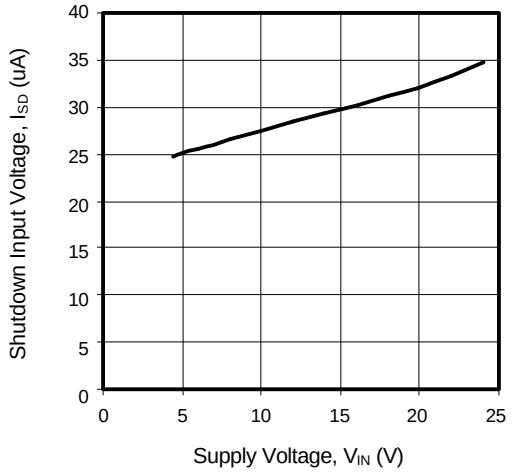
Unless otherwise specified, these specifications apply over V_{IN}=19V and T_A= 25°C.

Symbol	Parameter	Test Conditions	APW8820			Unit
			Min	Typ	Max	
CURRENT SENSE						
I_{CSPx}	CSPx Pin Input Current	V_{CSPx} = 5V	-100	-	+100	nA
I_{CSNx}	CSNx Pin Input Current	V_{CSNx} = 5V	-100	-	+100	nA
BOOTSTRAP SWITCH						
V_F	Forward Voltage	V_{LDO5} – $V_{BOOTx-GND}$, I_F = 10mA	-	0.5	0.8	V
I_R	Reverse Leakage	$V_{BOOTx-GND}$ = 30V, V_{PHASEx} = 25V, V_{LDO5} = 5V	-	-	1	µA
CURRENT MODE PWM CONTROL						
gm	Error Amplifier Transconductance (Note 4)	V_{IN}=5.5V ~ 28V	-	640	-	µA/V
	Open-Loop Gain (Note 4)	R_L = 10KΩ, C_L =10pF	-	80	-	dB
	Open-Loop Bandwidth (Note 4)	R_L = 10KΩ, C_L = 10pF	-	20	-	MHz
	FB Input Leakage Current	V_{FB} = 0.8V	-	0.1	1	µA
	COMP High Voltage		-	3	-	V
	COMP Low Voltage		-	0.5	-	V
	COMP Source Current	V_{COMP} = 2V	-	100	-	µA
	COMP Sink Current	V_{COMP} = 2V	-	100	-	µA
ENABLE CONTROL						
	ENLDO Input Voltage	Shutdown Threshold	-	-	0.4	V
		Enable Threshold	2.4	-	-	V
	PWM Shutdown Threshold	COMPx Threshold	-	-	0.45	V
INTERNAL SOFT-START						
T_{SS}	Soft-start Interval		-	1	-	ms
SYSPOK CONTROL						
	SYSPOK Threshold	FB5 and FB3 Rising	87	90	93	%
		FB5 or FB3 Falling	-	5	-	%
	SYSPOK Propagation Delay	FB5/FB3 Falling & Rising	-	10	-	µs
	SYSPOK Low Voltage	I_{SINK}=4mA	-	0.1	0.2	V
	SYSPOK Leakage Current	V_{SYSPOK}=5V	-	-	1	µA
R_{SYSPOK}	PWM5 Fault Detected	I_{PWMPOK}=5mA (sink)	90	120	150	Ω
	PWM3 Fault Detected	I_{PWMPOK}=5mA (sink)	45	60	75	Ω
PROTECTION for PWMx						
	OVP Rising Threshold		115	120	125	%
	UVP Falling Threshold		65	70	75	%
I_{OCSETx}	OCSETx Current Source		9	10	11	µA
	Over-Temperature Protection Rising Threshold		-	160	-	°C

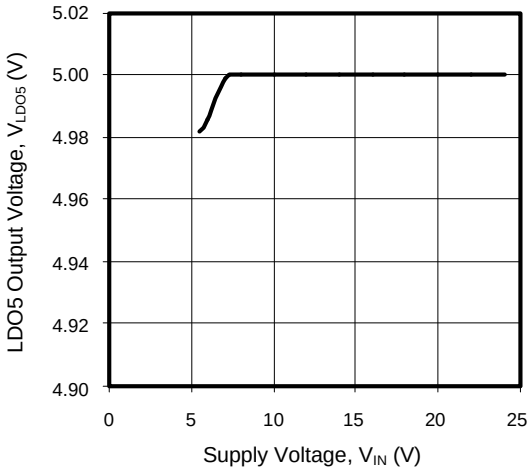
Note 4: Grauantee by design, not production test.

Typical Operating Characteristics

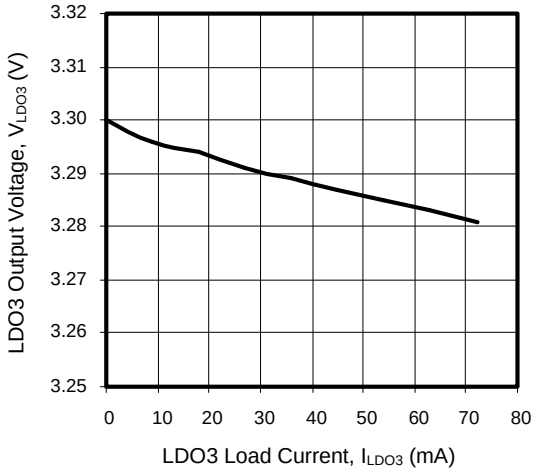
Shutdown Input Current vs. Supply Voltage



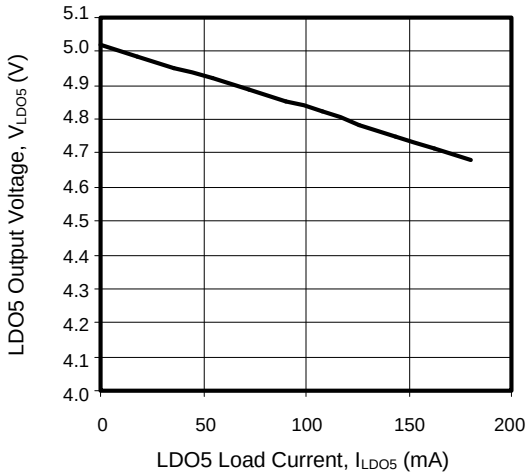
LDO5 Output Voltage vs. Supply Voltage



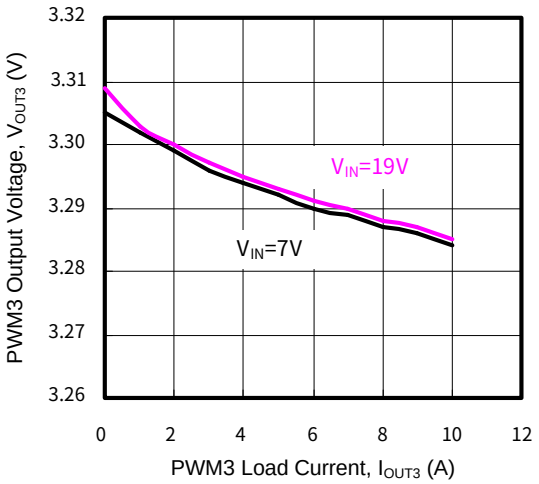
LDO3 Output Voltage vs. Load Current



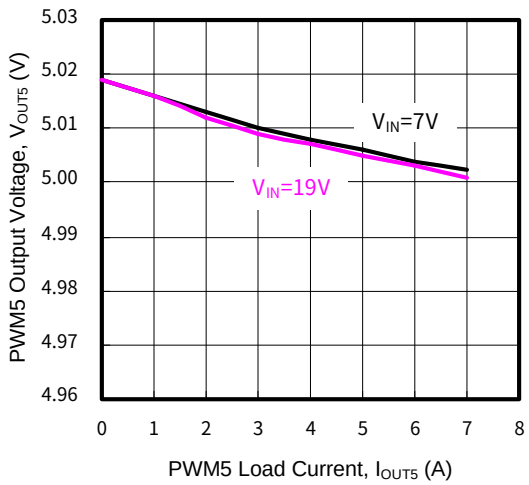
LDO5 Output Voltage vs. Load Current



PWM3 Output Voltage vs. Load Current



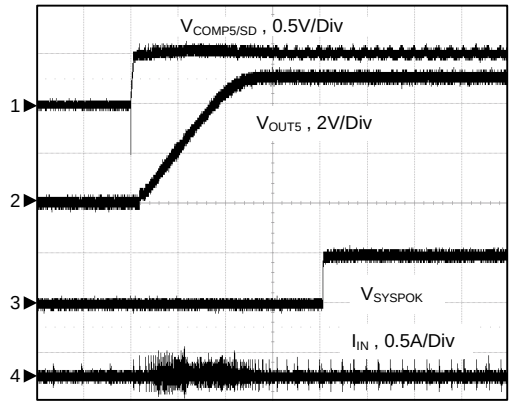
PWM5 Output Voltage vs. Load Current



Operating Waveforms

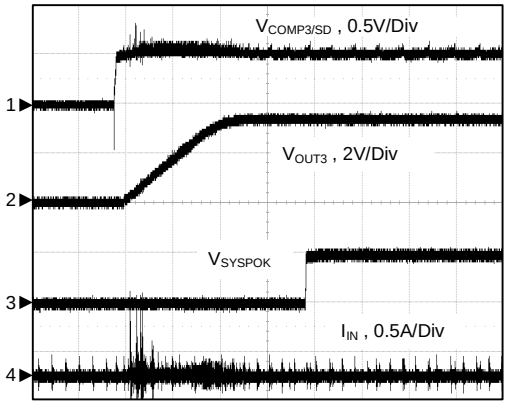
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A= 25°C unless otherwise specified.

Enable PWM5



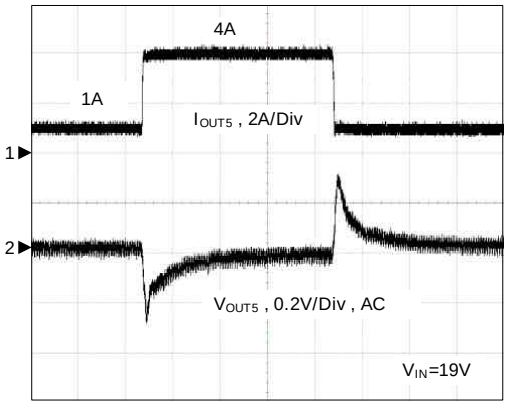
TIME: 0.5ms/Div

Enable PWM3



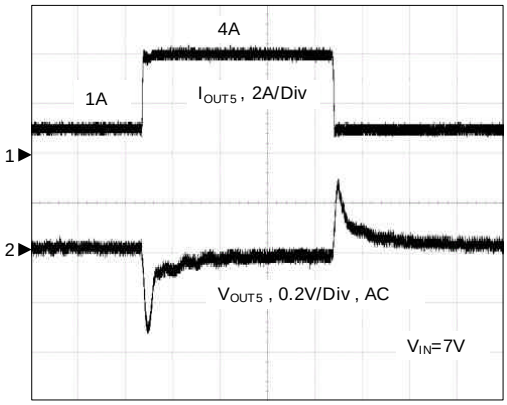
TIME: 0.5ms/Div

Load Transient Response of PWM 5



TIME: 20µs/Div

Load Transient Response of PWM 5

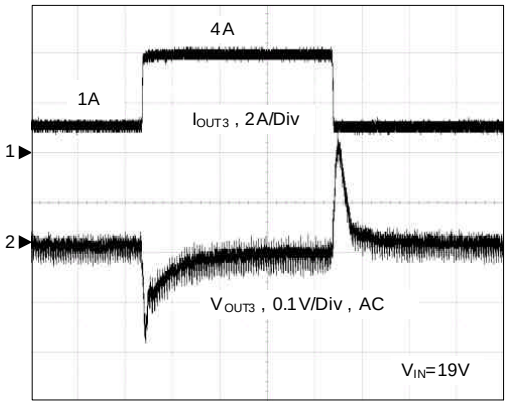


TIME: 20µs/Div

Operating Waveforms

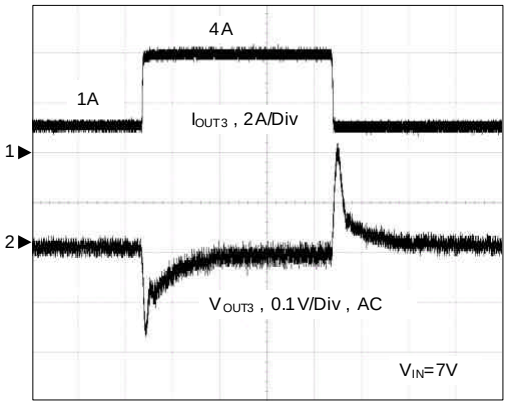
Refer to the typical application circuit. The test condition is V_{IN}=19V, T_A= 25°C unless otherwise specified.

Load Transient Response of PWM 3



TIME: 20µs/Div

Load Transient Response of PWM 3



TIME: 20µs/Div

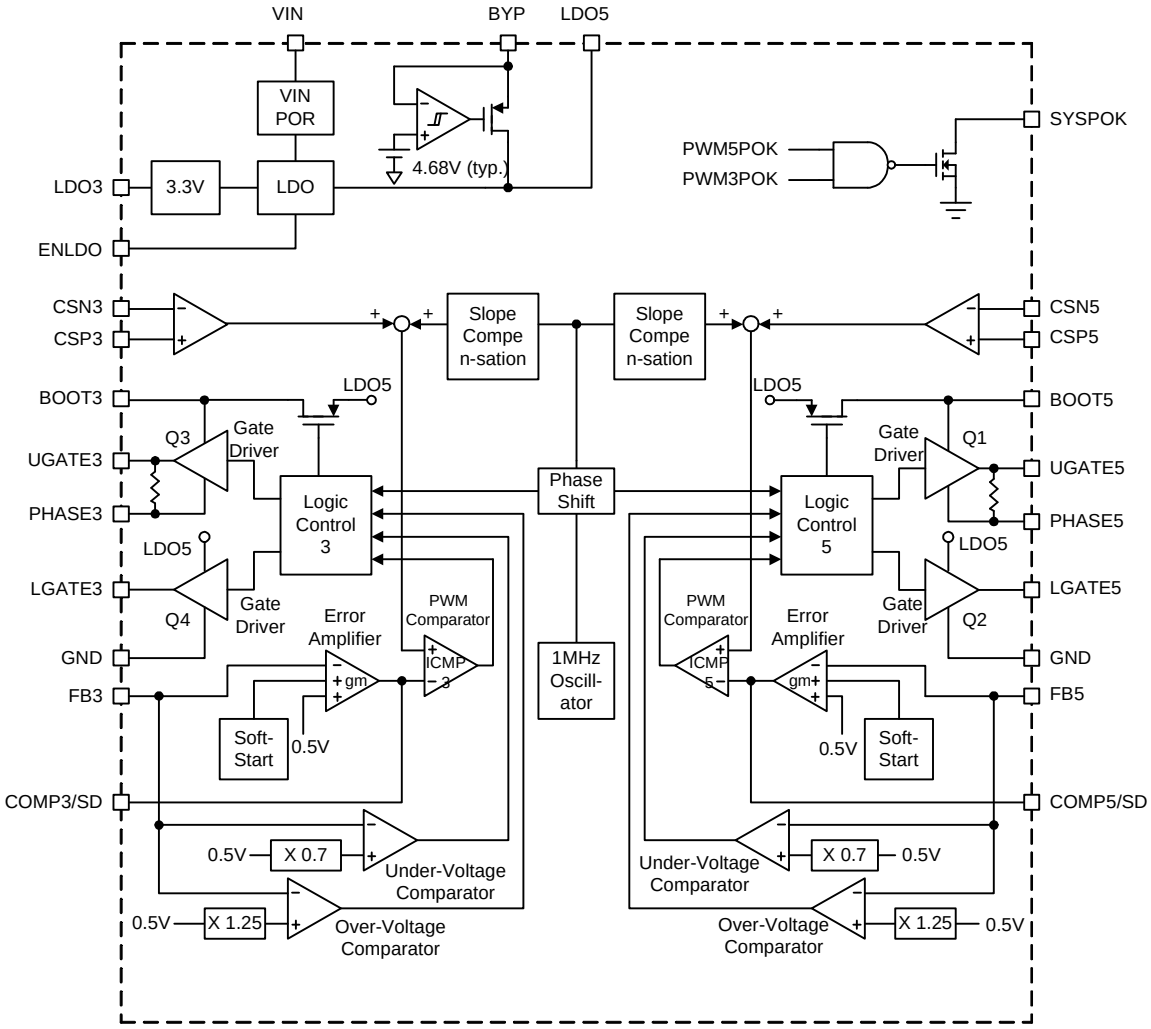
Pin Description

PIN			Function
TQFN4x4-24	QFN3x3-20	NAME	
1	1	CSP5	Positive Input of current sensing Amplifier for PWM5. This pin combined with CSN5 senses the inductor current through an RC network.
2	2	FB5	Feedback Input of PWM5. The converter senses feedback voltage via FB5 and regulates the FB5 voltage at 0.5V. Connecting FB5 with a resistor-divider from the output sets the output voltage of the converter.
3	3	COMP5/SD	This is a multiplexed pin. During the soft-start and normal converter operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB5 pin. Pulling COMP5/SD low ($V_{DISABLE}$=0.4V) will shut down the PWM5. Once the pull-down device is released, the COMP5/SD pin will start to rise. After the COMP5/SD pin exceeds the $V_{DISABLE}$ trip point, the PWM5 will begin a new initialization and soft-start cycle.
4	4	COMP3/SD	This is a multiplexed pin. During the soft-start and normal converter operation, this pin represents the output of the error amplifier. It is used to compensate the regulation control loop in combination with the FB3 pin. Pulling COMP3/SD low ($V_{DISABLE}$=0.4V) will shut down the PWM3. Once the pull-down device is released, the COMP3/SD pin will start to rise. After the COMP3/SD pin exceeds the $V_{DISABLE}$ trip point, the PWM3 will begin a new initialization and soft-start cycle.
5	5	FB3	Feedback Input of PWM3. The converter senses feedback voltage via FB3 and regulates the FB3 voltage at 0.5V. Connecting FB3 with a resistor-divider from the output sets the output voltage of the converter.
6	6	CSP3	Positive Input of current sensing Amplifier for PWM3. This pin combined with CSN3 senses the inductor current through an RC network.
7	7	CSN3	Positive Input of current sensing Amplifier for PWM3. This pin combined with CSN3 senses the inductor current through an RC network.
8	-	GND	Signal and Power Ground. Connected this pin to exposed pad.
9	-	ENLDO	Enable pin of LDO5/3. Forcing this pin above 2.4V enables the LDO5/3, or pulling this pin below 0.4V to shut it down. **Do not leave this pin floating.**
10	8	PHASE3	This pin is the return path for the high-side gate driver of PWM3. Connecting this pin to the high-side MOSFET source and connecting a capacitor to BOOT3 for the bootstrap voltage.
11	9	UGATE3	High-side Gate Driver Output of PWM3. This pin is connected to high-side MOSFET.
12	10	BOOT3	This pin provides the bootstrap voltage to the high-side gate driver of PWM3 for driving the N-channel MOSFET. An external capacitor connected from PHASE3 to BOOT3 is required for the high-side gate driver.
13	11	LGATE3	Low-side Gate Driver Output of PWM3. This pin is the gate driver for low-side MOSFET.
14	12	VIN	Power Supply Input. Connect a nominal 5V to 28V power supply voltage to this pin. A power-on-reset function monitors the input voltage at this pin. It is recommended that a decoupling capacitor (1 to 10µF) be connected to GND for noise decoupling.
15	13	LDO3	Internal 3.3V LDO Output.
16	14	LDO5	Power Supply of Internal Gate Drivers. When V_{BYP} below 4.68V, the LDO5 internally connect to internal LDO. When VBYP exceeds 4.68V, an internal switch connects LDO5 to BYP.
17	-	NC	No Internal Connection.
18	15	LGATE5	Low-side Gate Driver Output of PWM5. This pin is the gate driver for low-side MOSFET.
19	16	BOOT5	This pin provides the bootstrap voltage to the high-side gate driver of PWM5 for driving the N-channel MOSFET. An external capacitor connected from PHASE5 to BOOT5 is required for the high-side gate driver.
20	17	UGATE5	High-side Gate Driver Output of PWM5. This pin is connected to high-side MOSFET.

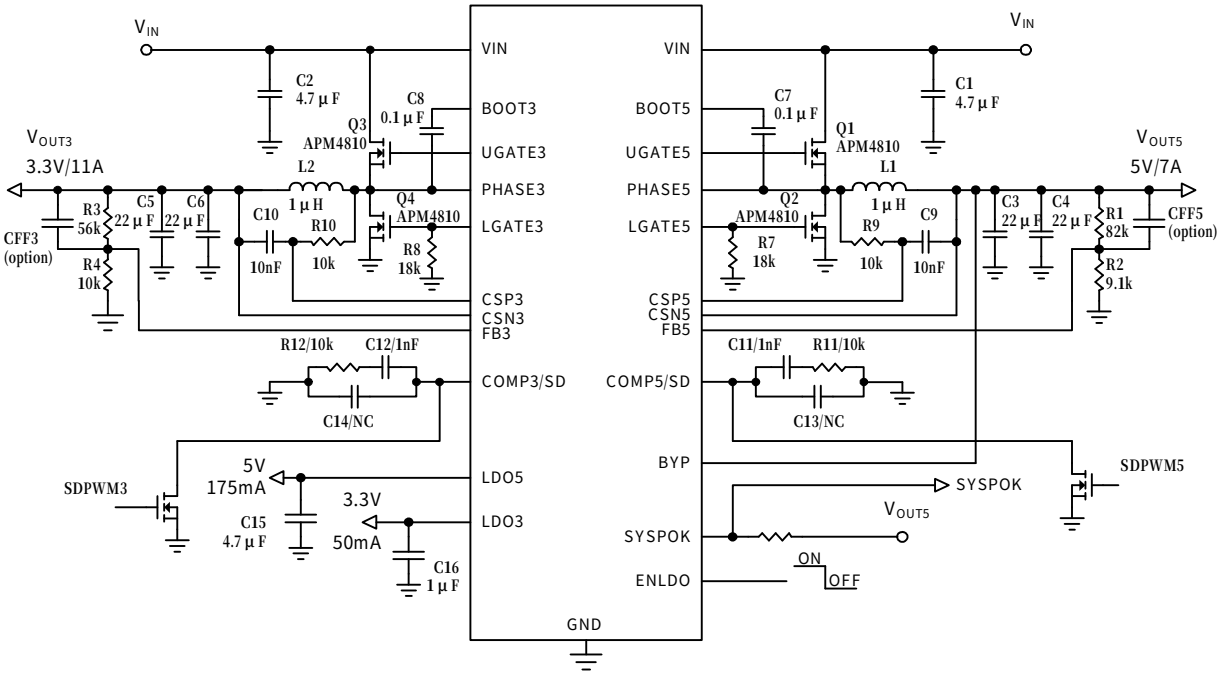
Pin Description (Cont.)

PIN			Function
TQFN4x4-24	QFN3x3-20	NAME	
21	18	PHASE5	This pin is the return path for the high-side gate driver of PWM5. Connecting this pin to the high-side MOSFET source and connecting a capacitor to BOOT5 for the bootstrap voltage.
22	19	SYSPOK	PWM5 and PWM3 Power Good Output Indicator. This pin used to indicate the status of the PWM5 and PWM3. If an fault even detected on FB5, this pin represents a 100Ω resistance. If an fault even detected on FB3, this pin represents a 45Ω resistance. Once the V_{FB5} and V_{FB3} exceed 90% of reference voltage and operate normally, this pin represents high impedance.
23	-	BYP	Bypass this pin to LDO5. Once V_{BYP} exceeds 4.68V, an internal switch connects BYP to LDO5. Connecting this pin to output of PWM5.
24	20	CSN5	Negative Input of current sensing amplifier for PWM5. This pin combined with CSP5 senses the inductor current through an RC network.
Exposed Pad	Exposed Pad	GND	Signal and Power Ground.

Block Diagram



Typical Application Circuit



Function Description

The APW8820 integrate 2 PWM controllers and two LDO with 175mA source capability.

PWMx Control Loop

The APW8820 is a constant frequency, synchronous rectifier and current-mode switching controllers. In normal operation, the high side power MOSFET is turned on each cycle. The peak inductor current at which ICMPx turn off the high side MOSFET is controlled by the voltage on the COMPx node, which is the output of the error amplifier (EAMPx). An external resistive divider connected between V_{OUTx} and ground allows the EAMPx to receive an output feedback voltage V_{FBx} at FBx pin. When the load current increases, it causes a slightly decrease in V_{FBx} relative to the reference voltage (0.5V typical), which in turn causes the COMPx voltage to increase until the average inductor current matches the new load current.

Power-On-Reset

A Power-On-Reset (POR) function is designed to prevent wrong logic controls. The POR function continually monitors the supply voltage on the VIN pin. When the VIN voltage starts to establish, the internal LDO5 and LDO3 voltage start to rise.

Soft-Start

The APW8820 has a built-in digital soft-start to control the output voltage rise and limit the current surge at the start-up. During soft-start, an internal ramp connected to the one of the positive inputs of the gm amplifier rises up to replace the reference voltage (0.5V) until the ramp voltage reaches the reference voltage. The soft-start interval is about 1ms typical, independent of the converter¡¦s input and output voltages.

Soft-Stop

The APW8820 integrated a soft-stop circuitry in the event of PWM under-voltage or shutdown. The soft-stop function discharges the PWM output voltages (V_{OUTx}) from CSNx to the GND through an internal 20Ω switch. The reference remains active to provide an accurate threshold and over-voltage protection.

PSM/PWM

At light loads, the inductor current may reach zero or reverse on each pulse. The bottom MOSFET is turned off by the current reversal comparator, the switch voltage will ring. This is discontinuous mode operation, and is normal behavior for the switching regulator. At very light loads, the APW8820 will automatically skip pulses in pulse skipping mode operation to maintain output regulation.

Ultrasonic Mode

The APW8820 integrated ultrasonic mode. The ultrasonic mode activates an unique PFM mode with a minimum switching frequency of 25kHz. The minimum frequency 25kHz of ultrasonic mode eliminates audio-frequency interference in light load condition. It will transit to unique PFM mode when output loading makes the frequency exceed ultrasonic frequency. When the controller detects that no switching has occurred within about 40ms (typical), an ultrasonic pulse will be occurred. The ultrasonic controller turns on the lowside MOSFET firstly to reduce the output voltage. After the COMPx voltage exceed 0.45V, the controller turns off lowside MOSFETs and turns high-side MOSFETs on. When the inductor current rise in which COMPx exceed 0.45V, the controller turns on the low-side MOSFET again until the inductor current is below the zero-crossing threshold. The behavior is the same as PFM mode.

Enable/Shutdown

The APW8820 integrate individual control input pin for both converters. Pulling COMPx/SD low ($V_{DISABLE}$=0.4V) will shut down the represent controller. When the pull-down device is released, the COMPx/SD pin will start to rise. When the COMPx/SD pin rises above the $V_{DISABLE}$ trip point, the APW8820 will begin a new initialization and soft-start cycle.

Power Good Indicator

The SYSPOK is used to indicate the status of the PWM5 and PWM3. If an Fault even detected on FB5, this pin represents a 100Ω resistance. If an fault even detected on FB3, this pin represents a 60Ω resistance.

The fault even includes FBx over-voltage, FBx under-voltage, inductor over-current sense at CSP5/3 and CSN5/3. When the V_{FB5} and V_{FB3} exceed 90% of reference voltage and operate normally, this pin represents high impedance.

Function Description (Cont.)

Adaptive Shoot-Through Protection

The gate driver incorporates adaptive shoot-through protection to high-side and low-side MOSFETs from conducting simultaneously and shorting the input supply. This is accomplished by ensuring the falling gate has turned off one MOSFET before the other is allowed to rise.

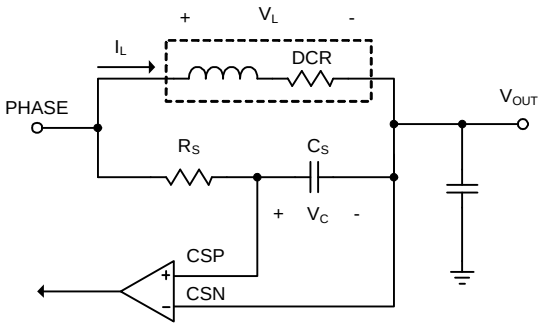
During turn-off the low-side MOSFET, the internal LGATE voltage is monitored until it below 1.5V threshold, at which time the UGATE is released to rise after a constant delay. During turn-off the high-side MOSFET, the UGATE voltage is also monitored until it above 1.5V threshold, at which time the LGATE is released to rise after a constant delay.

Over-Temperature Protection (OTP)

When the junction temperature exceed the threshold temperature 160oC (typical), the device enter the over temperature protection (OTP). When the OTP occurs, the APW8820 shut off 2 channels of regulators' circuitry with a latch. The APW8820 will initiate a soft-start process until re-cycle power supply or both the control input (COMPx/SD).

Over-Temperature Protection (OTP)

Below shows the circuit of sensing inductor current. Connecting a series resistor (R_S) and a capacitor (C_S) network in parallel with the inductor and measuring the voltage (V_C) across the capacitor can sense the inductor current.



The equations of the sensing network are:

$$V_L(s) = I_L(s) \times (sL + DCR)$$

$$V_C(s) = V_L(s) \times \frac{1}{1 + sR_SC_S} = \frac{I_L(s) \times (sL + DCR)}{1 + sR_SC_S}$$

Take

$$R_SC_S = \frac{L}{DCR}$$

If the above is true, the voltage across the capacitor C_S is equal to voltage drop across the inductor DCR, and the voltage VC is proportional to the inductor current I_L.

$$V_C = DCR \times I_L$$

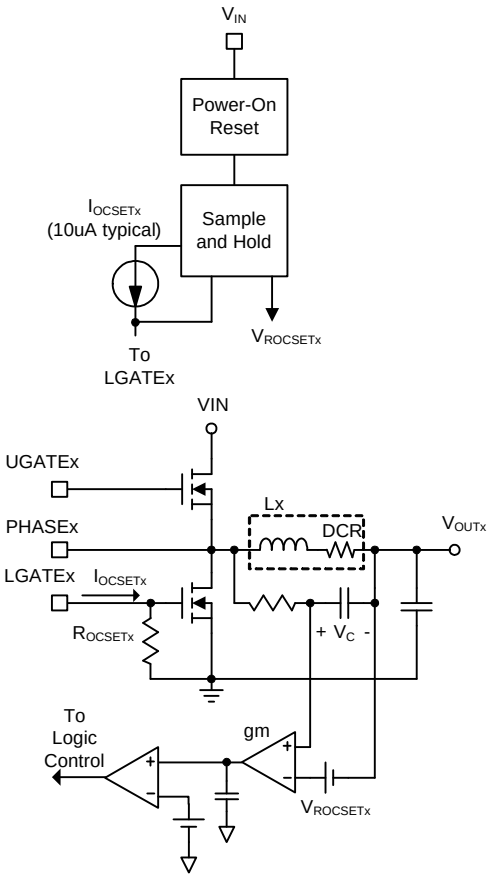
Where
I_L is the inductor current
DCR is the inductor resistance

Inductor Current Sense and Over-Circuit Protection

The over-current function protects the switching converter against over-current or short-circuit conditions. The controller senses the inductor current by detecting the drain to-source voltage which is the product of the inductor's current and the on-resistance of the low-side MOSFET during it's on-state. A resistor (R_{OCSETx}), connected from the LGATEx to the GND, programs the over-current trip level. Before the IC initiates soft-start process, an internal current source, I_{OCSETx} (5mA typical), flowing through the R_{OCSETx} develops a voltage ($V_{ROCSETx}$) across the R_{OCSETx}. The device holds $V_{ROCSETx}$ and stops the current source, I_{OCSETx}. The APW8820 initial soft-start process after over-current setting completed. Once the voltage across the low-side MOSFET exceeds the V_{ROCSET}, the IC shuts off the converter. Both the output of the PWMx converter are latched. The threshold of the valley inductor current-limit is therefore given by:

$$I_{LIMIT} = \frac{I_{OCSETx} \times R_{OCSETx}}{DCR}$$

Function Description (Cont.)



For the over-current is never occurred in the normal operating load range; the variation of all parameters in the above equation should be considered:

The minimum IOCSET (9µA) and minimum R_{OCSETx} should be used in the above equation.

The overshoot and transient peak current also should be considered.

Due to the OCP sense the integrated VC, the OCP threshold equal to output current (I_{OUTx}) rather than peak or valley inductor current.

The APW8820 will initiate a soft-start process until re-cycle power supply or both the control input (COMPx/SD).

Under Voltage Protection

In the operational process, if short-circuit occurs, the output voltage will drop quickly. When load current increased, the output voltage will falls out of the required regulation range. The under-voltage circuitry continually monitors the setting output voltage after soft-start is completed. If a load step is strong enough to pull the output voltage lower than the under-voltage threshold, the PWM controller starts a soft-stop process to shut down the output gradually. If any channel triggers under-voltage, both under-voltage protection circuits active and latched off when the soft-stop process is completed. The under-voltage threshold is 70% of the nominal output voltage. The APW8820 will initiate a soft-start process until re-cycle power supply or both the control input (COMPx/SD).

Output Over-Voltage Protection

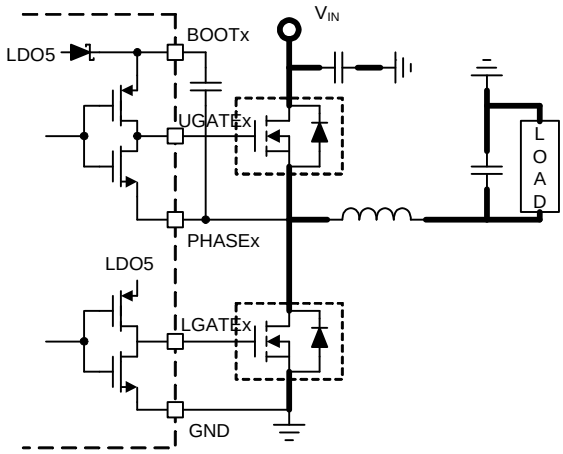
The over-voltage protection circuitry monitors the FB5 and FB3 voltage to prevent the output from over-voltage. Once the feedback voltage, FB5 and FB3, exceed 120% of reference voltage, the APW8820 turns on the low-side MOSFET until the output voltage falls below 5% of normal. When the output voltage falls below 5% of normal, all the channels converter are shut off. The UGATEx and LGATEx are pulled low. The APW8820 will initiate a soft-start process until re-cycle power supply or both the control input (COMPx/SD).

Application Information

Layout Consideration

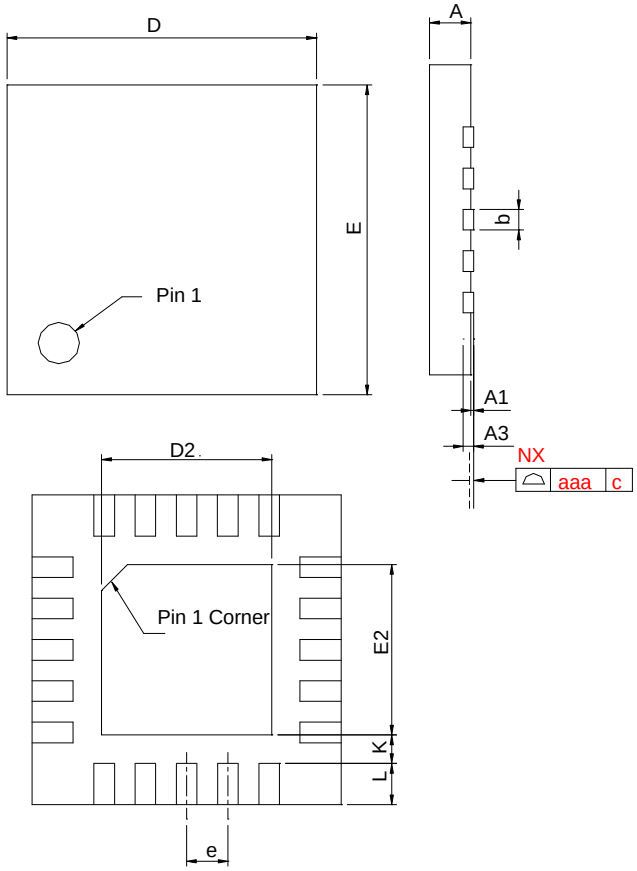
In any high switching frequency converter, a correct layout is important to ensure proper operation of the regulator. With power devices switching at 1000kHz, the resulting current transient will cause voltage spike across the interconnecting impedance and parasitic circuit elements. As an example, consider the turn-off transition of the PWM MOSFET. Before turn-off, the MOSFET is carrying the full load current. During turn-off, current stops flowing in the MOSFET and is free-wheeling by the lower MOSFET and parasitic diode. Any parasitic inductance of the circuit generates a large voltage spike during the switching interval. In general, using short and wide printed circuit traces should minimize interconnecting impedances and the magnitude of voltage spike. And signal and power grounds are to be kept separate till combined using ground plane construction or single point grounding. Below illustrates the layout, with bold lines indicating high current paths; these traces must be short and wide. Components along the bold lines should be placed lose together. Below is a checklist for your layout:

- The gate driver trace should be as short as possible. CBOOTx which connected between BOOTx and PHASEx should closed to IC. Keep the switching nodes (UGATEx, LGATEx, and PHASEx) as short as possible.
- Keep the sensitive small nodes (FBx, CSPx, CSNx, COMPx) away from the switching nodes (UGATEx, LGATEx, and PHASEx).
- Place the source of the high-side MOSFET and the drain of the low-side MOSFET as close as possible. Minimizing the impedance with wide layout plane between the two pads reduces the voltage bounce of the node.
- Decoupling capacitor, compensation component, the resistor dividers, and boot capacitors should be close their pins. (For example, place the decoupling ceramic capacitor near the drain of the high-side MOSFET as close as possible. The bulk capacitors are also placed near the drain).
- The input capacitor should be near the drain of the upper MOSFET; the output capacitor should be near the loads. The input capacitor GND should be close to the output capacitor GND and the lower MOSFET GND.
- The drain of the MOSFETs (VIN and PHASE nodes) should be a large plane for heat sinking.



Package Information

QFN3x3-20

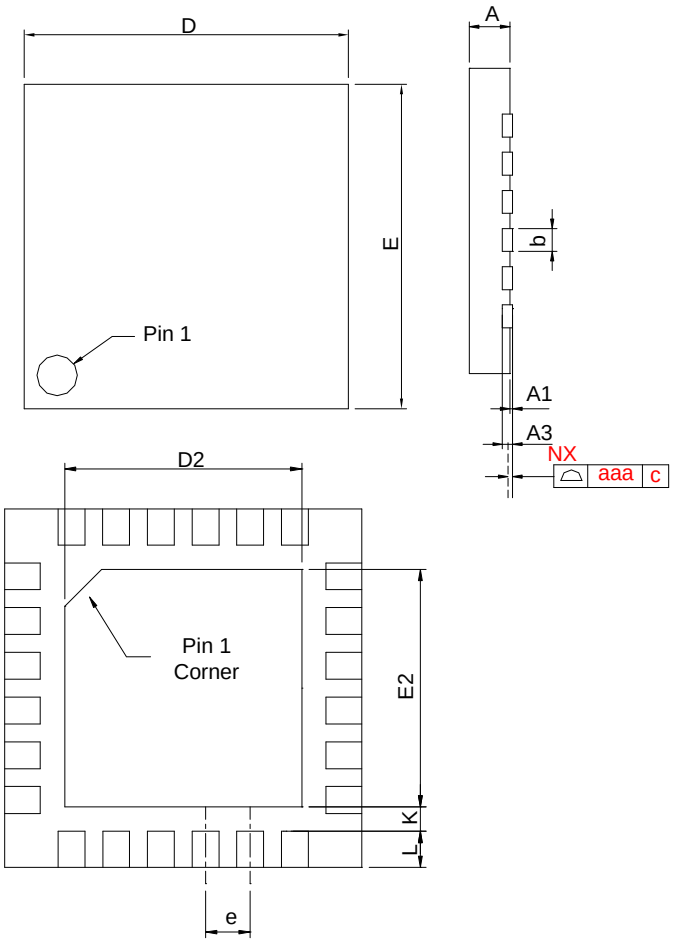


SYMBOL	QFN3x3-20			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.15	0.25	0.006	0.010
D	2.90	3.10	0.114	0.122
D2	1.50	1.80	0.059	0.071
E	2.90	3.10	0.114	0.122
E2	1.50	1.80	0.059	0.071
e	0.40 BSC		0.016 BSC	
L	0.30	0.50	0.012	0.020
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Followed from JEDEC MO-220 WEEE

Package Information

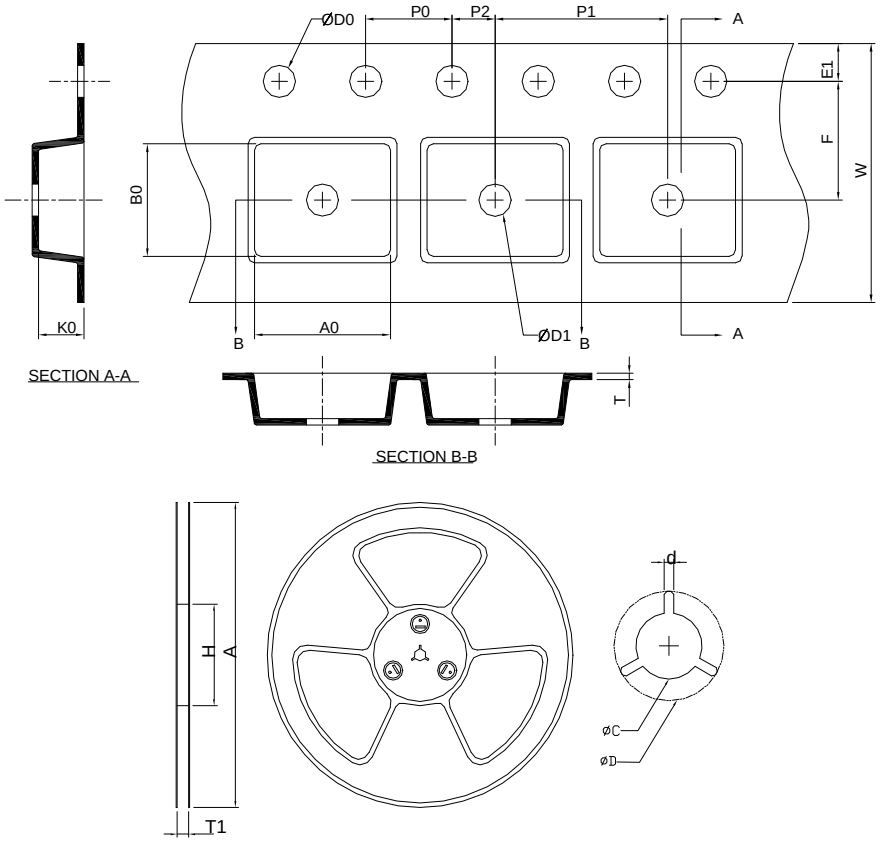
QFN4x4-24



SYMBOL	TQFN4x4-24			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	0.70	0.80	0.028	0.032
A1	0.00	0.05	0.000	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.008	0.012
D	3.90	4.10	0.154	0.161
D2	2.50	2.80	0.098	0.110
E	3.90	4.10	0.154	0.161
E2	2.50	2.80	0.098	0.110
e	0.50 BSC		0.020 BSC	
L	0.35	0.45	0.014	0.018
K	0.20		0.008	
aaa	0.08		0.003	

Note : 1. Doll owed from JEDFC MO-220 WGGD-6

Carrier Tape & Reel Dimensions



Application	A	H	T1	C	d	D	W	E1	F
QFN3X3-20	330±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	3.30±0.20	3.30±0.20	1.30±0.20
TQFN4x4-24	**A**	**H**	**T1**	**C**	**d**	**D**	**W**	**E1**	**F**
	330.0±2.00	50 MIN.	12.4+2.00 -0.00	13.0+0.50 -0.20	1.5 MIN.	20.2 MIN.	12.0±0.30	1.75±0.10	5.5±0.05
	P0	**P1**	**P2**	**D0**	**D1**	**T**	**A0**	**B0**	**K0**
	4.0±0.10	8.0±0.10	2.0±0.05	1.5+0.10 -0.00	1.5 MIN.	0.6+0.00 -0.40	4.30±0.20	4.30±0.20	1.30±0.20

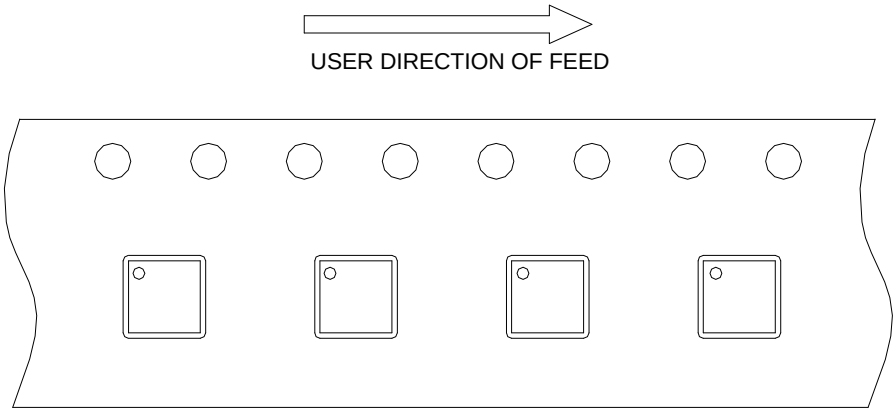
(mm)

Devices Per Unit

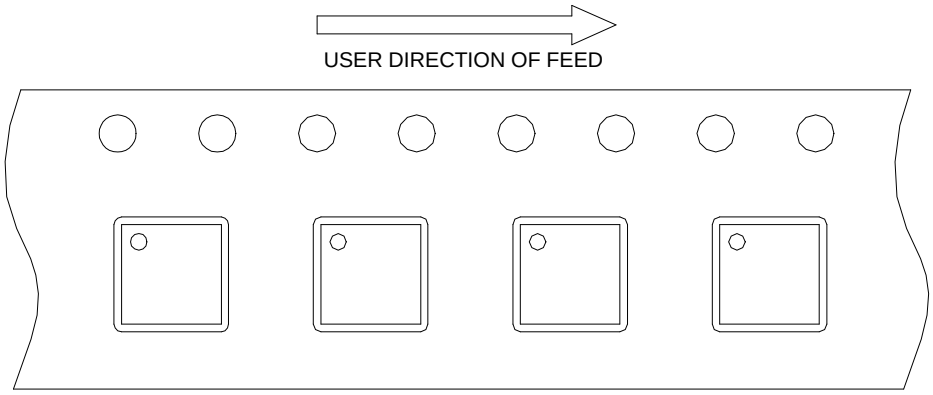
Package Type	Unit	Quantity
QFN3x3-20	Tape & Reel	3000
TQFN4x4-24	Tape & Reel	3000

Taping Direction Information

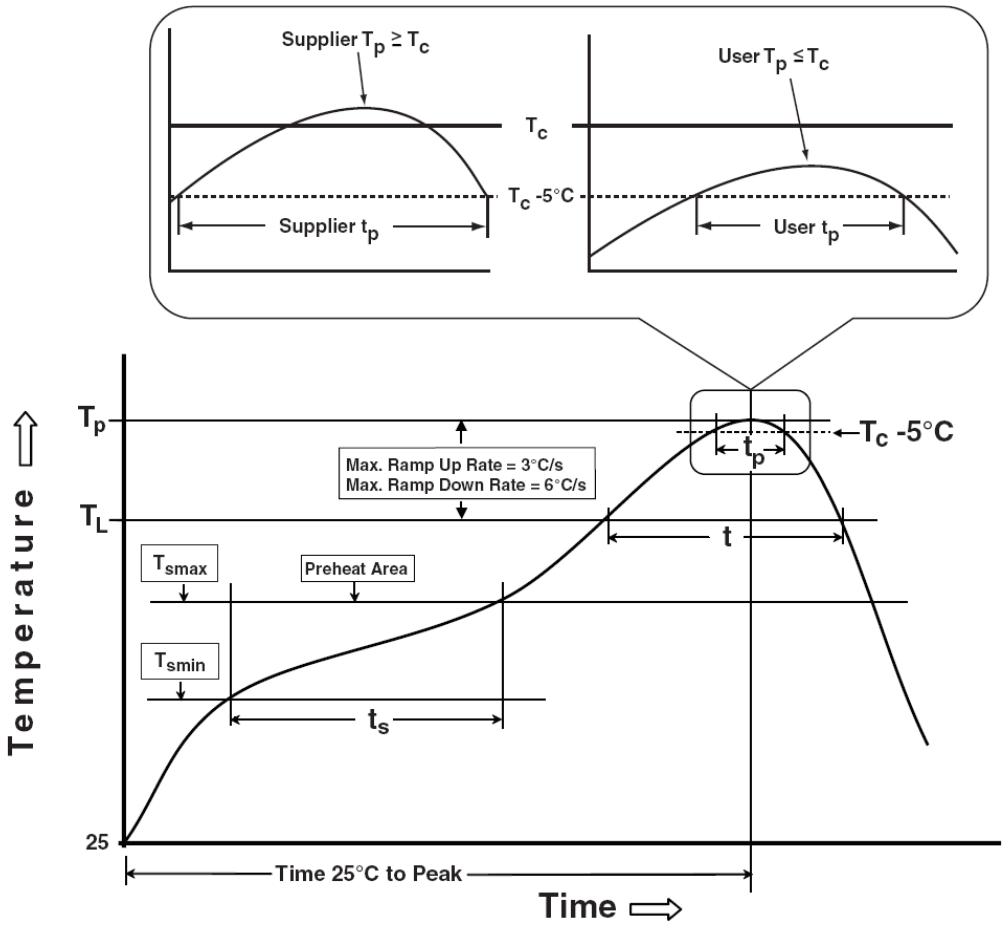
QFN3x3-20



TQFN4x4-24



Classification Profile



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Preheat & Soak Temperature min (T_{smin}) Temperature max (T_{smax}) Time (T_{smin} to T_{smax}) (t_s)	100 °C 150 °C 60-120 seconds	150 °C 200 °C 60-120 seconds
Average ramp-up rate (T_{smax} to T_P)	3 °C/second max.	3°C/second max.
Liquidous temperature (T_L) Time at liquidous (t_L)	183 °C 60-150 seconds	217 °C 60-150 seconds
Peak package body Temperature (T_p)*	See Classification Temp in table 1	See Classification Temp in table 2
Time (t_P)** within 5°C of the specified classification temperature (T_c)	20** seconds	30** seconds
Average ramp-down rate (T_p to T_{smax})	6 °C/second max.	6 °C/second max.
Time 25°C to peak temperature	6 minutes max.	8 minutes max.
* Tolerance for peak profile Temperature (T_p) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.		

Table 1. SnPb Eutectic Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	235 °C	220 °C
≥2.5 mm	220 °C	220 °C

Table 2. Pb-free Process – Classification Temperatures (Tc)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm – 2.5 mm	260 °C	250 °C	245 °C
≥2.5 mm	250 °C	245 °C	245 °C

Reliability Test Program

Test item	Method	Description
SOLDERABILITY	JESD-22, B102	5 Sec, 245°C
HOLT	JESD-22, A108	1000 Hrs, Bias @ T_j=125°C
PCT	JESD-22, A102	168 Hrs, 100%RH, 2atm, 121°C
TCT	JESD-22, A104	500 Cycles, -65°C~150°C
HBM	MIL-STD-883-3015.7	VHBM≧2KV
MM	JESD-22, A115	VMM≧200V
Latch-Up	JESD 78	10ms, 1_{tr}≧100mA

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