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CX02048

Low Power 3.3 Volt Limiting Amplifier For Data Rates to 3.3 Gbps

Data Sheet

- Features
- Description
- Applications
- Pin Descriptions
- Measurement Tables
- Functional Description

Applications Information

Please use this data sheet in conjunction with the technical information:

CX02048 Product Bulletin:	02048-PBD-001-B
CX02048 Application Note:	Note 0019 Rev 01
BCC Package Application Note:	AN0004 Rev 01
Bare Die Application Note:	Note 0024 Rev 02

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Low Power 3.3 Volt Limiting Amplifier for Data Rates to 3.3 Gbps

FEATURES

- Wide dynamic range with 5 mV input sensitivity at 3.3 Gbps
- Programmable input signal level detect
- Fully differential
- CML data outputs with default <80 ps rise and fall time
- Temperature range 0 to +85°C
- Operates with +3.3 V supply
- Supply current typically 26 mA
- Programmable output amplitude (default 400 mVpp differential)
- On-chip DC offset cancellation circuit; no external capacitors needed

APPLICATIONS

- 3.3 Gbps SDH/SONET with FEC
- 2.5 Gbps STM-16/OC-48 SDH/SONET
- 2.12 Gbps Fibre Channel

DESCRIPTION

The CX02048 is an integrated high-gain limiting amplifier intended for high-speed fiber optics based communications. Placed following the photodetector and transimpedance amplifier, the limiting amplifier provides the necessary gain to ensure full CML output swing even at minimum input sensitivity.

Capable of operating over a very wide frequency range, the CX02048 supports data rates up to 3.3 Gbps.

The CX02048 also includes a programmable signal level detector, allowing the user to set the threshold at which the status logic outputs are enabled.

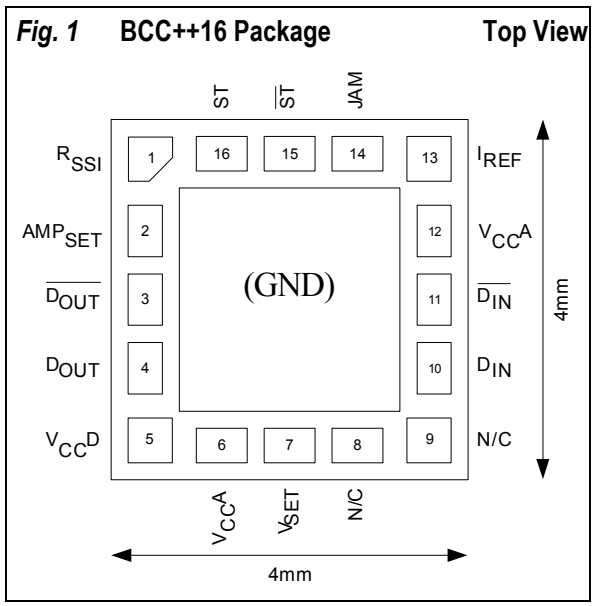
TABLE 1 ORDERING INFORMATION

Part Number	Pin Package
CX02048DIEWP	Waffle Packed Die
CX02048WAFER	Expanded whole wafer on a Grip ring
CX02048B16	BCC++16
CX02048B16TR	BCC++16 Tape and Reel
M02048-EVM	Evaluation board

Please see application note CX02048-Note 0019.

CONNECTIONS

Fig. 1 **BCC++16 Package** **Top View**



TOP LEVEL DIAGRAM

Fig. 2

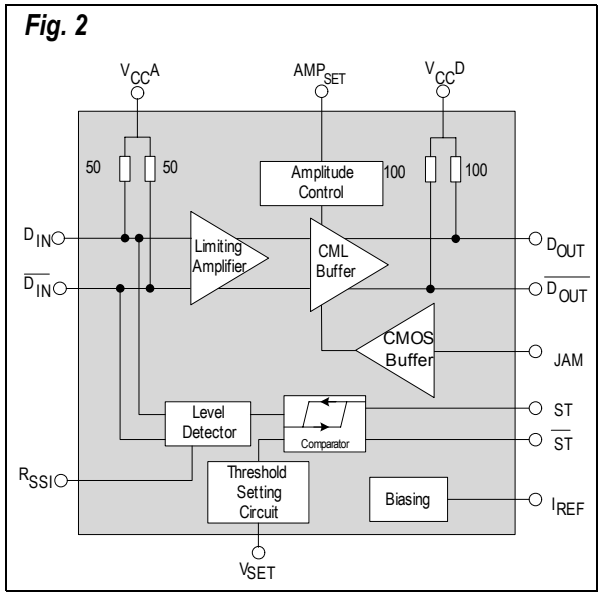


TABLE 2 PIN DESCRIPTIONS

Die Pads	BCC++16	Name	Function
23	1	R_{SSI}	Receiver signal strength indication. Connect to ground with a 4.7 nF capacitor (referenced to V_{CC})
1	2	AMP_{SET}	Enables setting of output voltage swing from 400 mV pp differential to 800 mV pp differential using an external 1% resistor (R_{AMPSET} to ground)
2	-	GNDD	Digital ground
3	-	GNDD	Digital ground
4	3	$\overline{D_{OUT}}$	Inverting differential data output
5	4	D_{OUT}	Non-inverting differential data output
6	-	GNDD	Digital ground
7	5	$V_{CC}D$	Digital positive supply
8	6	$V_{CC}A$	Analog positive supply
9	-	GNDA	Analog ground
10	7	V_{SET}	Signal detect threshold setting input. User programmed with 1% resistor (R_{SET}) to V_{CC}
11	-	GNDA	Analog ground
-	8	NC	Not connected
-	9	NC	Not connected
12	10	D_{IN}	Non-inverting data input
13	11	$\overline{D_{IN}}$	Inverting data input
14	-	GNDA	Analog ground
15	-	GNDA	Analog ground
16	12	$V_{CC}A$	Analog positive supply
17	13	I_{REF}	This pin generates an on-chip reference current, and must be connected via an external 1% resistor (R_{REF}) to ground
18	-	GNDA	Analog ground
19	14	JAM	When HIGH data outputs D_{OUT} and $\overline{D_{OUT}}$ are disabled (D_{OUT} being held LOW and $\overline{D_{OUT}}$ being held HIGH)
20	15	$\overline{ST}$	Logical inverse of ST pin. May be connected to JAM pin to enable automatic jam function on output. This is an open drain output with an internal 100K Ω pull-up
21	16	ST	Input signal level status. This output is low when the input signal is below the set threshold. This is an open drain output with an internal 100K Ω pull-up
22	-	GNDA	Analog ground
-	Center	GND	Ground. Connect via die-plate

TABLE 3 ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Units
Power supply voltage (V_{CC}-GND)	-0.5 to +6V	V
Operating ambient temperature	0 to +85	°C
Storage temperature	-65 to +150	°C

These are the absolute maximum ratings at or beyond which the IC can be expected to fail or be damaged. Reliable operation at these extremes for any length of time is not implied.

Note: The die-plate must be adequately grounded to ensure correct thermal and electrical performance, and it is recommended that vias are inserted through to a lower ground plane.

TABLE 4 RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Units
Power supply (V_{CC}-GND)	3.3 ± 10%	V
Junction temperature	0 to +110	°C
Operating ambient	0 to +85	°C

TABLE 5 DC CHARACTERISTICS

(V_{CC} = +3.3 V + 10%, T_A = 0 °C to +85 °C, unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply current (I_{CC})	AC-coupled 50 Ω load 400 mVpp differential output amplitude	-	26	33	mA
	800 mV p-p differential output amplitude	-	32.5	41	mA
CML outputs LOW	R_{AMPSET} = 0 Ω (Note 1), Output load AC- or DC-coupled 50 Ω to V_{CC} single ended	V_{CC} -0.21	V_{CC} -0.2	V_{CC} -0.19	V
CML outputs HIGH	R_{AMPSET} = 0 Ω (Note 1), Output load AC- or DC-coupled 50 Ω to V_{CC} single ended	V_{CC} -0.02		V_{CC}	V
CML outputs LOW	R_{AMPSET} = 820 Ω (Note 1), Output load DC-coupled 50 Ω to V_{CC} single ended	V_{CC} -0.42	V_{CC} -0.4	V_{CC} -0.38	V
CML outputs HIGH	R_{AMPSET} = 820 Ω (Note 1), Output load DC-coupled 50 Ω to V_{CC} single ended	V_{CC} -0.04		V_{CC}	V
Data input differential input resistance	(2 x 50 Ω to V_{CC} internally)	85	100	115	Ω
Data output differential output impedance	(2 x 100 Ω to V_{CC} internally)	170	200	230	Ω
Status output HIGH voltage	10 kΩ pull up resistor	V_{CC} -0.1			V
Status output LOW voltage	10 kΩ pull up resistor			100	mV
JAM input HIGH voltage		1.33			V
JAM input LOW voltage				1.1	V
Status output sink current		1.5	-	-	V

Note 1: The maximum single-ended output value when AC-coupled into a 50 Ω load is 200 mVpp (R_{AMPSET} = 0 Ω). When connected as shown in Fig. 3, the maximum AC-coupled output value is 300 mVpp (R_{AMPSET} = 820 Ω). When DC coupled, the maximum single-ended output is 400 mVpp. For more information, please refer to Product Bulletin 02048-PBD-001-B.

TABLE 6 AC CHARACTERISTIC

(V_{CC} = +3.3 V + 10%, T_A = 0 °C to +85 °C, unless otherwise specified)

Parameter	Conditions	Min.	Typ.	Max.	Units
Input Sensitivity	For BER <10^{-10}, differential input	-	3.5	5	mVpp
Input Overload	For BER <10^{-10}, differential input	1200	-	-	mVpp
Signal detect programmable range	Differential inputs (Note 3)	10	-	200	mVpp
Assert and deassert reaction time	C_{RSSI} = 4.7 nF	2.3		10	µs
Signal detect hysteresis (electrical)	Signal detect level set to assert level of 15 mVpp (Note 1)	2.0	4.5	6.0	dB
Small signal -3dB low frequency cut-off	Excluding AC-coupling capacitors			20	kHz
Pulse width distortion	Alternating 1-0 pattern at 622 Mbps			20	ps
tr, tf	400 mV pp differential output amplitude, ($RAMP_{SET}$ = 0 Ω) (Note 2)		65	80	ps
	800 mV pp differential output amplitude, ($RAMP_{SET}$ = 820 Ω) (Note 2)		85	100	ps

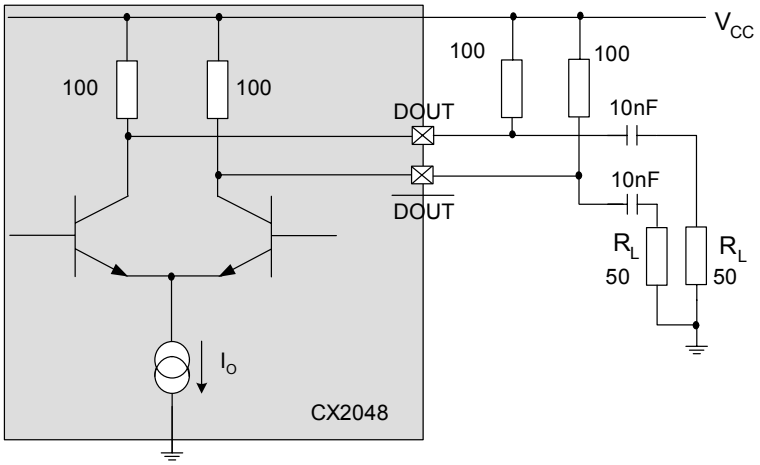
Note 1: Hysteresis of 4.5dB Electrical, corresponds to 2.25dB Optical hysteresis.

Note 2: The rise and fall times are defined as 20% to 80% of each output. The output is AC-coupled into 50 Ω to ground.

Note 3: Refers to assert level (asserted when ST switches from logic 0 to logic 1).

OUTPUT CONNECTION FOR MAXIMUM AC-COUPLED OUTPUT AMPLITUDE OF 300MVPP SE

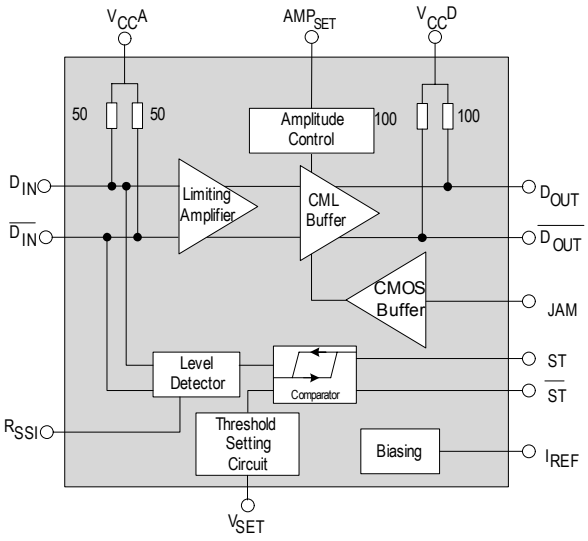
Fig. 3



Low Power 3.3 Volt Limiting Amplifier for Data Rates to 3.3 Gbps

FUNCTIONAL BLOCK DIAGRAM

Fig. 4



FUNCTIONAL DESCRIPTION

Overview

The CX02048 is a high-gain limiting amplifier for applications up to 3.3 Gbps and incorporates a limiting amplifier, a CML buffer, and an input signal level detection circuit. The CX02048 also features a fully integrated DC-offset cancellation loop that does not require any external components.

The user is provided with the flexibility to set the data output amplitude levels and the signal detect level.

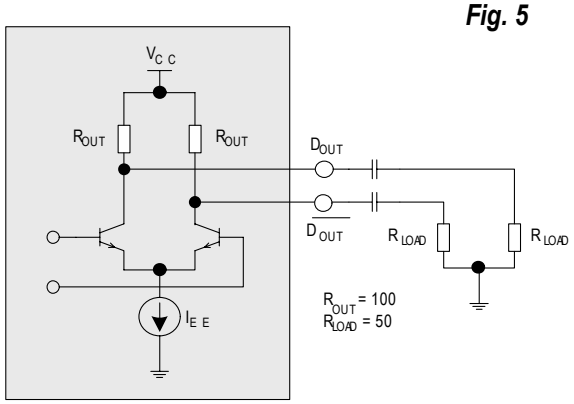
Inputs

The data inputs are internally biased to V_{CC} via 50 Ω resistors and may be AC or DC-coupled. Note that if the inputs are AC-coupled, the coupling capacitor should be of sufficient value to pass the lowest frequencies of interest, bearing in mind the number consecutive identical bits and the input resistance.

Outputs

The basic output configuration is as shown in Fig. 5. By controlling the value of I_{EE} via external resistor R_{AMPSET}, it is possible to set the output voltage swing linearly between 400 mVpp differential and 800 mVpp differential when terminated with the appropriate load. See the applications information for further details.

Fig. 5



DC Offset Compensation

Internal DC feedback requiring no external components is included to remove the effects of DC offsets and act as a DC auto-zero circuit. The circuit is configured such that the feedback is effective only at frequencies below the lowest frequency of interest. The low frequency cut off is less than 20 kHz.

Signal Level Detector

The CX02048 features input signal level detection over an extended range. Using an external resistor, (R_{SET}), between pin V_{SET} and V_{CC}, the user can program the input signal threshold level. The signal detect status is

FUNCTIONAL DESCRIPTION

indicated on the ST and $\overline{ST}$ open-drain output pins. The signal detection circuitry has the equivalent of 4.5 dB (typical) electrical hysteresis. The curve in Fig. 8 gives an indication of the typical value of R_{SET} required to set a given signal detect level. See the applications section for further details.

JAM Function

Signal level detection can be used to automatically force the data outputs to a known state when the input signal falls below the threshold. The function is normally used to allow data to propagate only when the signal is above the user's bit-error-rate requirement. It therefore inhibits the data outputs toggling due to noise when there is no signal present JAM.

In order to implement this function, $\overline{ST}$ should be connected to the JAM pin, thus forcing the data outputs to logical zero when the signal falls below the threshold.

Note that R_{SET} must be connected, even if the level detector function is not required.

Bias

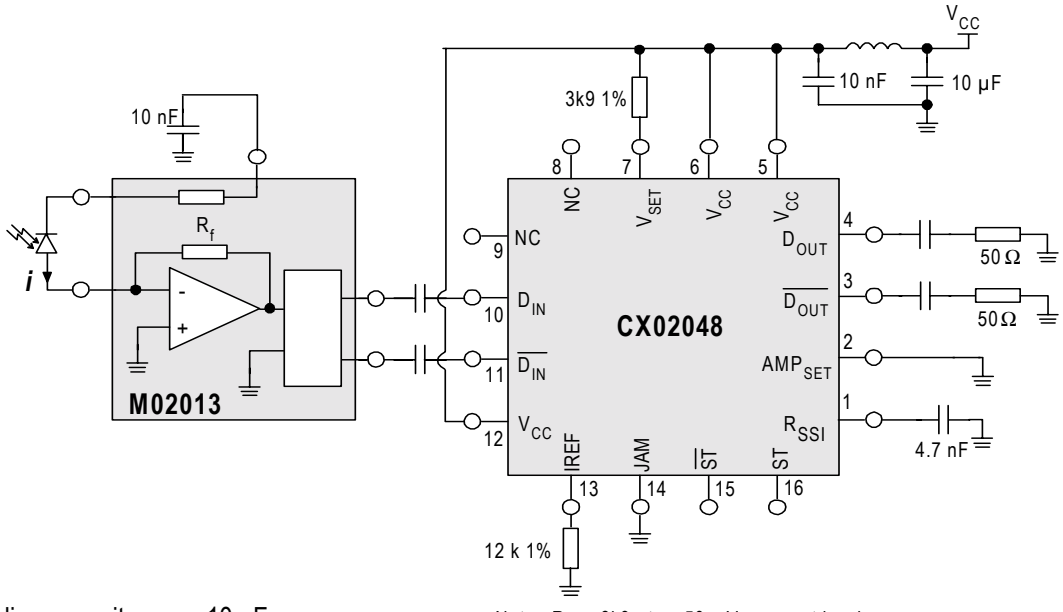
The CX02048 contains an accurate on-chip bias circuit requiring an external 12 kΩ 1% resistor, $R_{REF,}$ from pin I_{REF} to ground to define an on-chip reference current.

RSSI

The voltage at RSSI (with respect to V_{CC}) allows the user to monitor the input signal amplitude, see Fig. 9.

APPLICATIONS CIRCUIT (1) 400 MVPP-DIFF

Fig. 6



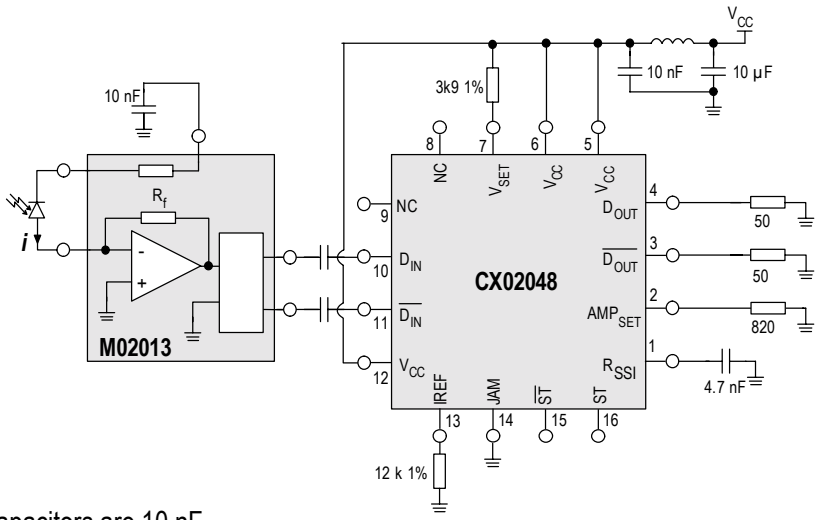
Note: Coupling capacitors are 10 nF

Note : R_{SET} 3k9 - typ. 50 mVpp assert level

Low Power 3.3 Volt Limiting Amplifier for Data Rates to 3.3 Gbps

APPLICATIONS CIRCUIT (2) 800 MVPP - DIFF (DC-COUPLED OUTPUT ONLY)

Fig. 7



Note: Coupling capacitors are 10 nF

Note : R_{SET} 3k9 - typ. 50 mVpp assert level

APPLICATIONS INFORMATION

Setting Output Swing Level

The output circuit is shown in Fig 5. It is basically a differential pair with a tail current of I_{EE}. The load of the differential pair is formed by the parallel combination of R_{OUT} and R_{LOAD} for high frequencies where the coupling capacitor can be considered as a short circuit (100 // 50 = 33.3 Ω). The power consumption in the output stage is given by EQ.1:

$$P = I_{EE} \times V_{CC} \quad \text{EQ.1}$$

The single-ended output voltage swing is given by EQ.2:

$$V_{SWING} = I_{EE} \times (R_{OUT} // R_{LOAD}) \quad \text{EQ.2}$$

So the power consumption and the voltage swing are related to each other. The required minimum voltage swing sets the I_{EE} and the I_{EE} determines the power consumption. The minimum voltage swing depends on the application. Therefore, CX02048 provides the user the flexibility to optimize the voltage swing and the power consumption in his own application by setting I_{EE} using an external resistor (R_{AMPSET}). To select the required swing, use the following simple equation (EQ.3):

$$I_{EE} = 6\ mA + (R_{AMPSET} \times 7.3 \times 10^{-3})\ mA \quad \text{EQ.3}$$

In default case, I_{EE} is at minimum and equal to 6 mA which can be set by just connecting AMP_{SET} pin to ground. So in this case, there is no external resistor needed (R_{AMPSET} = 0 Ω, short-circuit). The resulting voltage swing is 200 mVpp, single-ended (= 6 mA x 33.3 Ω). This is sufficient for most of the applications. If needed the voltage swing can be increased at the expense of the power consumption by connecting an external resistor R_{AMPSET} between AMP_{SET} and GND pins. The value of R_{AMPSET} can be calculated from EQ.3. A resistor of 820 Ω results in 12 mA tail current (EQ.3) which delivers a voltage swing of 400 mVpp, single-ended (12 mA x 33.3 Ω). (Please see Note 1 under Table 5).

Setting Signal Detect Level

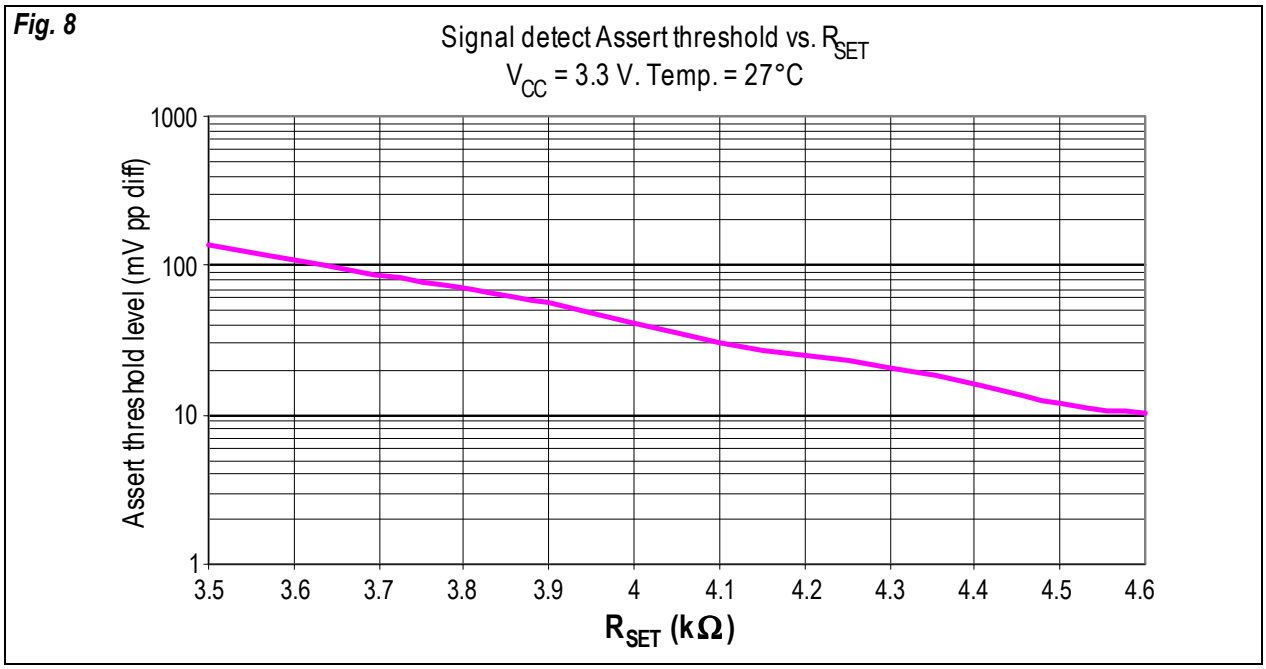
The CX02048 allows the user to set the required signal detect assert level using an external resistor (R_{SET}) to V_{CC}. To select the appropriate value, refer to Fig. 8. Three example values are given below:

TABLE 7 RESISTOR VALUES

VIN (mV pp) single-ended	R_{SET} (KΩ)
10	4.6
50	3.9
100	3.65

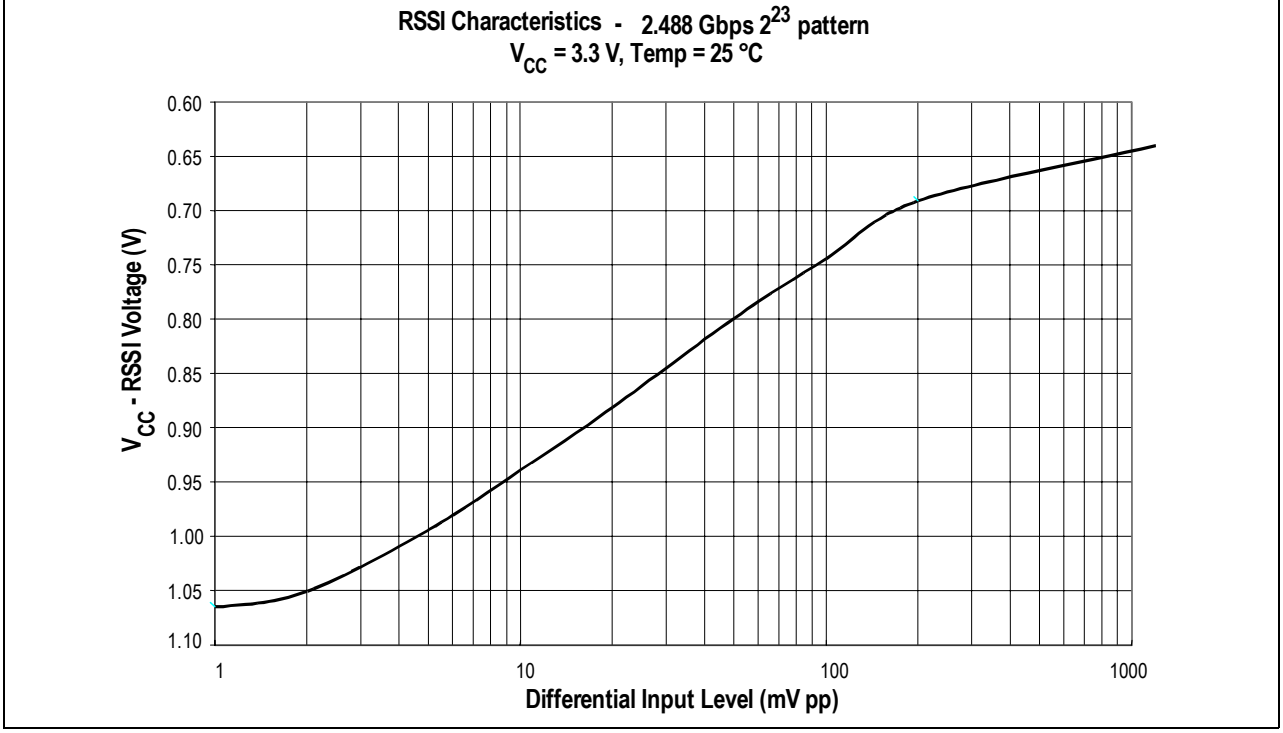
TYPICAL SIGNAL DETECT LEVEL

Fig. 8



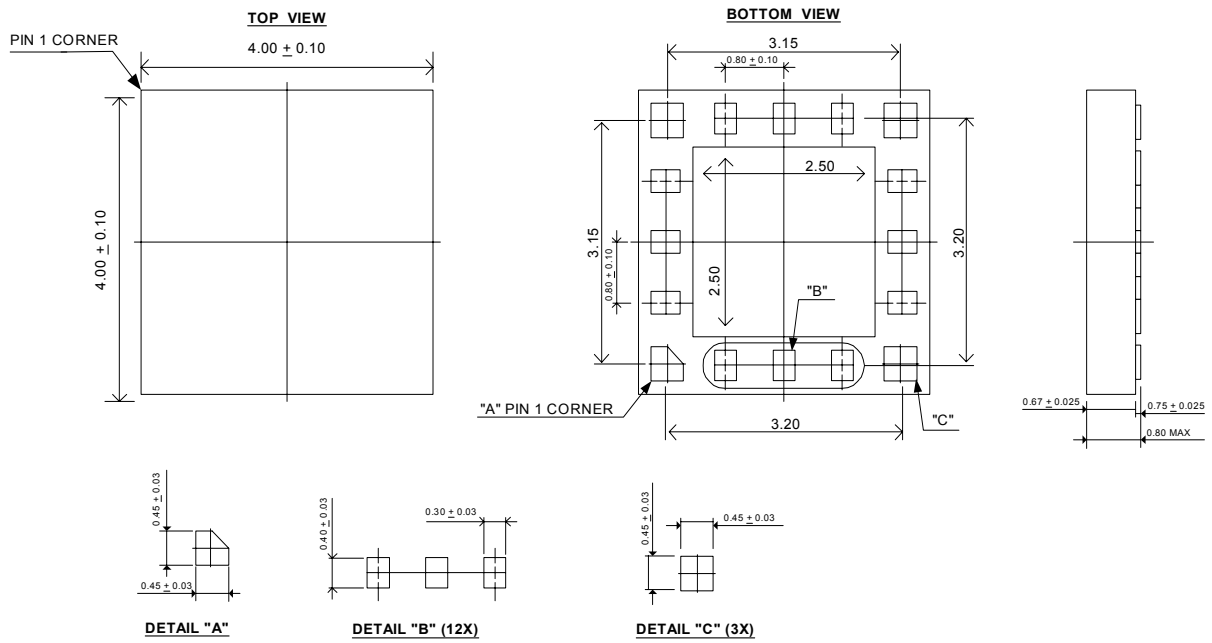
RSSI CHARACTERISTICS

Fig. 9



PACKAGE INFORMATION

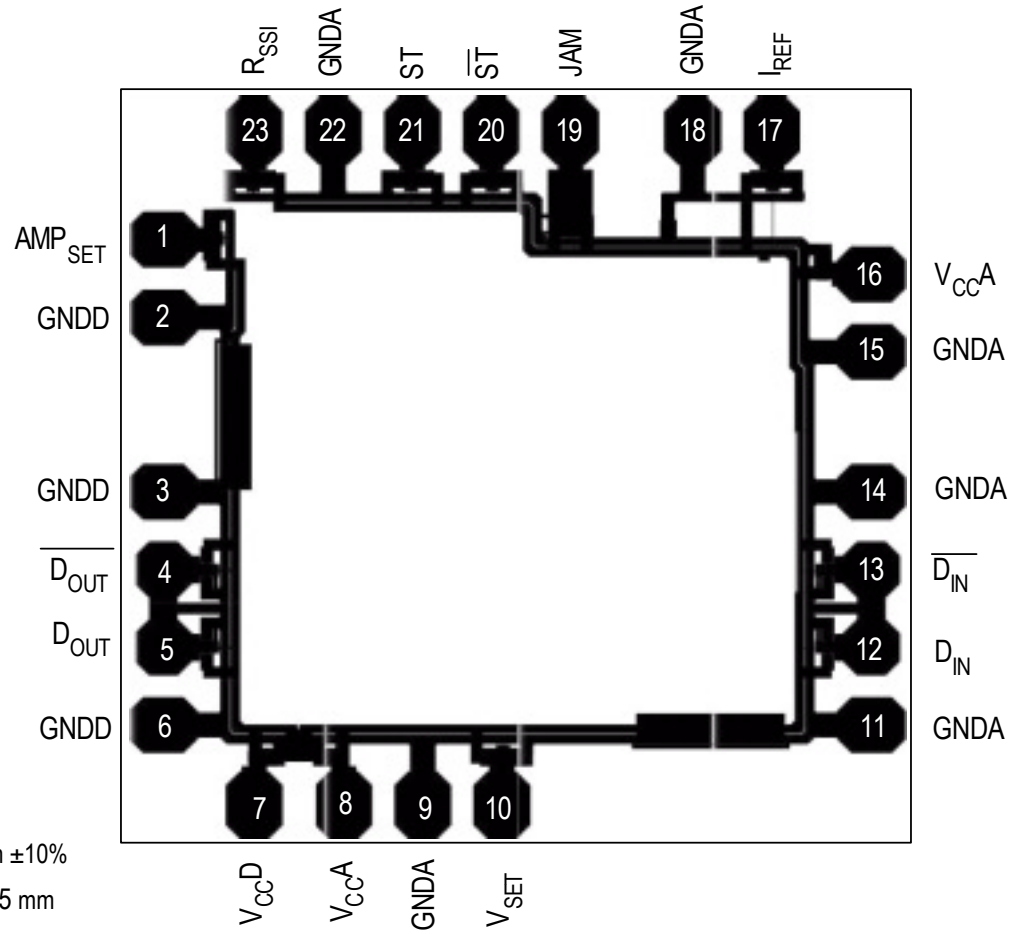
Fig. 10



Thermal performance <50 °C/W

BARE DIE

Fig. 11



Die thickness: 275 µm ±10%

Die size: 1.535 x 1.535 mm

TABLE 8 PAD CO-ORDINATES

Pad Reference	X (µm)	Y(µm)	Pad Reference	X (µm)	Y(µm)
AMP_{SET}	-591.274	418.987	$\overline{D_{IN}}$	662.726	-175.413
GNDD	-591.274	278.987	GNDA	662.726	-35.413
GNDD	-591.274	-35.413	GNDA	662.726	216.737
$\overline{D_{OUT}}$	-590.986	-175.413	$V_{CC}A$	662.726	356.737
D_{OUT}	-590.986	-315.413	I_{REF}	486.126	614.287
GNDD	-591.274	-455.413	GNDA	346.126	614.287
$V_{CC}D$	-430.224	-599.713	JAM	129.776	614.287
$V_{CC}A$	-271.824	-599.713	$\overline{ST}$	-10.224	614.287
GNDA	-131.824	-599.713	ST	-150.224	614.287
V_{SET}	8.176	-599.713	GNDA	-290.224	614.287
GNDA	662.726	-455.413	R_{SSI}	-430.224	614.287
D_{IN}	662.726	-315.413			

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Headquarters

Newport Beach
Mindspeed Technologies
4000 MacArthur Boulevard, East Tower
Newport Beach, CA 92660
Phone: (949) 579-3000
Fax: (949) 579-3020

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www.mindspeed.com