2.5V or 3.3V,10- 220 MHz, Low Jitter, 5 Output Zero Delay Buffer

Features

- **10 MHz to 220 MHz maximum operating range**
- **Zero input-output propagation delay, adjustable by loading on CLKOUT pin**
- **Multiple low-skew outputs**
  - **— 30 ps typical output-output skew**
  - **— One input drives five outputs**
- **22 ps typical cycle-to-cycle jitter**
- **13 ps typical period jitter**
- **Standard and High drive strength options**
- **Available in space-saving 150-mil SOIC package**
- **3.3V or 2.5V operation**
- **Industrial temperature available**

Functional Description

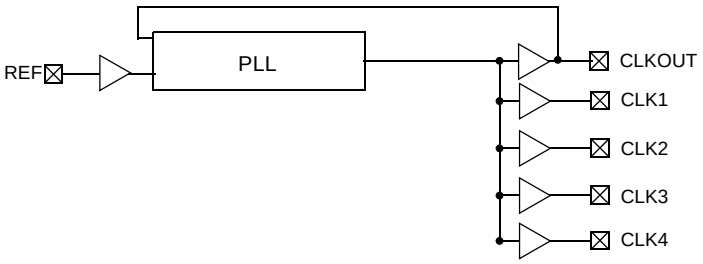
The CY23EP05 is a 2.5V or 3.3V zero delay buffer designed to distribute low-jitter high-speed clocks and is available in a 8-pin SOIC package. It accepts one reference input, and drives out five low-skew clocks. The -1H version operates up to 220 (200) MHz frequencies at 3.3V (2.5V), and has a higher drive strength than the -1 devices. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad.

The CY23EP05 PLL enters a power-down mode when there are no rising edges on the REF input (<~2 MHz). In this state, the outputs are three-stated and the PLL is turned off, resulting in less than 25 μA of current draw.

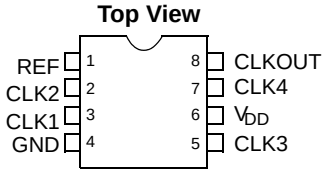
The CY23EP05 is available in different configurations, as shown in the Ordering Information table. The CY23EP05-1 is the base part. The CY23EP05-1H is the high-drive version of the -1, and its rise and fall times are much faster than the -1.

These parts are not intended for 5V input-tolerant applications

Block Diagram



Pin Configuration



Pin Description

Pin	Signal	Description
1	REF[1]	Input reference frequency
2	CLK2[2]	Buffered clock output
3	CLK1[2]	Buffered clock output
4	GND	Ground
5	CLK3[2]	Buffered clock output
6	V_{DD}	3.3V or 2.5V supply
7	CLK4[2]	Buffered clock output
8	CLKOUT[2,3]	Buffered clock output, internal feedback on this pin

Zero Delay and Skew Control

All outputs should be uniformly loaded to achieve Zero Delay between the input and output. Since the CLKOUT pin is the internal feedback to the PLL, its relative loading can adjust the input-output delay.

The output driving the CLKOUT pin will be driving a total load of 5 pF plus any additional load externally connected to this pin. For applications requiring zero input-output delay, the total load on each output pin (including CLKOUT) must be the same. If input-output delay adjustments are required, the CLKOUT load may be changed to vary the delay between the REF input and remaining outputs.

For zero output-output skew, be sure to load all outputs equally. For further information refer to the application note titled “CY2305 and CY2309 as PCI and SDRAM Buffers”.

Notes:
1. Weak pull-down.
2. Weak pull-down on all outputs.
3. This output is driven and has an internal feedback for the PLL. The load on this output can be adjusted to change the skew between the reference and output.

Absolute Maximum Conditions

Supply Voltage to Ground Potential ..... –0.5V to 4.6V
DC Input Voltage ..... V_{SS} – 0.5V to 4.6V
Storage Temperature ..... –65°C to 150°C
Junction Temperature ..... 150°C
Static Discharge Voltage
(per MIL-STD-883, Method 3015..... > 2000V

Operating Conditions

Parameter	Description	Min.	Max.	Unit
$V_{DD3.3}$	3.3V Supply Voltage	3.0	3.6	V
$V_{DD2.5}$	2.5V Supply Voltage	2.3	2.7	V
T_A	Operating Temperature (Ambient Temperature)—Commercial	0	70	°C
	Operating Temperature (Ambient Temperature)—Industrial	–40	85	°C
C_L[4]	Load Capacitance, <100 MHz, 3.3V	–	30	pF
	Load Capacitance, <100 MHz, 2.5V with High drive	–	30	pF
	Load Capacitance, <133.3 MHz, 3.3V	–	22	pF
	Load Capacitance, <133.3 MHz, 2.5V with High drive	–	22	pF
	Load Capacitance, <133.3 MHz, 2.5V with Standard drive	–	15	pF
	Load Capacitance, >133.3 MHz, 3.3V	–	15	pF
	Load Capacitance, >133.3 MHz, 2.5V with High drive	–	15	pF
C_{IN}	Input Capacitance[5]	–	5	pF
BW	Closed-loop bandwidth (typical), 3.3V	1–1.5		MHz
	Closed-loop bandwidth (typical), 2.5V	0.8		MHz
R_{OUT}	Output Impedance (typical), 3.3V High drive	29		Ω
	Output Impedance (typical), 3.3V Standard drive	41		Ω
	Output Impedance (typical), 2.5V High drive	37		Ω
	Output Impedance (typical), 2.5V Standard drive	41		Ω
t_{PU}	Power-up time for all VDD's to reach minimum specified voltage (power ramps must be monotonic)	0.01	50	ms
Theta Ja[6]	Dissipation, Junction to Ambient, 8-pin SOIC	131		°C/W
Theta Jc[6]	Dissipation, Junction to Case, 8-pin SOIC	81		°C/W

3.3V DC Electrical Specifications

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.6	V
V_{IL}	Input LOW Voltage		–	0.8	V
V_{IH}	Input HIGH Voltage		2.0	V_{DD} + 0.3	V
I_{IL}	Input Leakage Current	$0 < V_{IN} < V_{IL}$	–	±10	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$	–	100	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA (standard drive) I_{OL} = 12 mA (High drive)	– –	0.4 0.4	V V
V_{OH}	Output HIGH Voltage	I_{OH} = –8 mA (standard drive) I_{OH} = –12 mA (High drive)	2.4 2.4	– –	V V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz (Commercial)	–	12	µA
		REF = 0 MHz (Industrial)	–	25	µA
I_{DD}	Supply Current	Unloaded outputs, 66-MHz REF	–	30	mA

Notes:
4. Applies to Test Circuit #1.
5. Applies to both REF Clock and internal feedback path on CLKOUT.
6. Theta Ja, EIA JEDEC 51 test board conditions, 2S2P; Theta Jc Mil-Spec 883E Method 1012.1.

2.5V DC Electrical Specifications

Parameter	Description	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply Voltage		2.3	2.7	V
V_{IL}	Input LOW Voltage		–	0.7	V
V_{IH}	Input HIGH Voltage		1.7	V_{DD} + 0.3	V
I_{IL}	Input Leakage Current	$0<V_{IN}<V_{DD}$	–	10	µA
I_{IH}	Input HIGH Current	$V_{IN} = V_{DD}$	–	100	µA
V_{OL}	Output LOW Voltage	I_{OL} = 8 mA (Standard drive) I_{OL} = 12 mA (High drive)	– –	0.5 0.5	V V
V_{OH}	Output HIGH Voltage	I_{OH} = –8 mA (Standard drive) I_{OH} = –12 mA (High drive)	V_{DD} – 0.6 V_{DD} – 0.6	– –	V V
I_{DD} (PD mode)	Power Down Supply Current	REF = 0 MHz (Commercial)	–	12	µA
		REF = 0 MHz (Industrial)	–	25	µA
I_{DD}	Supply Current	Unloaded outputs, 66-MHz REF	–	45	mA

3.3V and 2.5V AC Electrical Specifications

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
$1/t_1$	Maximum Frequency[7] (Input/Output)	3.3V High drive	10	–	220	MHz
		3.3V Standard drive	10	–	167	MHz
		2.5V High drive	10	–	200	MHz
		2.5V Standard drive	10	–	133	MHz
T_{IDC}	Input Duty Cycle	<133.3 MHz	25	–	75	%
		>133.3 MHz	40	–	60	%
$t_2 \div t_1$	Output Duty Cycle[8]	<133.3 MHz	47	–	53	%
		>133.3 MHz	45	–	55	%
t_3, t_4	Rise, Fall Time (3.3V)[8]	Std drive, CL = 30 pF, <100 MHz	–	–	1.6	ns
		Std drive, CL = 22 pF, <133.3 MHz	–	–	1.6	ns
		Std drive, CL = 15 pF, <167 MHz	–	–	0.6	ns
		High drive, CL = 30 pF, <100 MHz	–	–	1.2	ns
		High drive, CL = 22 pF, <133.3 MHz	–	–	1.2	ns
		High drive, CL = 15 pF, >133.3 MHz	–	–	0.5	ns
t_3, t_4	Rise, Fall Time (2.5V)[8]	Std drive, CL = 15 pF, <133.33 MHz	–	–	1.5	ns
		High drive, CL = 30 pF, <100 MHz	–	–	2.1	ns
		High drive, CL = 22 pF, <133.3 MHz	–	–	1.3	ns
		High drive, CL = 15 pF, >133.3 MHz	–	–	1.2	ns
t_5	Output to Output Skew [8]	All outputs equally loaded	–	30	100	ps
t_6	Delay, REF Rising Edge to CLKOUT Rising Edge[8]	PLL enabled @ 3.3V	–100	–	100	ps
		PLL enabled @2.5V	–200	–	200	ps
t_7	Part to Part Skew[8]	Measured at $V_{DD}/2$. Any output to any output, 3.3V supply	–	–	±150	ps
		Measured at $V_{DD}/2$. Any output to any output, 2.5V supply	–	–	±300	ps

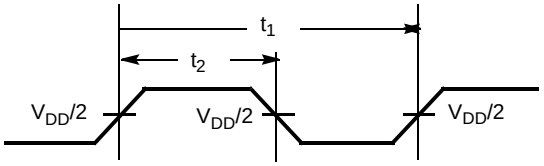
Notes:
7. For the given maximum loading conditions. See C_L in Operating Conditions Table.
8. Parameter is guaranteed by design and characterization. Not 100% tested in production.

3.3V and 2.5V AC Electrical Specifications (continued)

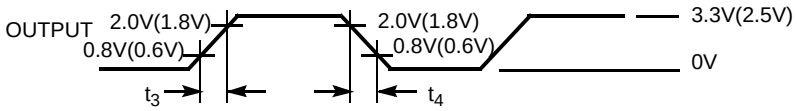
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{LOCK}	PLL Lock Time[8]	Stable power supply, valid clocks presented on REF and CLKOUT pins	–	–	1.0	ms
T_{JCC}[8,9]	Cycle-to-cycle Jitter, Peak	3.3V supply, >66 MHz, <15 pF	–	22	55	ps
		3.3V supply, >66 MHz, <30 pF, standard drive	–	45	125	ps
		3.3V supply, >66 MHz, <30 pF, high drive	–	45	100	ps
		2.5V supply, >66 MHz, <15 pF, standard drive	–	40	100	ps
		2.5V supply, >66 MHz, <15 pF, high drive	–	35	80	ps
		2.5V supply, >66 MHz, <30 pF, high drive	–	52	125	ps
T_{PER}[8,9]	Period Jitter, Peak	3.3V supply, 66–100 MHz, <15 pF	–	18	60	ps
		3.3V supply, >100 MHz, <15 pF	–	13	35	ps
		3.3V supply, >66 MHz, <30 pF, standard drive	–	28	75	ps
		3.3V supply, >66 MHz, <30 pF, high drive	–	26	70	ps
		2.5V supply, >66 MHz, <15 pF, standard drive	–	25	60	ps
		2.5V supply, 66–100 MHz, <15 pF, high drive	–	22	60	ps
		2.5V supply, >100 MHz, <15 pF, high drive	–	19	45	ps

Switching Waveforms

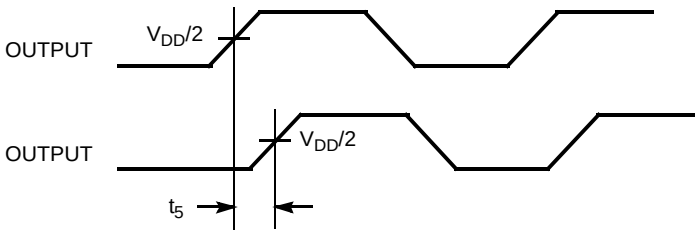
Duty Cycle Timing



All Outputs Rise/Fall Time



Output-Output Skew

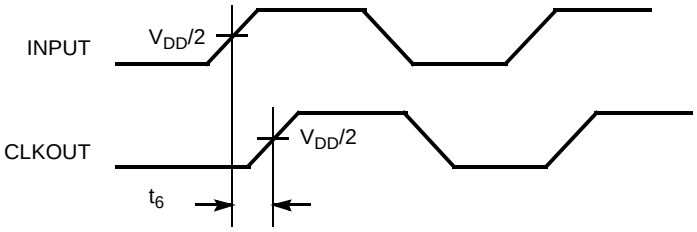


Note:

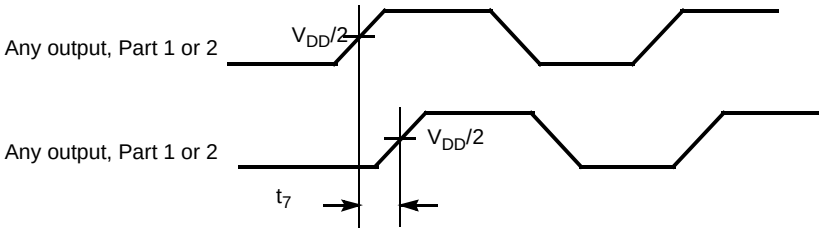
9. Typical jitter is measured at 3.3V or 2.5V, 29°C, with all outputs driven into the maximum specified load. Further information regarding jitter specifications may be found in the application notes, “Understanding Data Sheet Jitter Specifications for Cypress Products.”

Switching Waveforms (continued)

Input-Output Propagation Delay

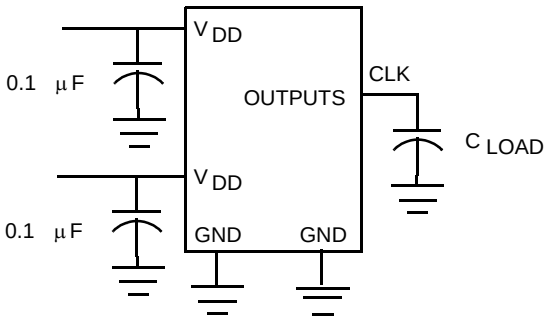


Part-Part Skew



Test Circuits

Test Circuit # 1



Supplemental Parametric Information

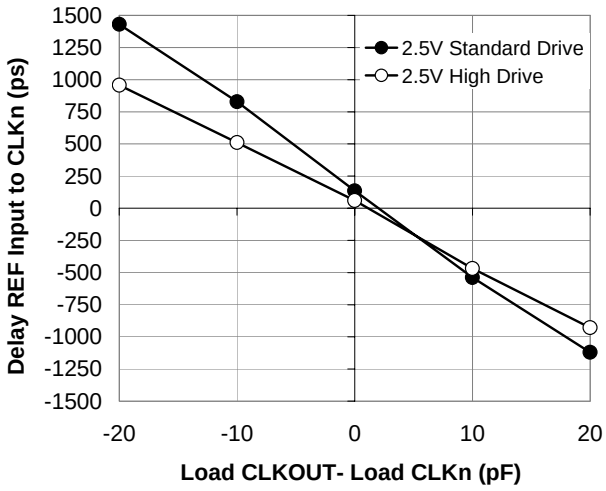


Figure 1. 2.5V Typical Room Temperature Graph for REF Input to CLKn Delay versus Loading Difference between CLKOUT and CLKn. Data is shown for 66 MHz. Delay is a weak function of frequency.

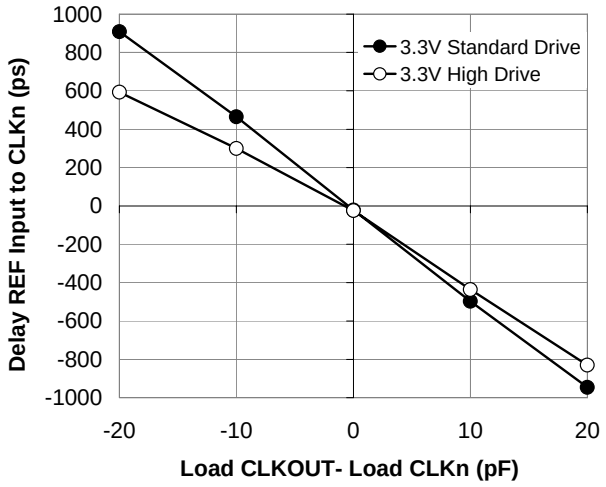


Figure 2. 3.3V Typical Room Temperature Graph for REF Input to CLKn Delay versus Loading Difference between CLKOUT and CLKn. Data is shown for 66 MHz. Delay is a weak function of frequency.

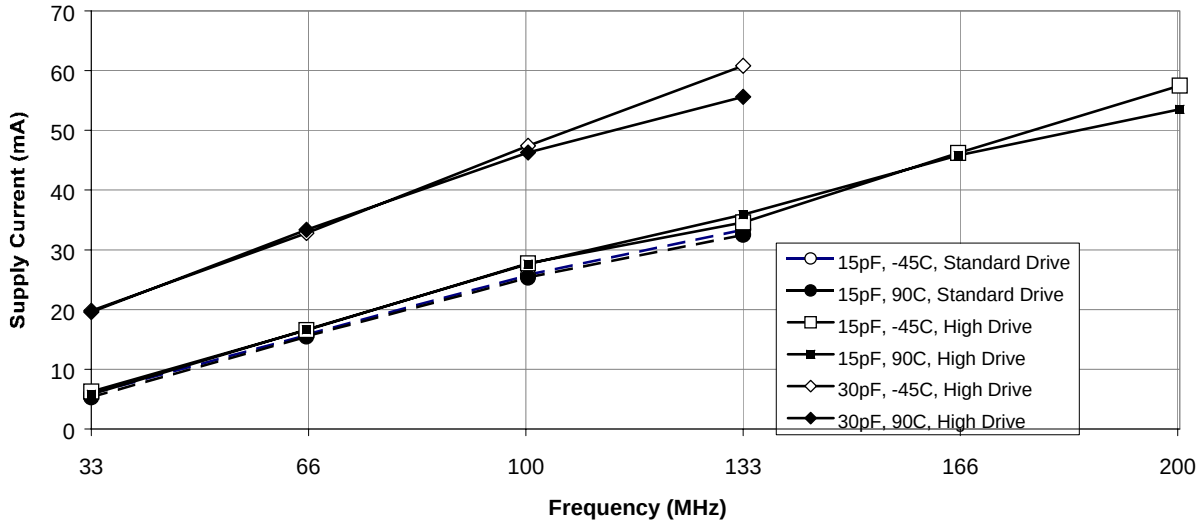


Figure 3. 2.7V Measured Supply Current versus Frequency, Drive Strength, Loading, and Temperature. Note that the 30-pF data above 100 MHz is beyond the data sheet specification of 22 pF.

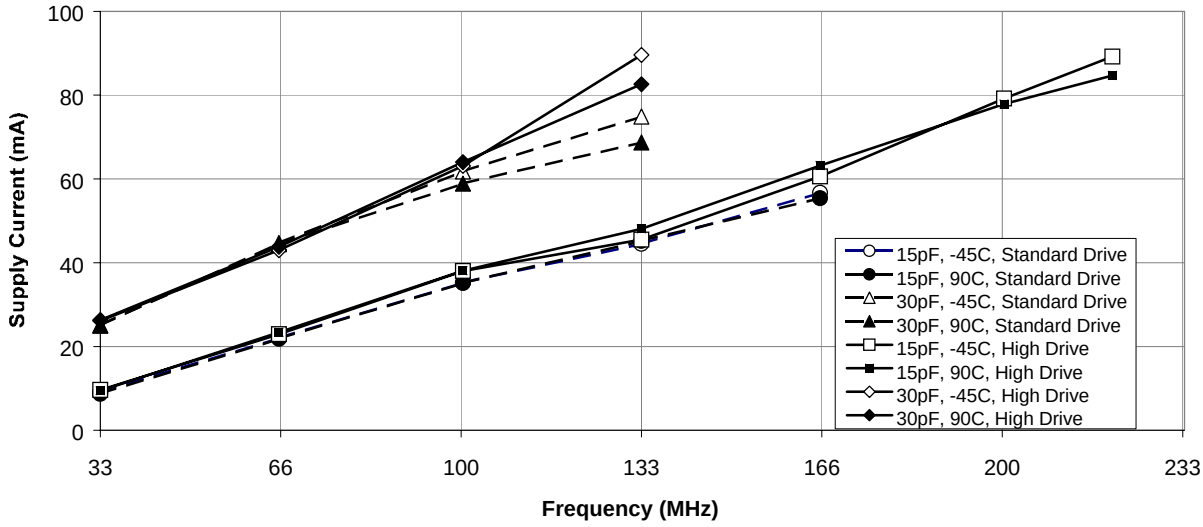


Figure 4. 3.6V Measured Supply Current versus Frequency, Drive Strength, Loading, and Temperature. Note that the 30-pF high-drive data above 100 MHz is beyond the data sheet specification of 22 pF.

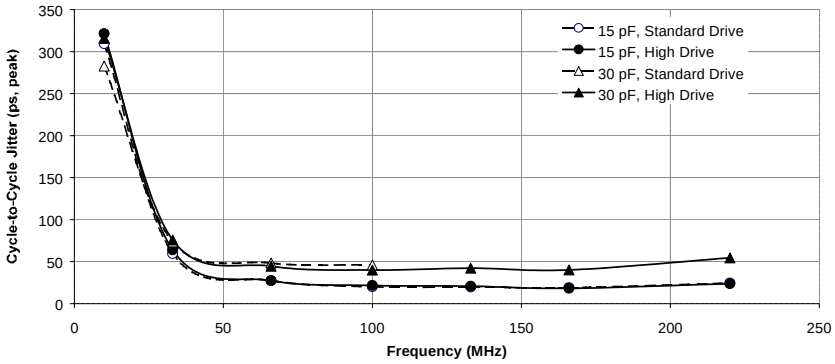


Figure 5. Typical 3.3V Measured Cycle-to-cycle Jitter at 29°C, versus Frequency, Drive Strength, and Loading

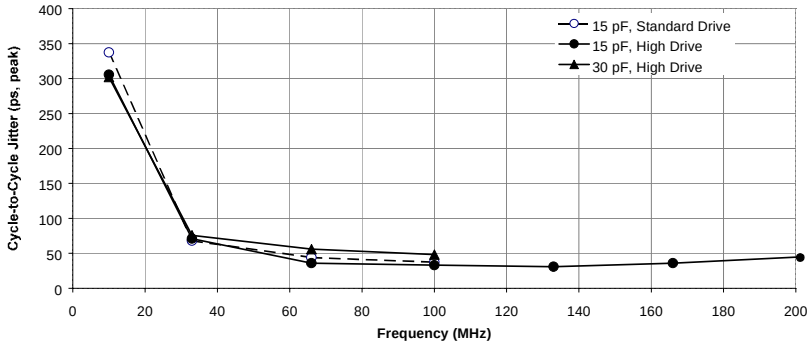


Figure 6. Typical 2.5V Measured Cycle-to-cycle Jitter at 29°C, versus Frequency, Drive Strength, and Loading

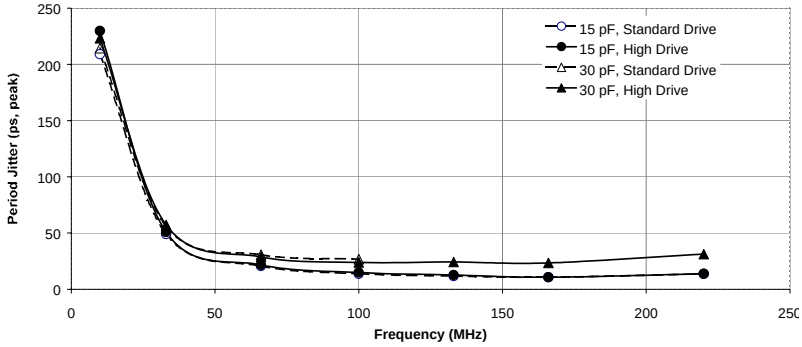


Figure 7. Typical 3.3V Measured Period Jitter at 29°C, versus Frequency, Drive Strength, and Loading

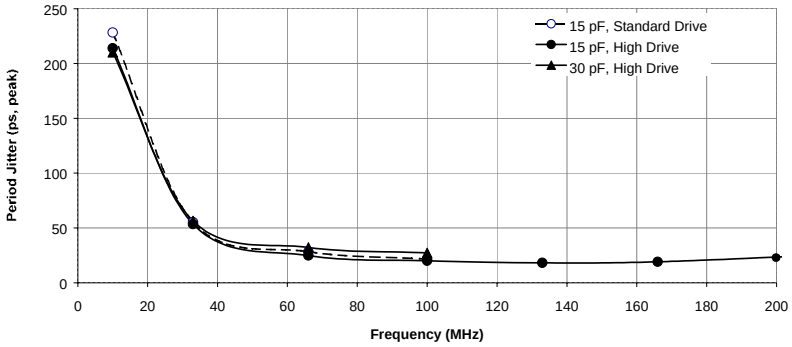


Figure 8. Typical 2.5V Measured Period Jitter at 29°C, versus Frequency, Drive Strength, and Loading

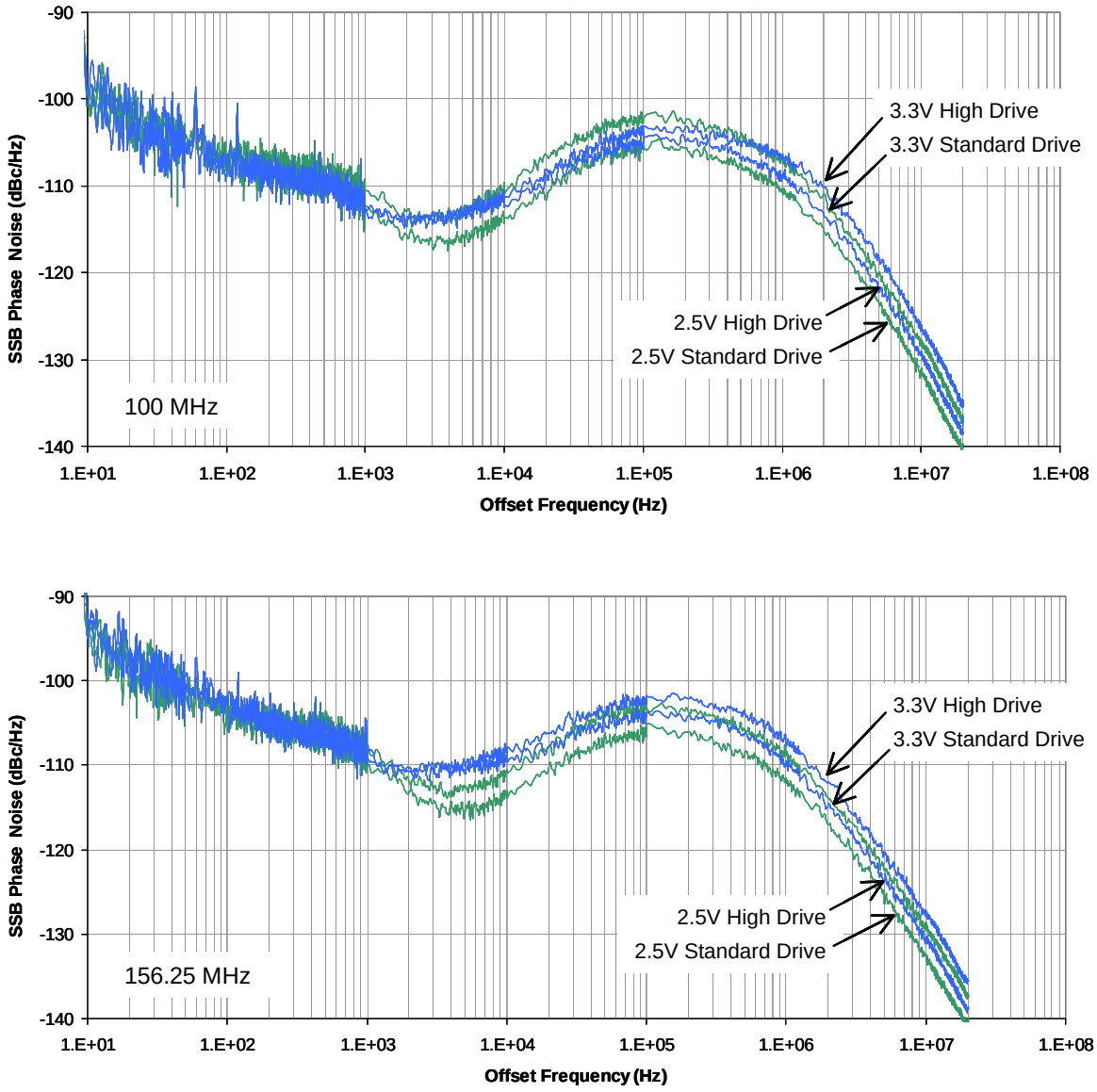


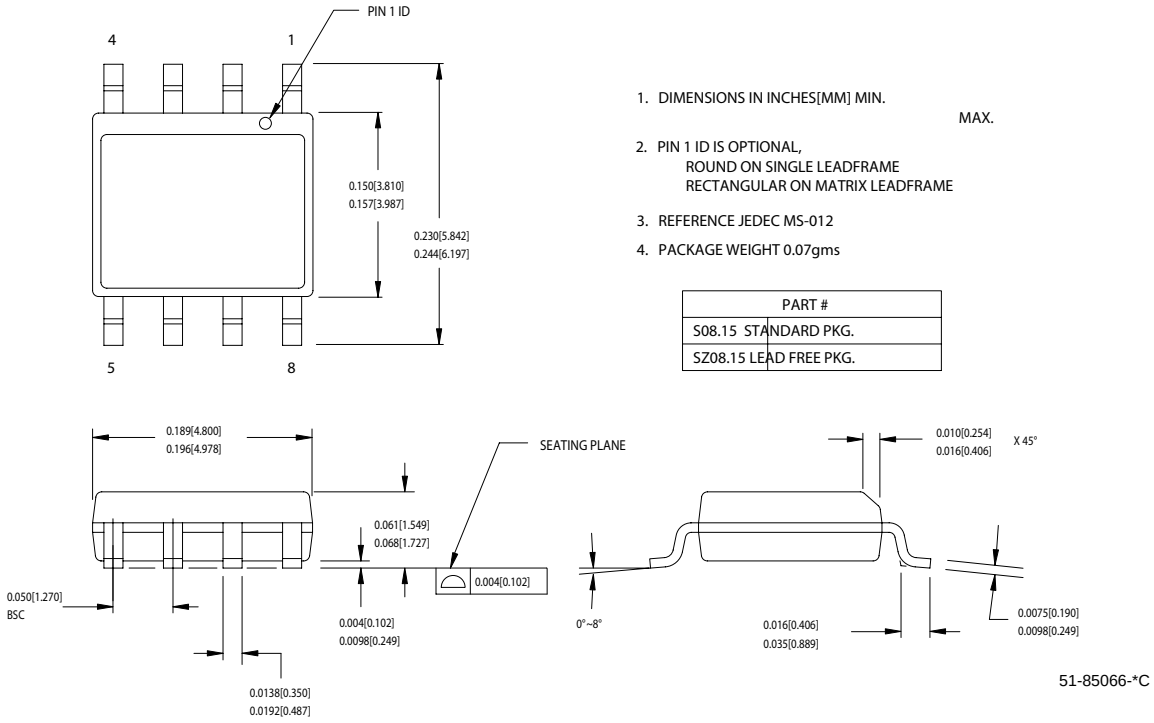
Figure 9. 100 MHz (top) and 156.25 MHz (bottom) Typical Phase-noise Data versus V_{DD} and Drive Strength[9]

Ordering Information

Ordering Code	Package Type	Operating Range
Lead-free		
CY23EP05SXC-1	8-pin 150-mil SOIC	Commercial
CY23EP05SXC-1T	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY23EP05SXI-1	8-pin 150-mil SOIC	Industrial
CY23EP05SXI-1T	8-pin 150-mil SOIC – Tape and Reel	Industrial
CY23EP05SXC-1H	8-pin 150-mil SOIC	Commercial
CY23EP05SXC-1HT	8-pin 150-mil SOIC – Tape and Reel	Commercial
CY23EP05SXI-1H	8-pin 150-mil SOIC	Industrial
CY23EP05SXI-1HT	8-pin 150-mil SOIC – Tape and Reel	Industrial

Package Drawing and Dimensions

8-lead (150-Mil) SOIC S8



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Document History Page

Document Title: CY23EP05 2.5V or 3.3V, 10-220-MHz, Low Jitter, 5 Output Zero Delay Buffer Document Number: 38-07759				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	349620	See ECN	RGL	New data sheet
*A	401073	See ECN	RGL	Updated Delay vs. Load graph with standard drive data Added Phase-noise graph
*B	413826	See ECN	RGL	Minor Change: typo - changed from CY23EP05SXC-T to CY23EP05SXC-1T