4-Channel Power Management IC For Portable Devices

General Description

The EMQ8932 is a high efficiency, 4-channel power management IC for portable devices application. It integrates a complete linear charger for single cell lithium-ion battery, a linear regulator and two high efficiency step-down DC/DC converters.

The linear charger (CH1) operates from 4.25V to 5.5V input voltage and up to 1A charging capability. It is thermal regulated and specifically designed to work within USB power specifications.

The linear regulator (CH2) features ultra-high power supply rejection ratio (75dB at 1kHz), low output voltage noise (30μV), low dropout voltage (270mV), low quiescent current (110μA) and fast transient response. It operates from 2.5V to 5.5V input voltage, up to 600mA loading capability and regulates adjustable output voltage from 1.2V to 5.0V.

The two Synchronous Buck converters (CH3, CH4) operate from 2.5V to 5.5V input voltage, up to 600mA loading capability and regulate adjustable output voltage from 0.6V to VIN. It features low quiescent current, fixed 1.5MHz internal frequency operation.

The EMQ8932 is available in TQFN24 4x4 package,
It is **Green compliant** (RoHS and Halogen-free).

Features

- **Linear Charger**
  - ∗ 4.25V to 5.5V Input Voltage
  - ∗ Programmable charge current up to 1A
  - ∗ Thermal regulation maximizes charge rate without risk of overheating
  - ∗ Act as a LDO when battery is removed
  - ∗ Preset 4.2V charge voltage with ±1% accuracy
  - ∗ Automatic recharge
  - ∗ Charge status indicator
  - ∗ C/10 charge termination
  - ∗ Battery reverse leakage current less than 1μA
  - ∗ 45μA shutdown supply current
  - ∗ Soft-start limits inrush current
- **Linear Regulator**
  - ∗ 1.2V to 5.0V Output Voltage
  - ∗ 75dB Typical PSRR at 1kHz
  - ∗ 30μV RMS Output Voltage Noise (10Hz to 100kHz)
  - ∗ 270mV Typical Dropout at 600mA
- **Two Synchronous Buck Converters**
  - ∗ 0.6V to VIN Output Voltage
  - ∗ Up to 95% Efficiency
  - ∗ Low Dropout Operation: 100% Duty Cycle
  - ∗ No Schottky Diode Needed

- Shutdown Current < 1μA (CH1-CH4)
- Independent Enable PIN(CH1-CH4)
- Independent Input Voltage PIN(CH1-CH4)
- No External Compensation Network needed
- Excellent Line and Load Transient Response(CH1-CH4)
- Over Current Protection
- Over Temperature Protection

Applications

- Hand-held Instruments
- Portable information applications
- Wireless Networking
- GPS
- MP3/MP4/PMP Multi-media

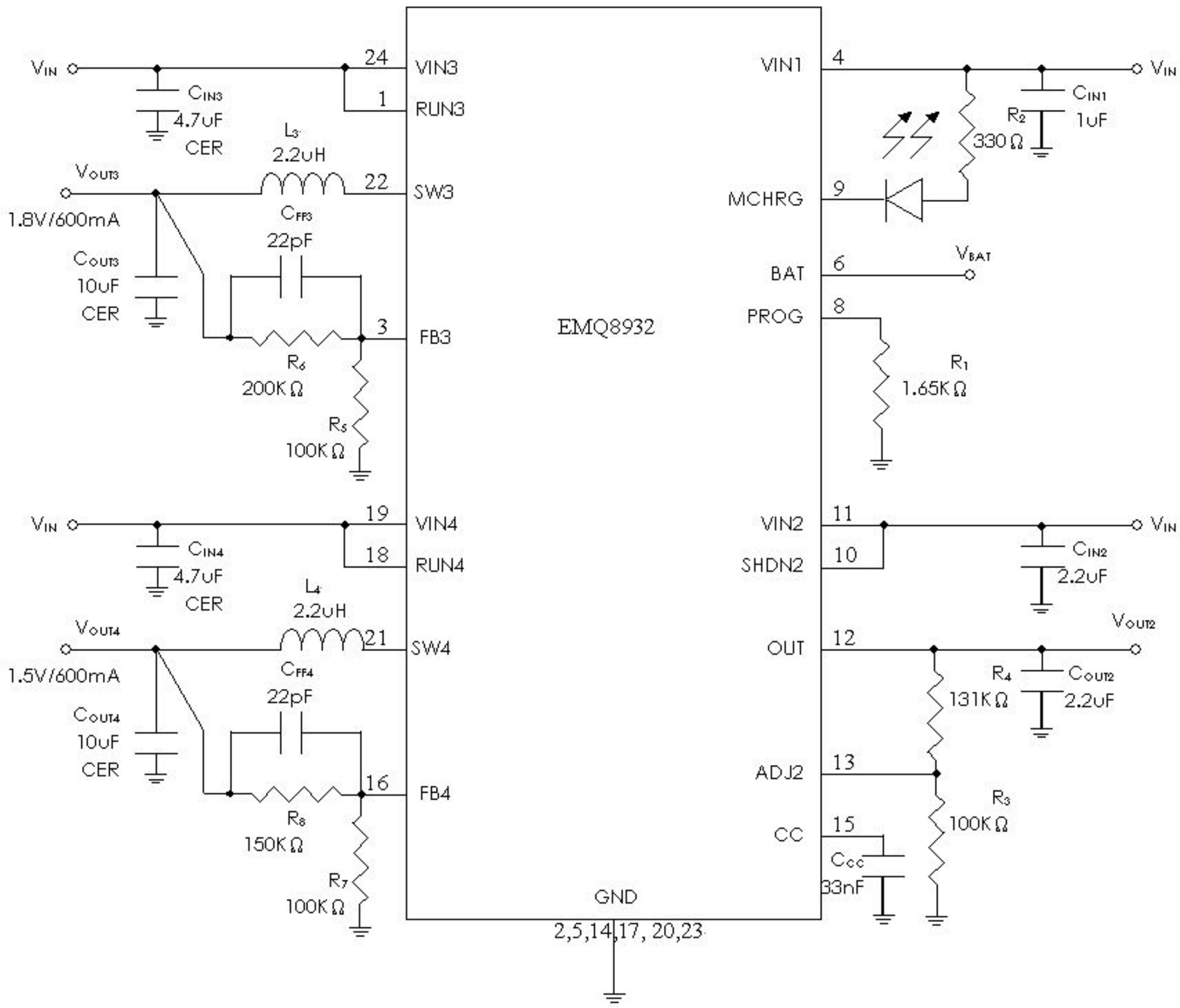
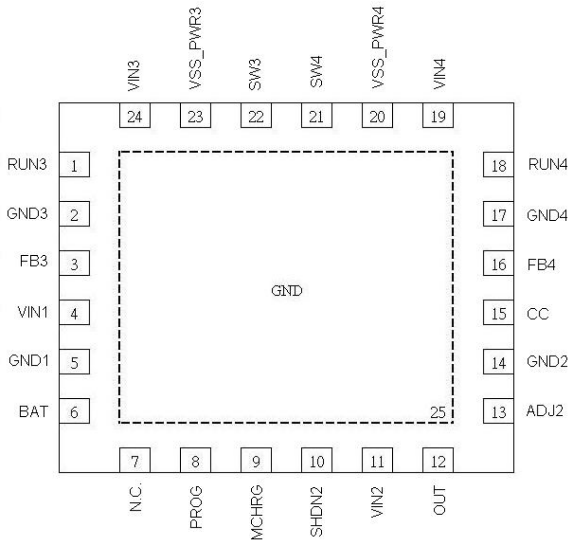


Figure 1. Typical Application

Connection Diagram

TQFN24 4x4



Order Information

EMQ8932-00HC24NRR

00	Adjustable output voltage
HC24	TQFN-24 Package
NRR	RoHS & Halogen free
	Rating: -40 to 85°C
	Package in Tape & Reel

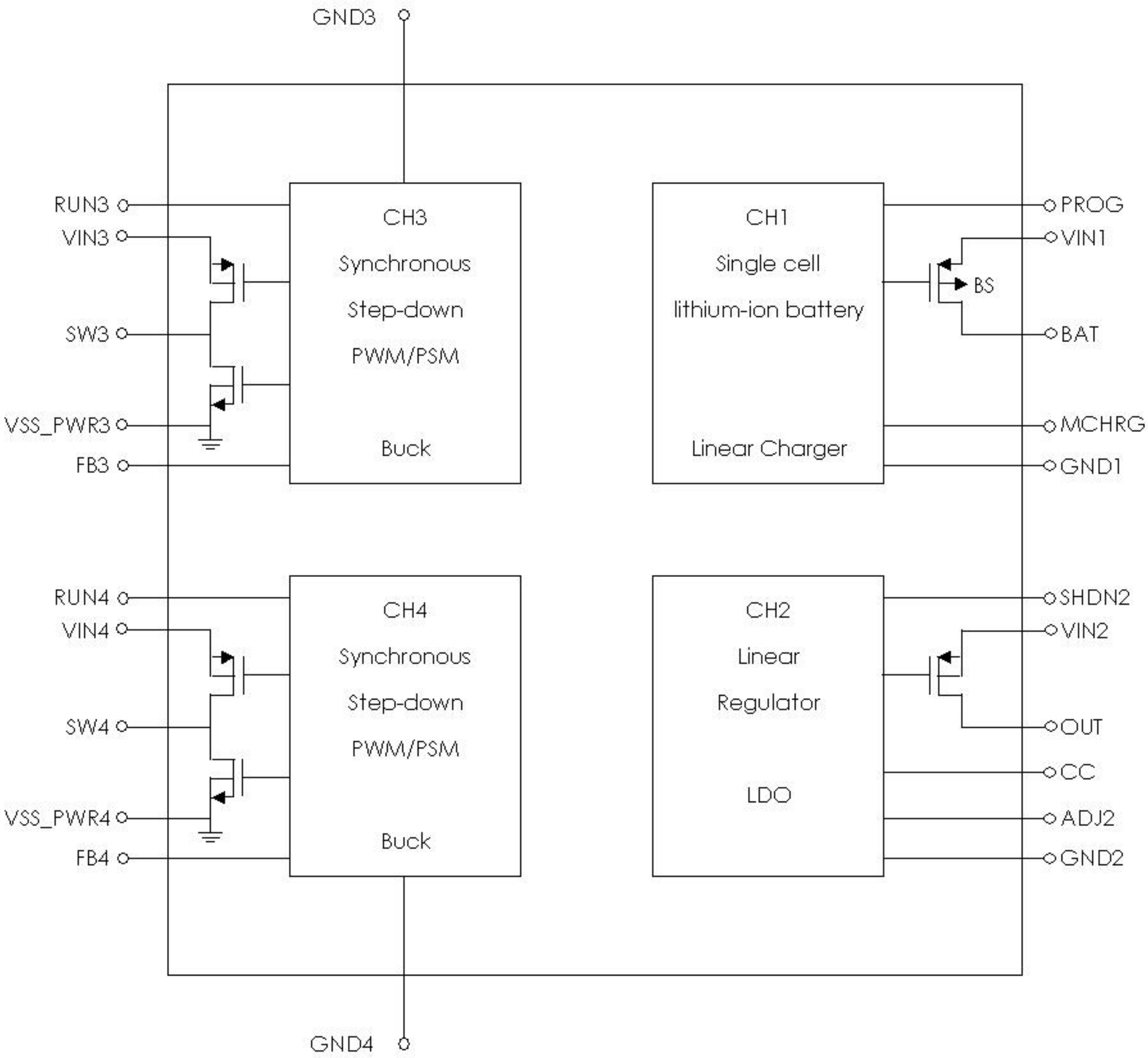
Order, Mark & Packing Information

Package	Product ID	Marking	Packing
TQFN-24	EMQ8932-00HC24NRR	EMP EMQ8932 Tracking Code Pin#1	3K units Tape & Reel

Terminal Functions

Terminal		I/O	Description
Name	NO.		
RUN3	1	I	CH3 Enable Input.
GND3	2	-	Ground.
FB3	3	I	CH3 Voltage Feedback PIN.
VIN1	4	I	CH1 Positive Input Supply Voltage.
GND1	5	-	Ground.
BAT	6	O	CH1 Charge Current Output and battery voltage feedback.
NC	7	-	Non-connection PIN.
PROG	8		CH1 Charge Current Program PIN, $I_{BAT}=(V_{PROG}/R_{PROG})*960$ **The PROG pin must not be directly shorted to ground at any condition.**
MCHRG	9	I	CH1 Open-Drain Charge Status Output.
SHDN2	10	I	CH2 Enable Input.
VIN2	11	I	CH2 Input Voltage.
OUT	12	O	CH2 Output Voltage Feedback.
ADJ2	13	I	CH2 Adjustable Negative Feedback Control.
GND2	14	-	Ground.
CC	15	I	CH2 Compensation Capacitor.
FB4	16	I	CH4 Voltage Feedback PIN.
GND4	17	-	Ground.
RUN4	18	I	CH4 Enable Input.
VIN4	19	I	CH4 Input Voltage.
VSS_PWR4	20	-	Ground.
SW4	21	O	CH4 Switch PIN. Must be connected to Inductor.
SW3	22	O	CH3 Switch PIN. Must be connected to Inductor.
VSS_PWR3	23	-	Ground.
VIN3	24	I	CH3 Input Voltage.

Function Block Diagram



Absolute Maximum Ratings

Supply Input Voltage (VIN, VIN2, VIN3, VIN4)	-0.3V to 6.0V
BAT Pin Voltage	-0.3V to 6.0V
MCHRG Pin Voltage	-0.3V to 6.0V
PROG Pin Voltage	-0.3V to 6.0V
SW3 Switch Pin Voltage	-0.3V to (VIN3+0.3V)
SW4 Switch Pin Voltage	-0.3V to (VIN4+0.3V)
Other I/O Pin Voltage	-0.3V to (VIN+0.3V)
Storage Temperature	-65°C to +150°C
Power Dissipation	1.85W

ESD Susceptibility HBM ---------------- 2KV
MM --------------- 200V

Junction Temperature 150°C

Thermal Resistance

θ_{JA} (TQFN24 4x4) 45°C/W

Operating Ratings

Temperature Range	-40°C ≦ T_A ≦ 85°C
VIN Supply Voltage	4.25V ≦ V_{DD} ≦ 5.5V
Supply Voltage (VIN2, VIN3, VIN4)	2.5V ≦ V_{DD} ≦ 5.5V

Electrical Characteristics

Apply for V_{IN}=5.0V, V_{IN2} = V_{OUT2} +1V (Note 6), V_{EN2} = V_{IN2}, C_{IN2} = C_{OUT2} = 2.2µF, C_{CC2} = 33nF, V_{IN3} = 3.6V, V_{IN4} = 3.6V and T_A = 25°C (unless otherwise noted), Boldface limits apply for the operating temperature extremes: -40°C and 85°C.

Symbol	Parameter	Conditions	EMQ8932 Min	EMQ8932 Typ	EMQ8932 Max	Units
CH1						
V_{IN}	Input voltage		4.25		5.5	V
I_{CC}	Input Supply Current	Charge Mode, R_{PROG}=10K (Note 4)		260		µA
		Standby Mode (Charge Terminated)		106		µA
		Shutdown Mode (R_{PROG} Not Connected, V_{IN}<V_{BAT} or V_{IN} <V_{UV})		45		µA
V_{FLOAT}	Regulated Output (Float) Voltage	0°C ≦ T_A ≦ 85°C	4.158	4.2	4.242	V
I_{BAT}	BAT Pin Current	R_{PROG}=2K, Current Mode		480		mA
		Standby Mode, V_{BAT}=4.2V	-1	0	1	µA
		Shutdown Mode (R_{PROG} Not Connected)	-1	0	1	µA
		Sleep Mode, V_{IN}=0V	-1	0	1	µA
$I_{TRICKLE}$	Trickle Charge Current	V_{BAT}<$V_{TRICKLE}$, R_{PROG}=2K		50		mA
$V_{TRICKLE}$	Trickle Charge Threshold Voltage	R_{PROG}=10K, V_{BAT} Rising		2.9		V
V_{TRHYS}	Trickle Charge Hysteresis Voltage	R_{PROG}=10K		210		mV
V_{UV}	V_{IN} Under voltage Lockout Threshold	From VIN Low to High		3.0		V
V_{UVHYS}	V_{IN} Under voltage Lockout Hysteresis			180		mV
V_{ASD}	V_{IN}-V_{BAT} Lockout Threshold	V_{IN} from Low to High		80		mV

	Voltage	V_{IN} from High to Low		30		mV
I_{TERM}	C/10 Termination Current Threshold	R_{PROG}=10K		0.1		mA/mA
V_{PROG}	PROG Pin Voltage	R_{PROG}=10K, Current Mode		1.0		V
I_{CHGB}	CHGB Pin Weak Pull-Down Current	V_{CHGB}=5V		24		μA
V_{CHGB}	CHGB Pin Output Low Voltage	I_{CHGB} =5mA		0.23		V
V_{RECHRG}	Recharge Battery Threshold Voltage	V_{FLOAT}-V_{RECHRG}		160		mV
T_{ILM}	Junction Temperature in Constant Temperature Mode			120		°C
R_{ON}	Power FET "ON" Resistance			450		mΩ
T_{SS}	Soft-Start Time	I_{BAT}=0 to I_{BAT}=960V/R_{PROG}		100		μs
$T_{RECHARGE}$	Recharge Comparator Filter Time	V_{BAT} High to Low		2.4		ms
T_{TERM}	Termination Comparator Filter Time	I_{BAT} Falling Below I_{CHG}/10		1.1		ms
I_{PROG}	PROG Pin Pull-up Current			0.4		μA
CH2 (note 8)						
V_{IN2}	Input Voltage		**2.5**		**5.5**	V
ΔV_{OTL2}	Output Voltage Tolerance	100μA ≤ I_{OUT2} ≤ 300mA $V_{OUT2\ (NOM)}$ +0.5V ≤ VIN2 ≤ 5.5V (Note 5) ADJ2=V_{OUT2}	-2		+2	% of $V_{OUT\ (NOM)}$
			-3		**+3**	
V_{OUT2}	Output Adjust Range		**1.20**		**5.0**	V
I_{OUT2}	Maximum Output Current	Average DC Current Rating	**600**			mA
I_{LIMIT2}	Output Current Limit		**600**	950		mA
I_{Q2}	Supply Current	I_{OUT2} = 0mA		110		μA
		I_{OUT2} = 600mA		255		
	Shutdown Supply Current	V_{OUT2} = 0V, EN2 = GND		0.001	1	
V_{DO2}	Dropout Voltage (Note 5)	I_{OUT2} = 50mA		19		mV
		I_{OUT2} = 300mA		110		
		I_{OUT2} = 600mA		230		
ΔV_{OU2T}	Line Regulation	I_{OUT2} = 1mA, (V_{OUT2} + 0.5V) ≤ V_{IN2} ≤ 5.5V (Note 6)	-0.1	0.02	0.1	%/V
	Load Regulation	100μA ≤ I_{OUT2} ≤ 600mA		0.001		%/mA

e_{n2}	Output Voltage Noise	I_{OUT2} = 10mA, 10Hz ≤ f ≤ 100kHz		30		μV_{RMS}
VEN2	EN2 Input Threshold	V_{IH}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 8)	**1.2**			V
		V_{IL}, (V_{OUT} + 0.5V) ≤ V_{IN} ≤ 5.5V (Note 8)			**0.4**	
I_{EN2}	EN2 Input Bias Current	EN2 = GND or VIN		0.1	100	nA
I_{ADJ2}	ADJ2 Input Leakage	ADJ2=1.3V (Note 7)		0.1	3	nA
T_{SD}	Thermal Shutdown Temperature	(Note 8)		165		℃
T_{SD_HYST}	Thermal Shutdown Hysteresis			30		℃
T_{ON2}	Start-Up Time	C_{OUT2} = 10µF, V_{OUT2} at 90% of Final Value		80		µs
CH3 (Note 8)						
I_{VFB3}	Feedback Current				±30	nA
V_{FB3}	Regulated Feedback Voltage	T_A = 25°C	0.588	0.600	0.612	V
		–40°C ≤ T_A ≤ 85°C	**0.585**	**0.600**	**0.615**	
ΔV_{FB3}	Reference Voltage Line Regulation	V_{IN3} = 2.5V to 5.5V			**0.4**	%/V
ΔV_{OVL3}	Output Over-voltage Lockout	$\Delta V_{OVL3} = V_{OVL3} - V_{FB3}$	20	50	80	mV
ΔV_{OUT3}	Output Voltage Line Regulation	V_{IN3} = 2.5V to 5.5V			**0.4**	%/V
	Output Voltage Load Regulation			0.5		%
I_{PK3}	Peak Inductor Current	V_{IN3} = 3V, V_{FB3} = 0.5V or V_{OUT3} = 90%, Duty Cycle < 35%		1.0		A
I_{Q3}	Quiescent Current (Note 9)	V_{FB3} = 0.5V or V_{OUT3} = 90%		200	340	µA
	Shutdown	V_{EN3} = 0V, V_{IN3} = 4.2V		0.1	1	µA
f_{OSC3}	Oscillator Frequency	V_{FB3} = 0.6V or V_{OUT3} = 100%	**1.2**	**1.5**	**1.8**	MHz
		V_{FB3} = 0V or V_{OUT3} = 0V		**290**		kHz
R_{PFET3}	$R_{DS(ON)}$ of PMOS	I_{SW3} = 100mA		0.45	0.55	Ω
R_{NFET3}	$R_{DS(ON)}$ of NMOS	I_{SW3} = –100mA		0.40	0.5	Ω
I_{SW3}	SW3 Leakage	V_{EN3} = 0V, V_{SW3} = 0V or 5V, V_{IN3} = 5V			±1	µA
V_{EN3}	EN3 Threshold		0.5		1.3	V
I_{EN3}	EN3 Leakage Current				**±1**	µA
CH4 (Note8)						
I_{VFB4}	Feedback Current				±30	nA

V_{FB4}	Regulated Feedback Voltage	T_A = 25°C	0.588	0.600	0.612	V
		–40°C ≤ T_A ≤ 85°C	**0.585**	**0.600**	**0.615**	
ΔV_{FB4}	Reference Voltage Line Regulation	V_{IN4} = 2.5V to 5.5V			**0.4**	%/V
ΔV_{OVL4}	Output Over-voltage Lockout	$\Delta V_{OVL4} = V_{OVL4} - V_{FB4}$	20	50	80	mV
ΔV_{OUT4}	Output Voltage Line Regulation	V_{IN4} = 2.5V to 5.5V			**0.4**	%/V
	Output Voltage Load Regulation			0.5		%
I_{PK4}	Peak Inductor Current	V_{IN4} = 3V, V_{FB4} = 0.5V or V_{OUT4} = 90%, Duty Cycle < 35%		1.0		A
I_{Q4}	Quiescent Current (Note 9)	V_{FB4} = 0.5V or V_{OUT4} = 90%		200	340	μA
	Shutdown	V_{EN4} = 0V, V_{IN4} = 4.2V		0.1	1	μA
f_{OSC4}	Oscillator Frequency	V_{FB4} = 0.6V or V_{OUT4} = 100%	**1.2**	**1.5**	**1.8**	MHz
		V_{FB4} = 0V or V_{OUT4} = 0V		**290**		kHz
R_{PFET4}	$R_{DS(ON)}$ of PMOS	I_{SW4} = 100mA		0.45	0.55	Ω
R_{NFET4}	$R_{DS(ON)}$ of NMOS	I_{SW4} = –100mA		0.40	0.5	Ω
I_{SW4}	SW4 Leakage	V_{EN4} = 0V, V_{SW4} = 0V or 5V, V_{IN4} = 5V			±1	μA
V_{EN4}	EN4 Threshold		0.5		1.3	V
I_{EN4}	EN4 Leakage Current				**±1**	μA

Note 1: Absolute Maximum ratings indicate limits beyond which damage may occur. Electrical specifications do not apply when operating the device outside of its rated operating conditions.
Note 2: All voltages are with respect to the potential at the ground pin.
Note 3: Maximum Power dissipation for the device is calculated using the following equations:

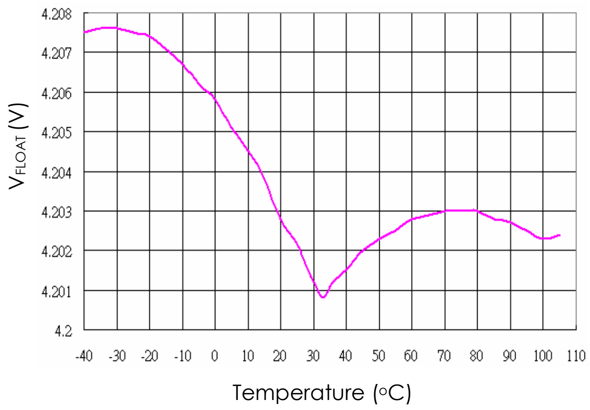
$$P_D = \frac{T_{J(MAX)} - T_A}{\theta_{JA}}$$

where TJ(MAX) is the maximum junction temperature, TA is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.
Note 4: CH1 Supply current includes PROG pin current (approximately 100μA) but does not include any current delivered to the battery through the BAT pin (approximately 96mA).
Note 5: CH2 does not apply to input voltages below 2.5V since this is the minimum input operating voltage.
Note 6: CH2 Dropout voltage is measured by reducing V_{IN} until V_{OUT} drops 100mV from its nominal value at V_{IN} -V_{OUT} = 0.5V. Dropout voltage does not apply to the regulator versions with V_{OUT} less than 2.5V.
Note 7: CH2 The ADJ2 pin is disconnected internally for the preset versions.
Note 8: CH2, CH3 and CH4 build-in internal over-temperature protection to prevent over-load condition.
Note 9: Dynamic quiescent current is higher due to the gate charge delivered at the switching frequency.

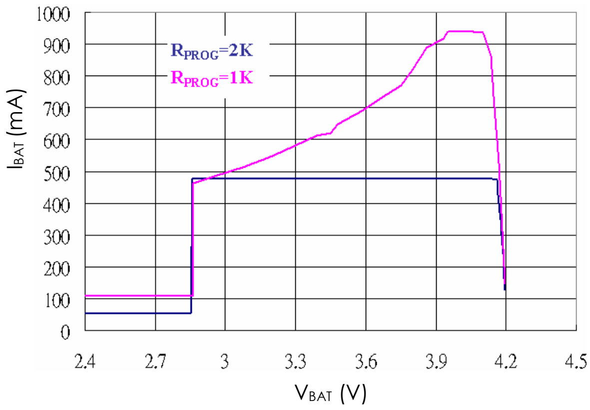
Typical Performance Characteristics

V_{IN}=5.0V, V_{IN2} = $V_{OUT2\ (NOM)}$ + 1V, C_{IN2} = C_{OUT2} = 2.2µF, C_{CC} = 33nF, V_{EN2} = V_{IN2}, V_{EN3} = V_{IN3}, C_{IN3}=4.7µF, L_3=2.2µH, C_{OUT3}=4.7µF, C_{IN4}=4.7µF, L_4=2.2µH, C_{OUT4}=4.7µF, V_{EN4} = V_{IN4} T_A = 25°C, unless otherwise specified

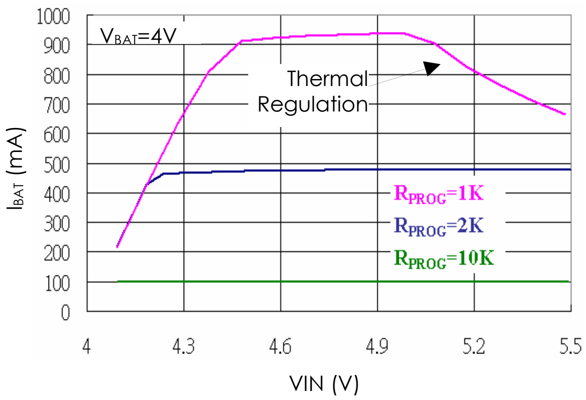
CH1 Regulated Output (Float) Voltage vs Temperature



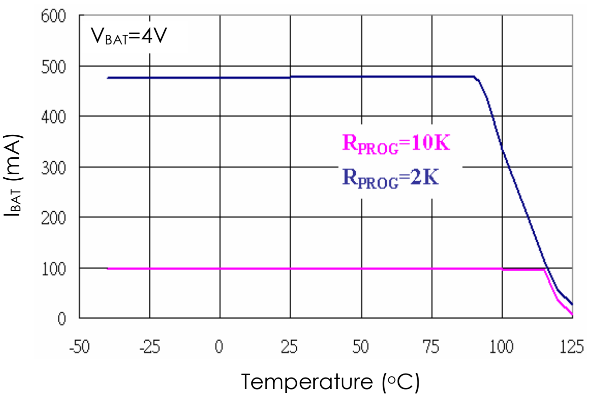
CH1 Charge Current vs Battery Voltage



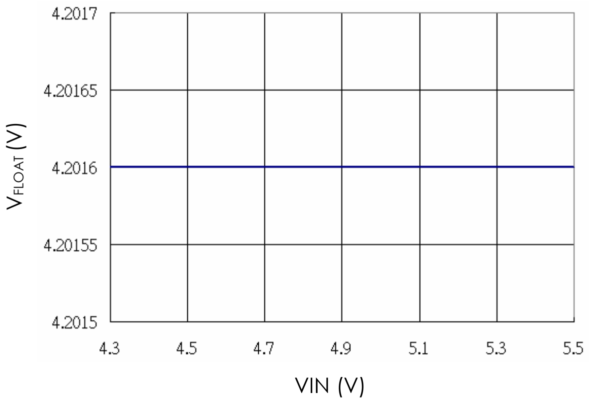
CH1 Charge Current vs Supply Voltage



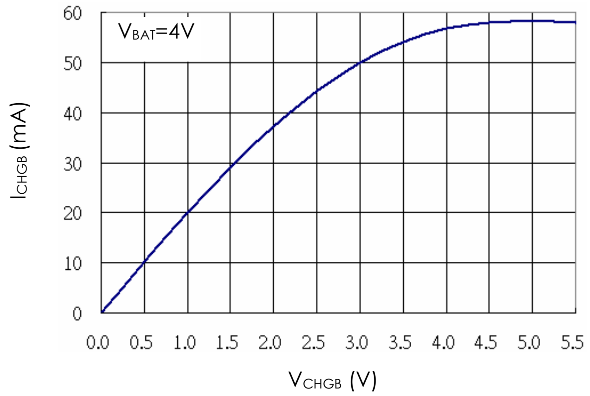
CH1 Charge Current vs Ambient Temperature



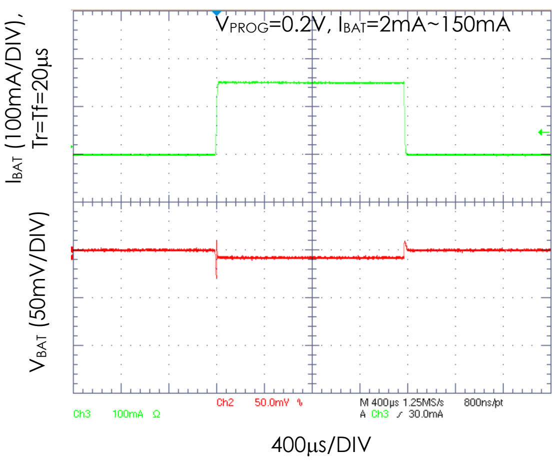
CH1 Regulated Output (Float) Voltage vs Supply Voltage



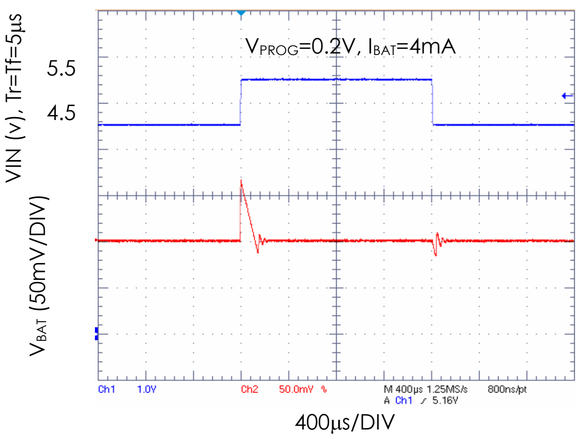
CH1 CHGB Pin I-V Curve (Strong Pull-Down State)



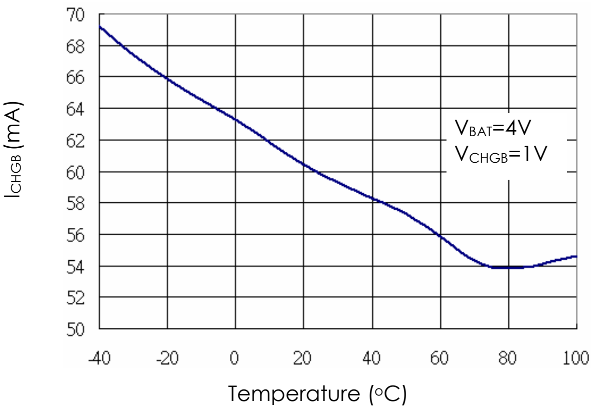
CH1 Load Transient (Battery Removed)



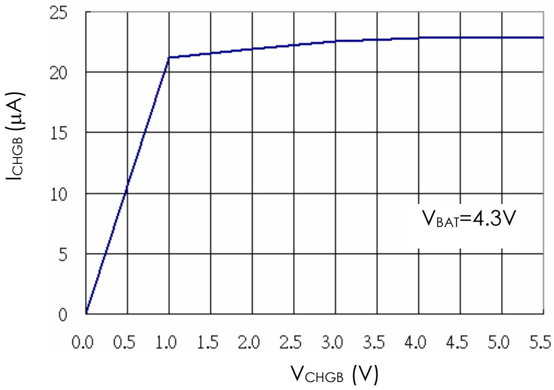
CH1 Line Transient (Battery Removed)



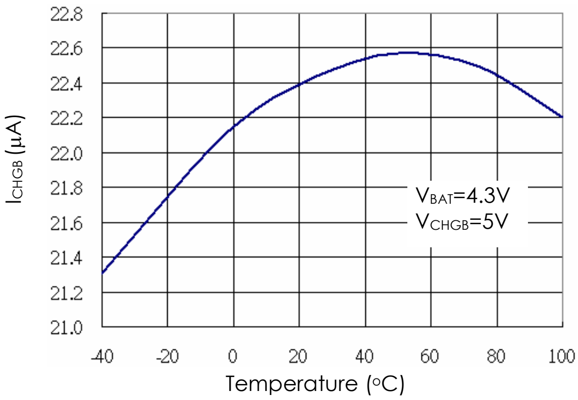
CH1 CHGB Pin Current vs Temperature (Strong Pull-Down State)



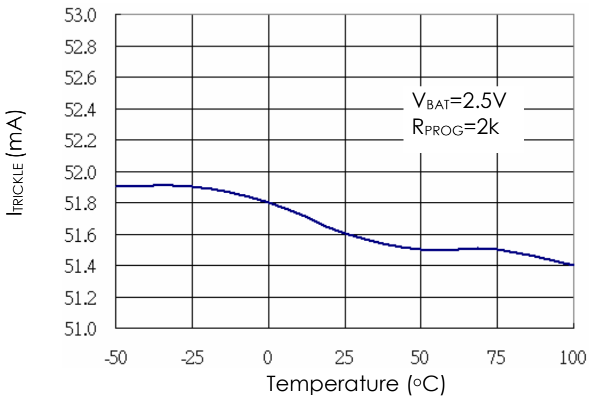
CH1 CHGB Pin I-V Curve (Weak Pull-Down State)



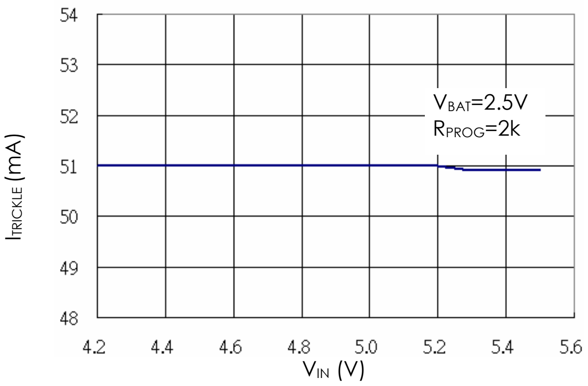
CH1 CHGB Pin Current vs Temperature (Weak Pull-Down State)



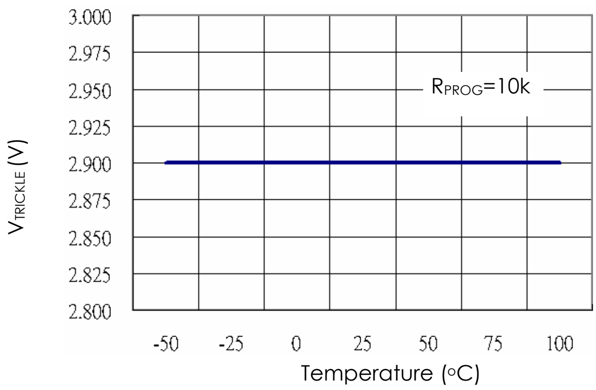
CH1 Trickle Charge Current vs Temperature



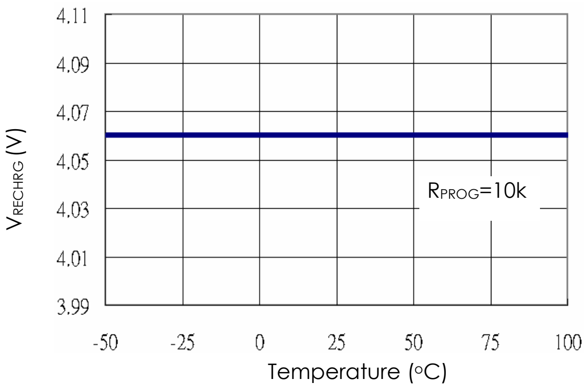
CH1 Trickle Charge Current vs Supply Voltage



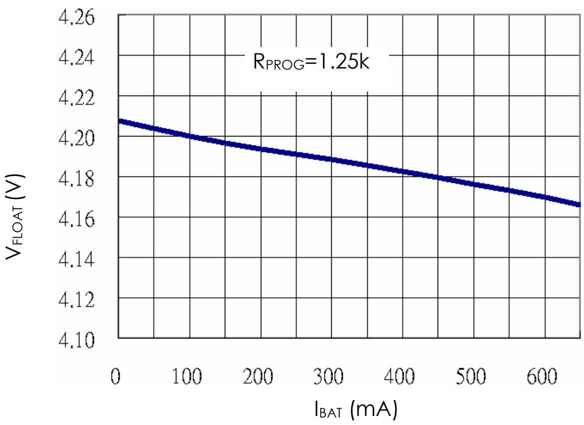
CH1 Trickle Charge Threshold vs Temperature



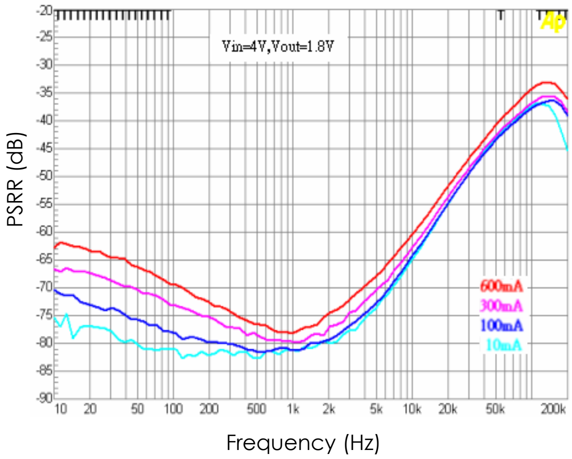
CH1 Recharge Voltage Threshold vs Temperature



CH1 Regulated Output (Float) Voltage vs Charge Current



CH2 PSRR vs. Frequency



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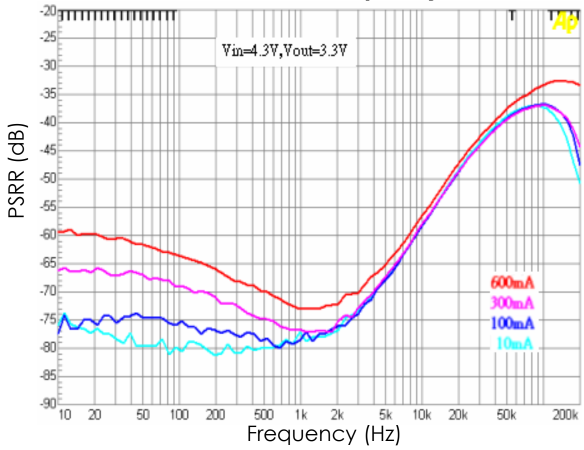

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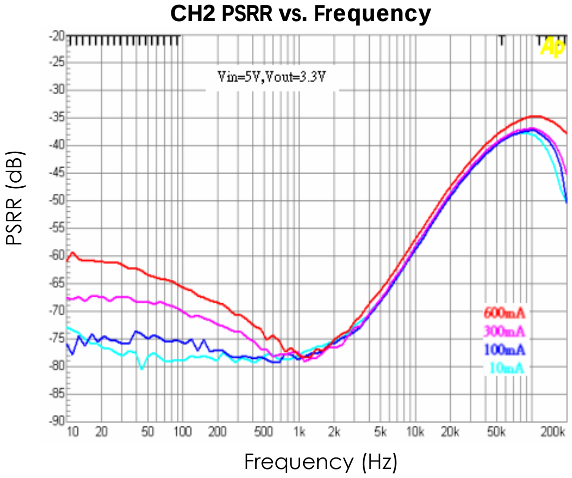

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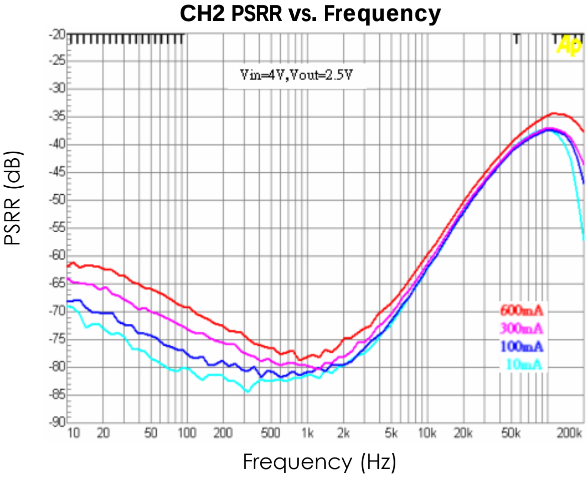
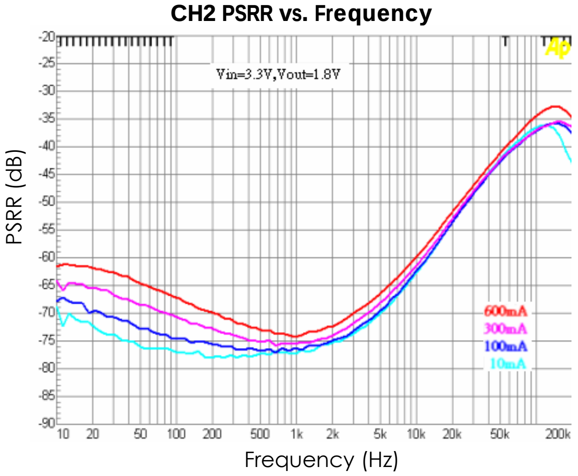
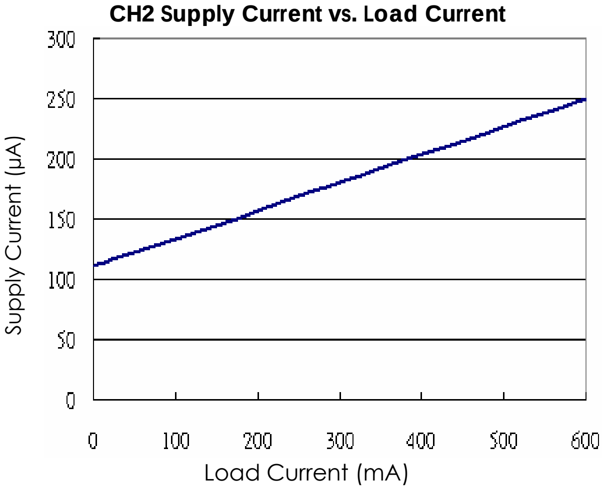


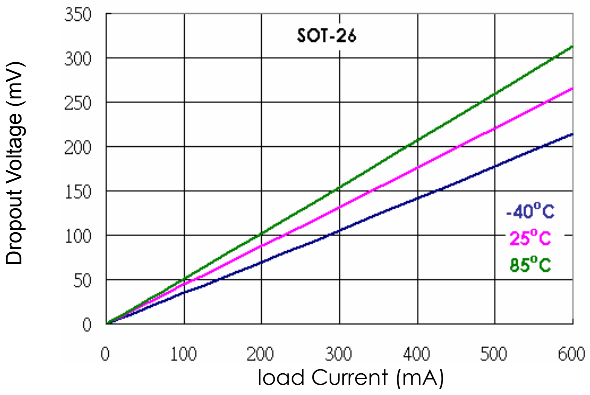
CH2 PSRR vs. Frequency



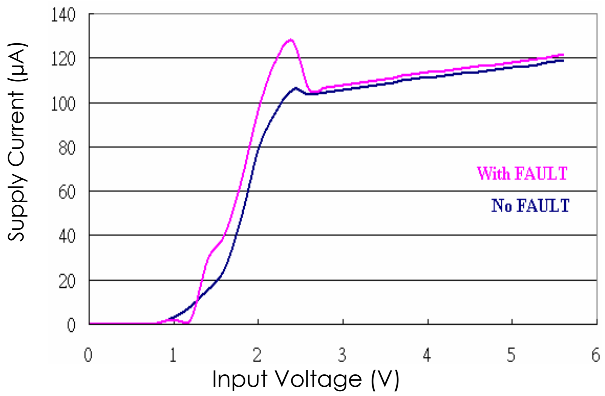
CH2 Supply Current vs. Load Current



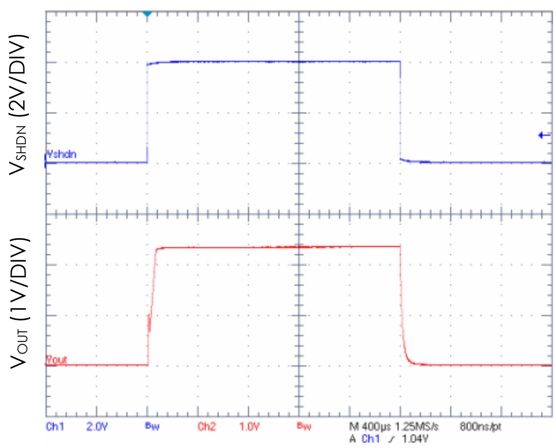
CH2 Dropout Voltage vs. Load Current



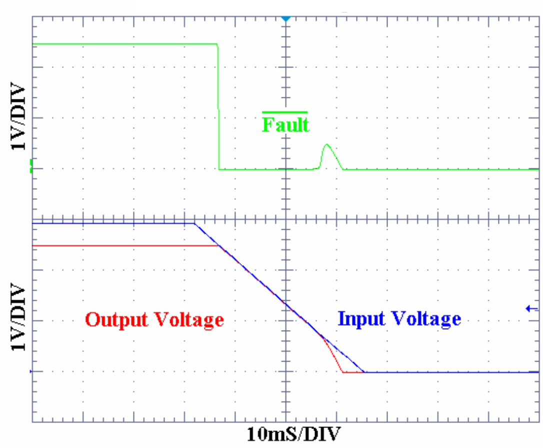
CH2 Supply Current vs. Input Voltage



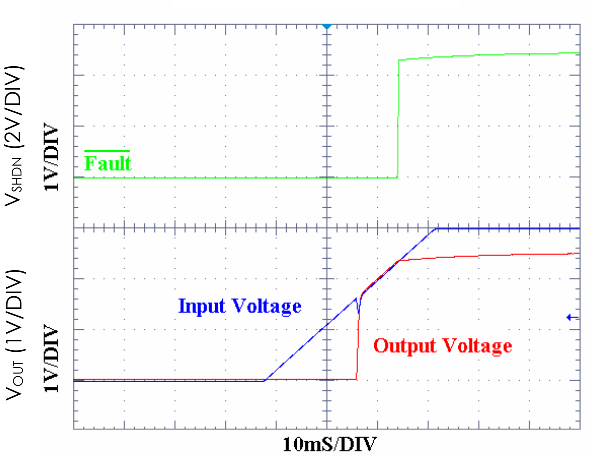
CH2 Enable and Disable



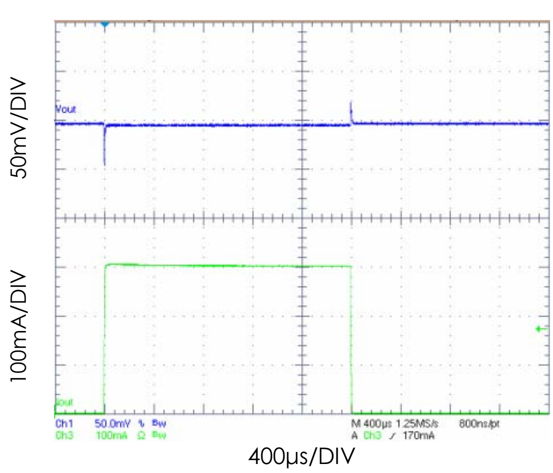
CH2 Power Down Response



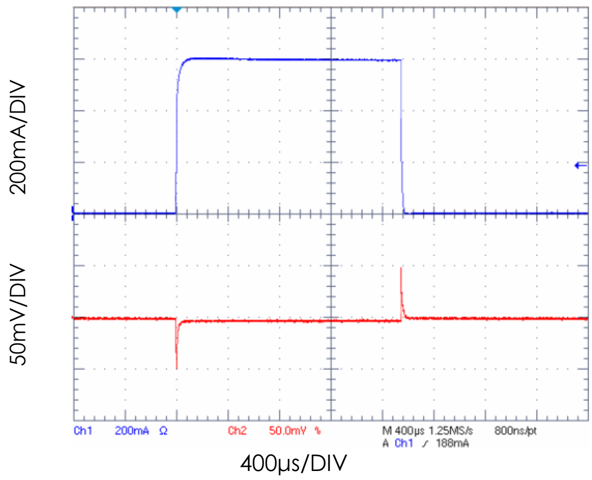
CH2 Power Up Response



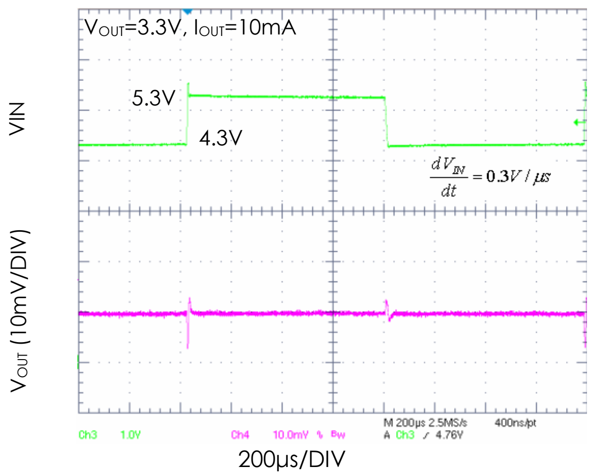
CH2 Load Transient



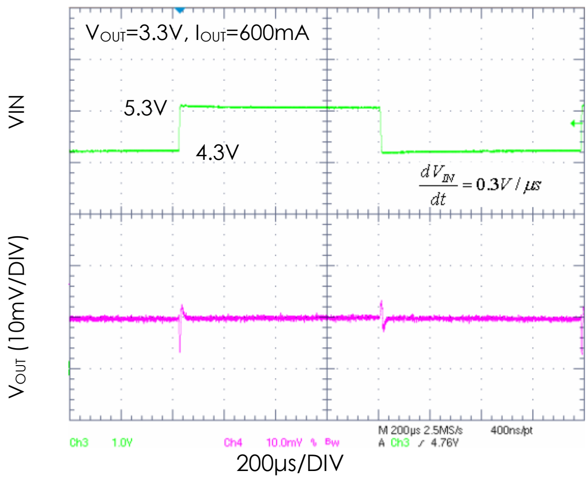
CH2 Load Transient



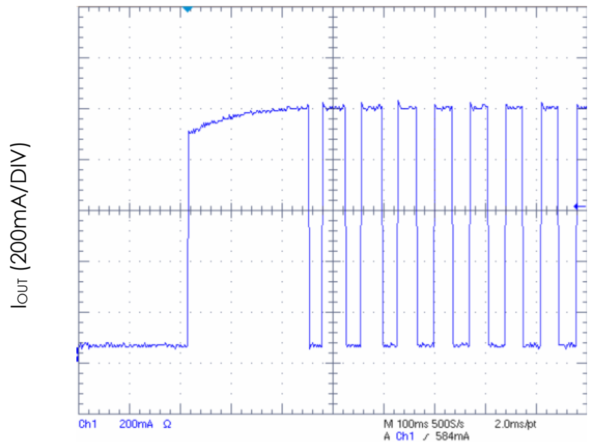
CH2 Line Transient



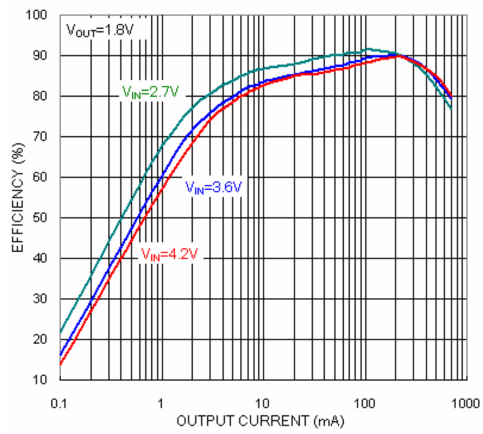
CH2 Line Transient



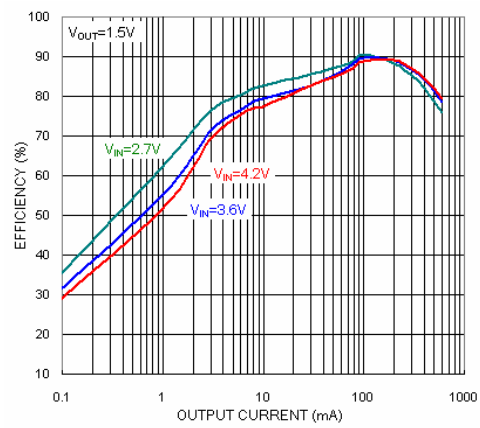
CH2 Current Limit



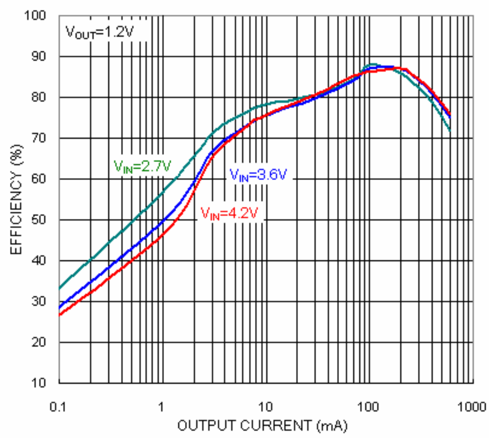
CH3/CH4 Efficiency vs Output Current



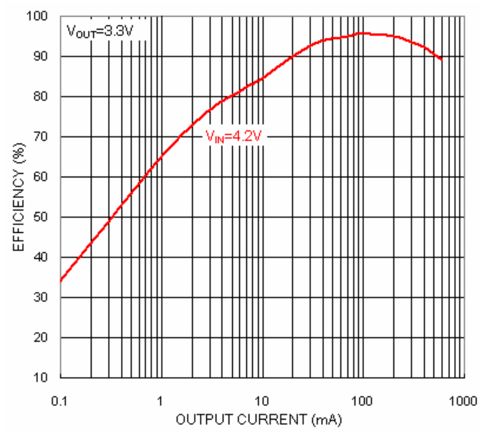
CH3/CH4 Efficiency vs Output Current



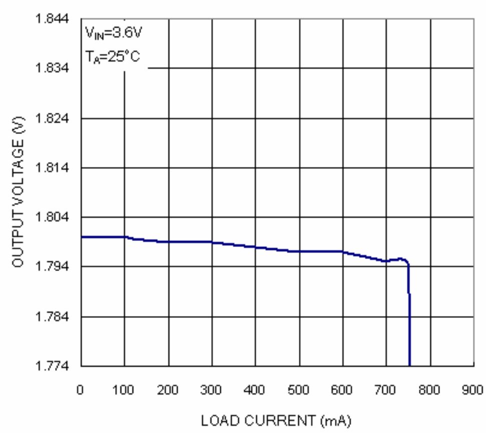
CH3/CH4 Efficiency vs Output Current



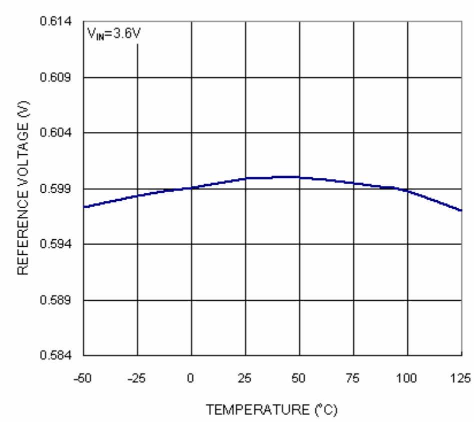
CH3/CH4 Efficiency vs Output Current



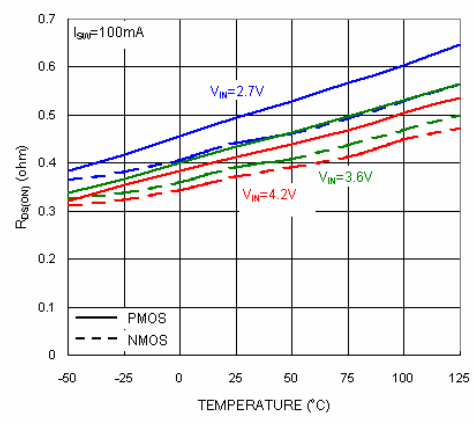
CH3/CH4 Output Voltage vs Load Current



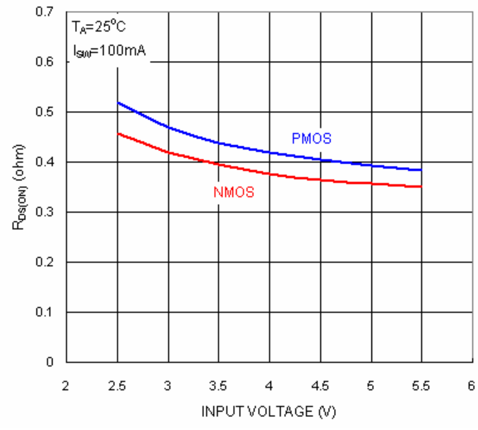
CH3/CH4 Reference voltage vs Temperature



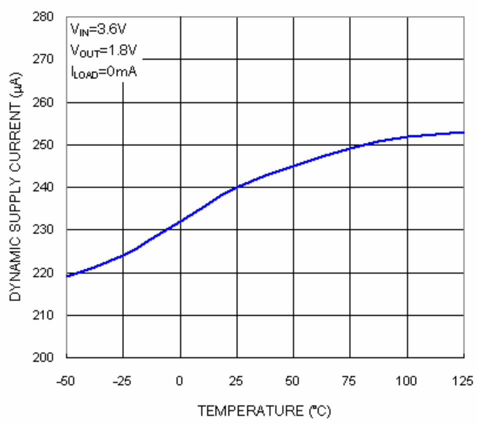
CH3/CH4 $R_{DS(ON)}$ vs Temperature



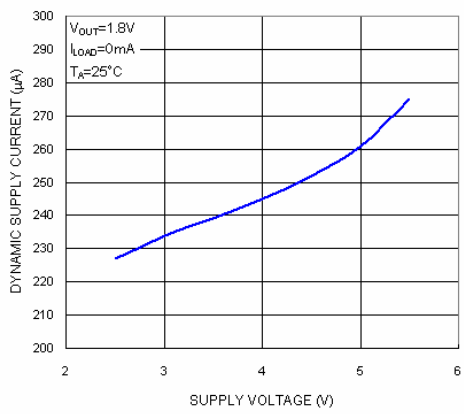
CH3/CH4 $R_{DS(ON)}$ vs Input Voltage



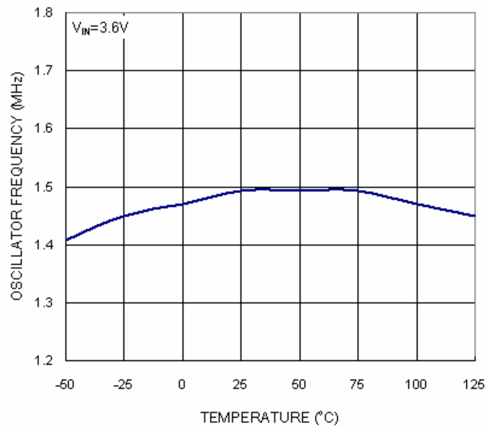
CH3/CH4 Dynamic Supply Current vs Temperature



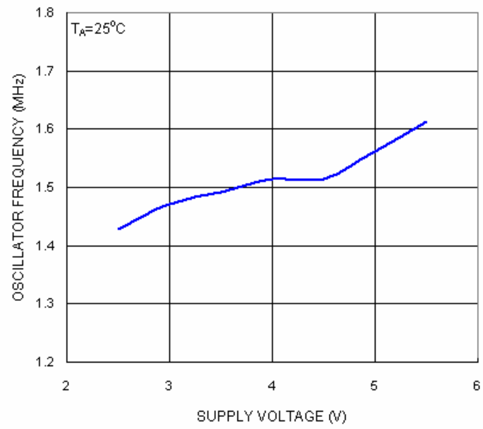
CH3/CH4 Dynamic Supply Current vs Supply Voltage



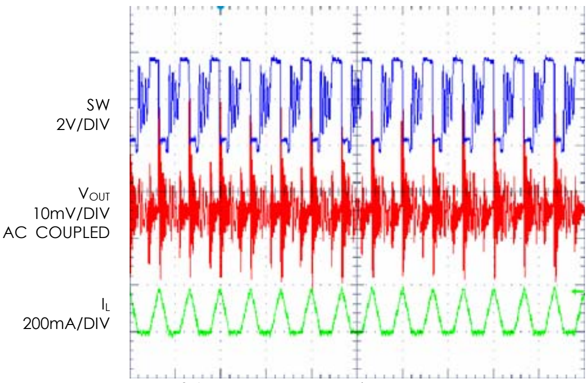
CH3/CH4 Oscillator Frequency vs Temperature



CH3/CH4 Oscillator Frequency vs Supply Voltage

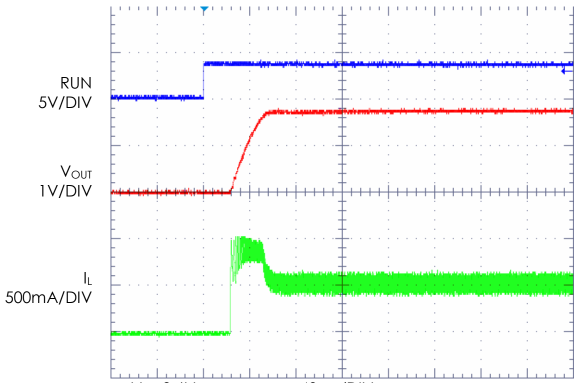


CH3/CH4 Discontinuous Operation



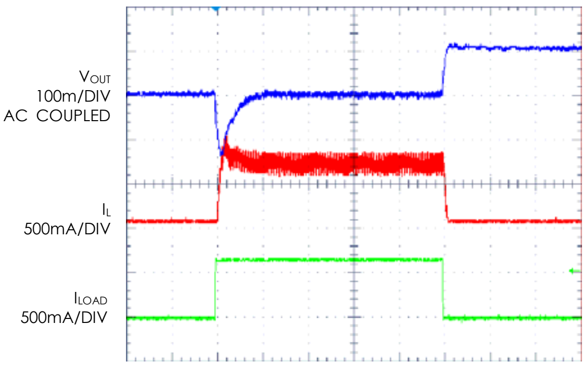
V_{IN}=3.6V 1μs/DIV
V_{OUT}=1.8V
I_{LOAD}=50mA

CH3/CH4 Start-up From Shutdown



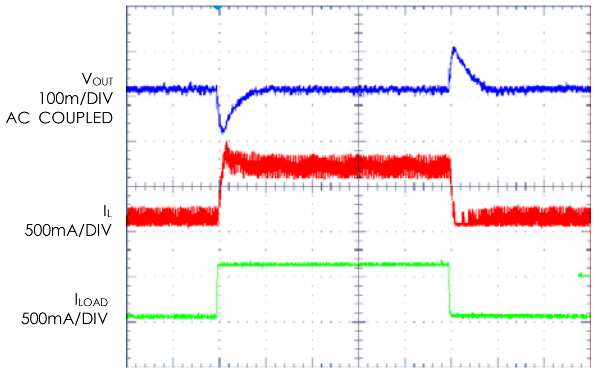
V_{IN}=3.6V 40μs/DIV
V_{OUT}=1.8V
I_{LOAD}=600mA (3Ω RESISTOR)

CH3/CH4 Load Step



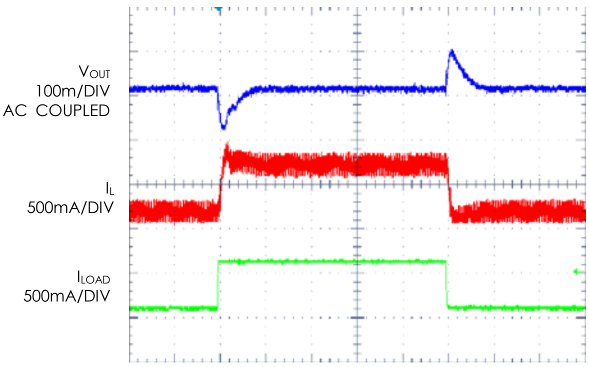
V_{IN}=3.6V 20μs/DIV
V_{OUT}=1.8V
I_{LOAD}=0mA to 600mA

CH3/CH4 Load Step



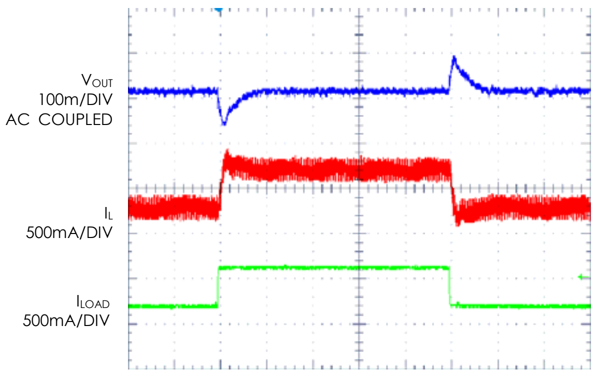
V_{IN}=3.6V 20μs/DIV
V_{OUT}=1.8V
I_{LOAD}=50mA to 600mA

CH3/CH4 Load Step



V_{IN}=3.6V 20μs/DIV
V_{OUT}=1.8V
I_{LOAD}=100mA to 600mA

CH3/CH4 Load Step



V_{IN}=3.6V 20μs/DIV
V_{OUT}=1.8V
I_{LOAD}=200mA to 600mA

Application Information

The EMQ8932 is a high efficiency, 4-channel power management IC for portable devices application.

The four channels are listed as following：

CH1：Linear charger for single cell lithium-ion battery

CH2：High PSRR, low noise, low dropout 600mA LDO

CH3/4：600mA Synchronous Buck converters

CH2/3/4 are Vout adjustable

CH1 Linear Charger

CH1：The Linear Charger is a complete linear charger for single cell lithium-ion battery that is specifically designed to work within USB power specifications.

No external sense resistor and blocking diode are required. Charging current can be programmed externally with a single resistor. The built-in thermal regulation facilitates charging with maximum power without risk of overheating.

The charger always preconditions the battery with 1/10 of the programmed charge current at the beginning of a charge cycle, until 40 s after it verifies that the battery can be fast-charged. The charger automatically terminates the charge cycle when the charge current drops to 1/10th the programmed value after the final float voltage is reached.

The charger can also be used as a LDO when battery is removed. Other features include reverse current protection, shutdown mode, charge current monitor, under voltage lockout, automatic recharge and status indicator.

- **CH1 Programming Charging Current**

The Charging current (I_{BAT}) can be programmed up to 1.0A by equation (1).

$I_{BAT}=(V_{PROG}/R_{PROG})*960$……………………………………(1)

CH2：High PSRR, low noise, low dropout 600mA LDO

The LDO adopts the classical regulator topology in which negative feedback control is used to perform the desired voltage regulating function. The negative feedback is formed by using feedback resistors (R3, R4) to sample the output voltage (V_{OUT2}) for the non-inverting input of the error amplifier, whose inverting input is set to the bandgap reference voltage. By virtue of its high open-loop gain, the error amplifier operates to ensure that the sampled output feedback voltage at its non-inverting input is virtually equal to the preset bandgap reference voltage.

The error amplifier compares the voltage difference at its inputs and produces an appropriate driving voltage to the P-channel MOS pass transistor to control the amount of current reaching the output. If there are changes in the output voltage due to load changes, the feedback resistors register such changes to the non-inverting input of the error amplifier. The error amplifier then adjusts its driving voltage to maintain virtual short between its two input nodes under all loading conditions. In a nutshell, the regulation of the output voltage is achieved as a direct result of the error amplifier keeping its input voltages equal. This negative feedback control topology is further augmented by the shutdown, the temperature protection and current protection circuitry.

- **CH2 Output Voltage Control**

The LDO allows direct user control of the output voltage in accordance with the amount of negative feedback present. To see the explicit relationship between the output voltage and the negative feedback, it is convenient to conceptualize the LDO as an ideal non-inverting operational amplifier with a fixed DC reference voltage V_{REF2} at its non-inverting input. Such a conceptual representation of the LDO in closed-loop configuration is shown in Figure 2. This ideal op amp features an ultra-high input resistance such that its inverting input voltage is virtually fixed at V_{REF2}. The output voltage is therefore given by:

$$V_{OUT2} = V_{REF2}\left[\frac{R_4}{R_3} + 1\right] \text{ ....(2)}$$

This equation can be rewritten in the following form to facilitate the determination of the resistor values for a chosen output voltage:

$$R_4 = R_3\left[\frac{V_{OUT2}}{1.19V} - 1\right] \text{ ....(3)}$$

Set R3 equal to 100kΩ to optimize for overall accuracy, power supply rejection, noise, and power consumption.

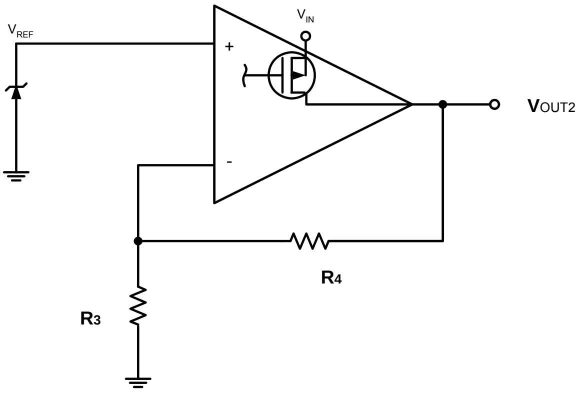


Figure 2. Simplified Regulator Topology

■ CH2 Output Capacitor

The LDO is specially designed for use with ceramic output capacitors of as low as 2.2μF to take advantage of the savings in cost and space as well as the superior filtering of high frequency noise. Capacitors of higher value or other types may be used, but it is important to make sure its equivalent series resistance (ESR) be restricted to less than 0.5Ω. The use of larger capacitors with smaller ESR values is desirable for applications involving large and fast input or output transients, as well as for situations where the application systems are not physically located immediately adjacent to the battery power source. Typical ceramic capacitors suitable for use with the LDO are X5R and X7R. The X5R and the X7R capacitors are able to maintain their capacitance values to within ±20% and ±10%, respectively, as the temperature increases.

■ CH2 No-Load Stability

The LDO is capable of stable operation during no-load conditions, a mandatory feature for some applications such as CMOS RAM keep-alive operations.

■ CH2 Input Capacitor

A minimum input capacitance of 1μF is required for the LDO. The capacitor value may be increased without limit. Improper workbench set-ups may have adverse effects on the normal operation of the regulator. A case in point is the instability that may result from long supply lead inductance coupling to the output through the gate capacitance of the pass transistor. This will establish a pseudo LCR network, and is likely to happen under high current conditions or near dropout. A 10μF tantalum input capacitor will dampen the parasitic LCR action thanks to its high ESR. However, cautions should be exercised to avoid regulator short-circuit damage when tantalum capacitors are used, for they are prone to fail in short-circuit operating conditions.

■ CH2 Compensation (Noise Bypass) Capacitor

Substantial reduction in the output voltage noise of the LDO is accomplished through the connection of the noise bypass capacitor C_{CC} (33nF optimum) between CC pin and the ground. Because CC pin connects directly to the high impedance output of the bandgap reference circuit, the level of the DC leakage currents in the C_{CC} capacitors used will adversely reduce the regulator output voltage. This sets the DC leakage level as the key selection criterion of the C_{CC} capacitor types for use with the

LDO. NPO and COG ceramic capacitors typically offer very low leakage. Although the use of the C_{CC} capacitors does not affect the transient response, it does affect the turn-on time of the regulator. Tradeoff exists between output noise level and turn-on time when selecting this capacitor value.

- **CH2 Power Dissipation and Thermal Shutdown**

Thermal overload results from excessive power dissipation that causes the IC junction temperature to increase beyond a safe operating level. The LDO relies on dedicated thermal shutdown circuitry to limit its total power dissipation. An IC junction temperature T_J exceeding 165°C will trigger the thermal shutdown logic, turning off the P-channel MOS pass transistor. The pass transistor turns on again after the junction cools off by about 30°C. When continuous thermal overload conditions persist, this thermal shutdown action then results in a pulsed waveform at the output of the regulator. The concept of thermal resistance θ_{JA} (°C/W) is often used to describe an IC junction's relative readiness in allowing its thermal energy to dissipate to its ambient air. An IC junction with a low thermal resistance is preferred because it is relatively effective in dissipating its thermal energy to its ambient, thus resulting in a relatively low and desirable junction temperature. The relationship between θ_{JA} and T_J is as follows:

$T_J = \theta_{JA}$ (PD) + T_A .... (4)

T_A is the ambient temperature, and P_D is the power generated by the IC and can be written as:

$P_D = I_{OUT}$ (V_{IN} - V_{OUT}) .... (5)

As the above equations show, it is desirable to work with ICs whose θ_{JA} values are small such that T_J does not increase strongly with P_D. To avoid thermal overloading the LDO, refrain from exceeding the absolute maximum junction temperature rating of 150°C under continuous operating conditions. Overstressing the regulator with high loading currents and elevated input-to-output differential voltages can increase the IC die temperature significantly.

- **CH2 Shutdown**

CH2 enters the sleep mode when the EN2 pin is low. When this occurs, the pass transistor, the error amplifier, and the biasing circuits, including the bandgap reference, are turned off, thus reducing the supply current to typically 1nA. Such a low supply current makes the LDO best suited for battery-powered applications. The maximum guaranteed voltage at the EN2 pin for the sleep mode to take effect is 0.4V. A minimum guaranteed voltage of 1.2V at the EN2 pin would activate the LDO. Direct connection of the EN2 pin to the V_{IN2} to keep the regulator on is allowed for the LDO. In this case, the EN2 pin must not exceed the supply voltage V_{IN2}.

- **Fast Start-Up**

Fast start-up time is important for overall system efficiency improvement. The LDO assures fast start-up speed when using the optional noise bypass capacitor (C_{CC}). To shorten start-up time, the LDO internally supplies a 500µA current to charge up the capacitor until it reaches about 90% of its final value.

CH3/4：600mA Synchronous Buck converters

The typical application circuit of the current mode DC/DC converters is shown in Fig.4.

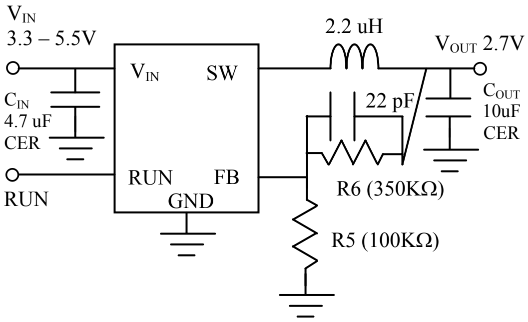


Fig. 3

■ **CH3/4 Inductor Selection**

Basically, inductor ripple current and core saturation are two factors considered to decide the Inductor value.

$$\Delta I_L = \frac{1}{f \cdot L} V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (6)$$

The Eq. 6 shows the inductor ripple current is a function of frequency, inductance, VI_N (V_{IN3}, V_{IN4}) and V_{OUT} (V_{OUT3}, V_{OUT4}). It is recommended to set ripple current to 40% of max. load current. A low DCR inductor is preferred.

■ **CH3/4 C_{IN} and C_{OUT} Selection**

A low ESR input capacitor can prevent large voltage transients at VI_N (V_{IN3}, V_{IN4}). The RMS current of input capacitor is required larger than I_{RMS} calculated by:

$$I_{RMS} \cong I_{OMAX} \frac{\sqrt{V_{OUT}(V_{IN} - V_{OUT})}}{V_{IN}} \quad (7)$$

ESR is an important parameter to select C_{OUT} (C_{OUT3}, C_{OUT4}). The output ripple $\triangle V_{OUT}$ ($\triangle V_{OUT3}$, $\triangle V_{OUT4}$) is determined by:

$$\Delta V_{OUT} \cong \Delta I_L \left(ESR + \frac{1}{8 \cdot f \cdot C_{OUT}}\right) \quad (8)$$

Higher values, lower cost ceramic capacitors are now available in smaller sizes. These ceramic capacitors have high ripple currents, high voltage ratings and low ESR that make them ideal for switching regulator applications. Optimize very low output ripple and small circuit size is doable from C_{OUT} selection since C_{OUT} does not affect the internal control loop stability. It is recommended to use the X5R or X7R which have the best temperature and voltage characteristics of all the ceramics for a given value and size.

■ **CH3/4 Output Voltage (V_{OUT3}, V_{OUT4})**

The output voltage can be determined by following equation:

$$V_{OUT} = 0.6\,V\left(1 + \frac{R_6}{R_5}\right) \quad (9)$$

CH3 Case, Replace R_5 as R_7, R_6 as R_8 in CH4 case.

■ **CH3/4 Thermal Considerations**

Although thermal shutdown is build-in in the step-down DC/DC converter(s) that protects the device from thermal damage, the total power dissipation that the converter(s) can sustain should be base on the package thermal capability. The formula to ensure the safe operation is shown in Note 3.

To avoid the DC/DC converter(s) from exceeding the maximum junction temperature, the user will need to do some thermal analysis.

■ **CH3/4 Guidelines for PCB Layout**

To ensure proper operation of the DC/DC converter(s) , please note the following PCB layout guidelines:

1. The GND trace, the SW (SW3, SW4) trace and the V_{IN} (V_{IN3}, V_{IN4}) trace should be kept short, direct and wide.

2. V_{FB} (FB3, FB4) pin must be connected directly to the feedback resistors. Resistive divider R_5/R_6 (CH3); R_7/R_8 (CH4) must be connected and parallel to the output capacitor C_{OUT} (C_{OUT3}, C_{OUT4}).

3. The Input capacitor C_{IN} (C_{IN3}, C_{IN4}) must be

connected to pin V_{IN} (V_{IN3}, V_{IN4}) as closely as possible.

4. Keep SW (SW3, SW4) node away from the sensitive V_{FB} (FB3, FB4) node since this node is with high frequency and voltage swing.

5. Keep the (–) plates of C_{IN} (C_{IN3}, C_{IN4}) and C_{OUT} (C_{OUT3}, C_{OUT4}) as close as possible.

- **CH3/4 Design Example**

Assume the Step-down DC/DC converter(s) is (are) used in a single lithium-ion battery-powered application. The V_{IN} (V_{IN3}, V_{IN4}) range will be about 2.7V to 4.2V. Output voltage (V_{OUT3}, V_{OUT4}) is 1.8V.

With this information we can calculate L using equation:

$$L = \frac{1}{f \cdot \Delta I_L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \text{..............................(10)}$$

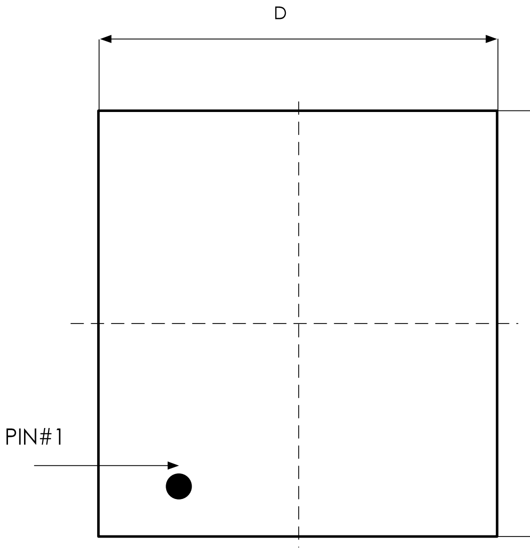
Substituting V_{OUT} = 1.8V, V_{IN} = 4.2V, I_L = 240mA and f = 1.5MHz in eq. 10 gives:

$$L = \frac{1.8V}{1.5MHz \cdot 240mA} \left(1 - \frac{1.8V}{4.2V}\right) = 2.86\mu H \text{ ....(11)}$$

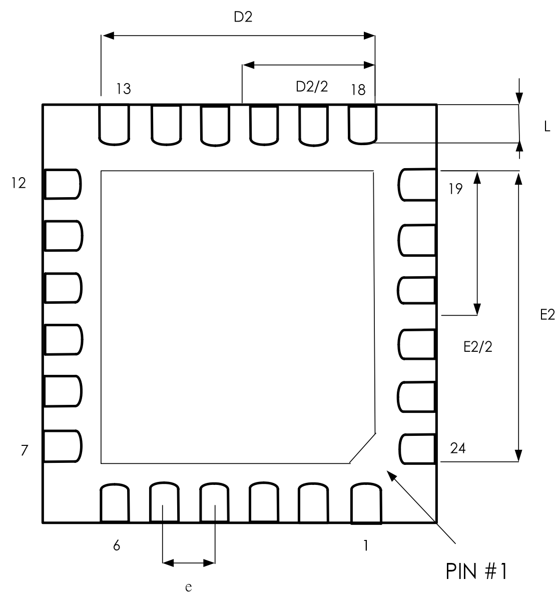
A 2.2μH inductor could be chose with this application.

A greater inductor with less equivalent series resistance makes best efficiency. C_{IN} (C_{IN3}, C_{IN4}) will require an RMS current rating of at least $I_{LOAD(MAX)}/2$ and low ESR. In most cases, a ceramic capacitor will satisfy this requirement.

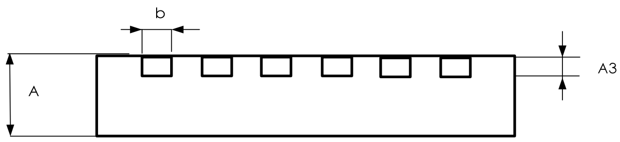
TQFN-24 4x4x0.75mm Outline Dimension



TOP VIEW



BOTTOM VIEW



SIDE VIEW

SYMBOL	COMMON					
	DIMENSIONS MILLIMETER			DIMENSIONS INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.700	0.750	0.800	0.027	0.029	0.031
A3	0.195	0.203	0.211	0.0077	0.0080	0.0083
b	0.180	0.230	0.300	0.007	0.009	0.012
D	3.925	4.000	4.075	0.154	0.157	0.160
E	3.925	4.000	4.075	0.154	0.157	0.160
e	0.50 BSC			0.020 BSC		
L	0.300	0.350	0.400	0.012	0.014	0.016
D2/E2	2.50/2.50	2.65/2.65	2.80/2.80	0.098/0.098	0.104/0.104	0.110/0.110

Revision History

Revision	Date	Description
1.0	2008.05.30	Original
1.1	2008.12.08	Correct pin order of MCHRG and SHDN2 in page 4.
1.2	2009.05.26	Modify order information
1.3	2010.10.13	Modify packing quantity for tape and reel

Important Notice