gm5862H/gm5822H

PRELIMINARY Datasheet

Ordering Information

Part Number	Output Resolution	Package	Temperature Range
gm5862H-LF[(1)]	WUXGA (1920x1200)	256-pin PQFP Lead Free	0-70°C
gm5822H-LF	WSXGA+ (1680x1050)		

Note (1): HDCP enabled parts are only sold to HDCP licensed customers.

GENESIS MICROCHIP CONFIDENTIAL

P/N C5862-DAT-01C

www.gnss.com

Copyright ©2006 Genesis Microchip Inc. All rights reserved. Including the right of reproduction in whole or in part in any form.

Even though Genesis Microchip Inc. has reviewed this publication, GENESIS MICROCHIP INC. MAKES NO WARRANTY OR REPRESENTATION, EITHER EXPRESS OR IMPLIED, WITH RESPECT TO THIS PUBLICATION, ITS QUALITY, ACCURACY, NONINFRINGMENT, MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE. AS A RESULT, THIS PUBLICATION IS PROVIDED "AS IS" AND THE READER ASSUMES THE RISK AS TO ITS QUALITY, ACCURACY, OR SUITABILITY FOR ANY PARTICULAR PURPOSE.

IN NO EVENT WILL GENESIS MICROCHIP INC. BE LIABLE FOR DIRECT, INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES RESULTING FROM ANY DEFECT OR INACCURACY IN THIS PUBLICATION, EVEN IF ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

This publication is provided with RESTRICTED RIGHTS. Use, duplication, or disclosure by the government are subject to restrictions set forth in DFARS 252.277-7013 or 48 CFR 52.227-19 as applicable.

The Genesis logo is a trademark of Genesis Microchip Inc. All other marks, brands and product names are the property of their respective owners.

Free Datasheet http://www.datasheet4u.com/

Revision History

Revision	Date	Description
C5862-DAT-01A	January 2006	Initial Release
C5862-DAT-01B	January 2006	Updated Tables 25, 26, and 30
C5862-DAT-01C	February 2006	Changed Min Sampling Frequency in Table 20 Changed Power Consumption speed, Table 26

Free Datasheet http://www.datasheet4u.com/

Contents

Free Datasheet http://www.datasheet4u.com/

Free Datasheet http://www.datasheet4u.com/

1 Overview

The gm5862H and derivative devices are a highly integrated mixed signal LCD controller for multi-function LCD monitors and LCD TV applications supporting up to WUXGA resolutions. The gm5862H has a proven ADC/PLL and Ultra-Reliable DVI® compatible digital receiver with frame rate conversion to ensure proven PC graphics compatibility.

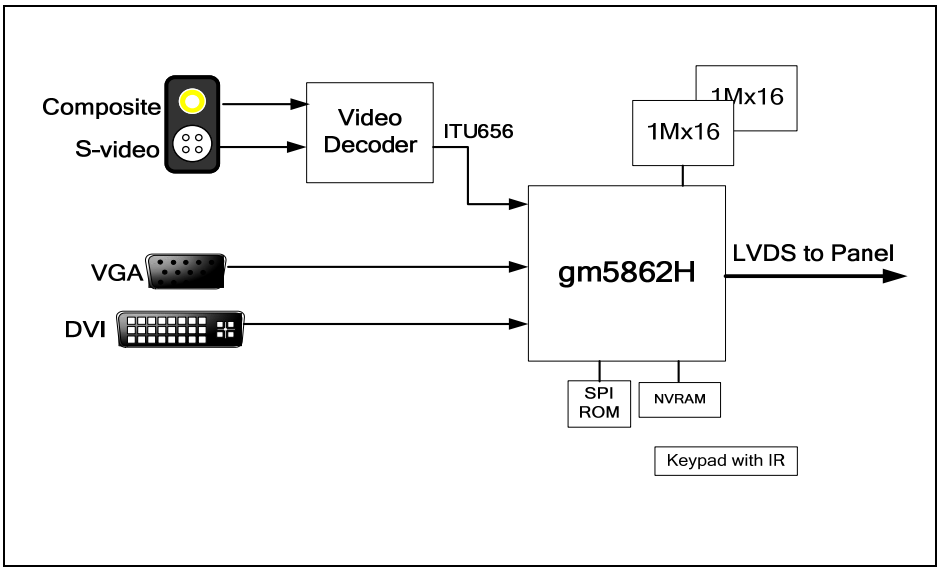
Adaptive Contrast and Color (ACC) and Active Color Management Three Dimension (ACM-3D), coupled with response time compensation provide superior image quality.

With integrated picture-in-picture, embedded microcontroller, versatile OSD engine, low bandwidth general purpose ADC and dual LVDS transmitters (or optional TTL output), the gm5862H family devices enable cost effective high resolution LCD monitor solutions.

1.1 System Design Example

Designs based on the gm5862H have reduced system cost, simplified hardware and firmware design and increased reliability due to the minimal number of components required in the system.

Figure 1: Multi-Function LCD Monitor System Design Example



Free Datasheet http://www.datasheet4u.com/

1.2 Features

DUAL ANALOG INPUT

- Operation up to 205MHz
- Dual RGB inputs
- Single RGB & single YPbPr up to 1080i inputs
- Bi-level and tri-level analog sync support and Macrovision support
- Dual HSYNC, VSYNC and SOG inputs

ULTRA-RELIABLE DVI INPUT

- Operation up to 165MHz
- Direct connect to all DVI compliant digital transmitters
- High-bandwidth Digital Content Protection

DIGITAL VIDEO INPUT

- ITU656 video input support for direct connect to commercially available video decoder
- ITU601 (16-bit) video input support for external MPEG2 decoder, DVI Rx and ADC

HIGH QUALITY ADVANCED SCALING ENGINE

- Independent and programmable H & V scaling factors
- Panoramic scaling (non-linear)
- Variable Sharpness Settings

PICTURE-IN-PICTURE (PIP)

- Variable PIP window size up to 640x480
- Side by side widow up to 960x600
- Video PIP on Graphics/Graphics PIP on Video
- Independent PIP window color controls

ADVANCED DIGITAL COLOR CONTROLS

- Adaptive Contrast and Color and Active Color Management Three Dimension

FRAME RATE CONVERSION (FRC)

- 16-bit/32-bit data path to support single or dual 1Mx16 SDR SDRAM
- Full frame rate conversion up to SXGA 75Hz

RESPONSE TIME COMPENSATION

- Compensates motion blur that results from slow response time of LCD panels – resulting in motion image that is clean and crisp

OSD CONTROLLER

- Up to 4 windows: 1, 2 or 4-bits per pixel color
- Blinking, transparency, blending and proportional fonts support

OUTPUT SUPPORT

- Dual Channel LVDS Transmitters with pin swap for flexibility in PCB layout
- Optional 24-bit TTL

SYSTEM-ON-CHIP INTEGRATION FOR LOWER BOM

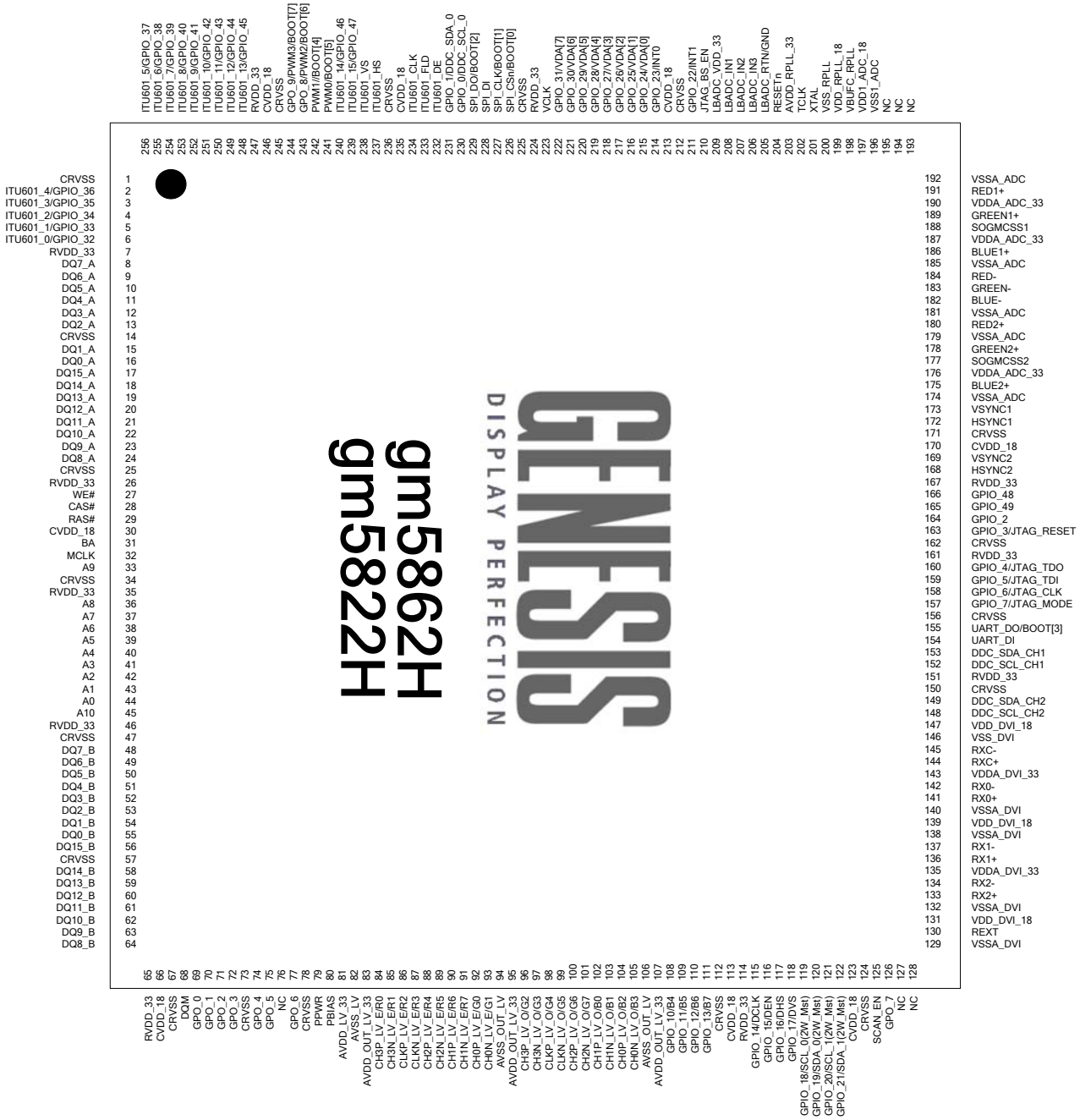
- On-chip reset circuit with Integrated Schmitt trigger for HSYNC and VSYNC
- Embedded x86 MCU with serial interface
- General Purpose Low Bandwidth ADC
- Integrated gamma and 3x3 LUT for sRGB compliance
- ESM® and Boundary Scan Support

Free Datasheet http://www.datasheet4u.com/

2 Pin Diagram

The gm5862H is packaged in a 256-pin Plastic Quad Flat Pack (PQFP).

Figure 2: gm5862H/gm5822H Pinout



Free Datasheet http://www.datasheet4u.com/

3 Pin List

I/O Legend: A = Analog, **I** = Input, **O** = Output, **P** = Power, **G**= Ground

Note: All ground pins to be connected to a single contiguous ground plane (system ground).

Table 1: LVDS Panel Interface

Pin Name	No	I/O	Description
AVDD_LV_3.3	81	AP	3.3V supply for LVDS PLL and Bandgap. Bypass to system ground with a 0.1uF capacitor.
AVSS_LV	82	AG	Ground for LVDS PLL and Bandgap. Tie directly to system ground.
AVDD_OUT_LV_3.3	83	AP	3.3V supply for LVDS/TTL outputs. Bypass to system ground with a 0.1uF capacitor.
CH3P_LV_E/R0	84	AO	LVDS data, shared with LVTTL Display Port R0
CH3N_LV_E/R1	85	AO	LVDS data, shared with LVTTL Display Port R1
CLKP_LV_E/R2	86	AO	LVDS Clock+, Shared with LVTTL Display Port R2
CLKN_LV_E/R3	87	AO	LVDS Clock-, Shared with LVTTL Display Port R3
CH2P_LV_E/R4	88	AO	LVDS data, shared with LVTTL Display Port R4
CH2N_LV_E/R5	89	AO	LVDS data, shared with LVTTL Display Port R5
CH1P_LV_E/R6	90	AO	LVDS data, shared with LVTTL Display Port R6
CH1N_LV_E/R7	91	AO	LVDS data, shared with LVTTL Display Port R7
CH0P_LV_E/G0	92	AO	LVDS data, shared with LVTTL Display Port G0
CH0N_LV_E/G1	93	AO	LVDS data, shared with LVTTL Display Port G1
AVSS_OUT_LV	94	AG	Ground for LVDS/TTL outputs. Tie directly to system ground.
AVDD_OUT_LV_3.3	95	AP	3.3V supply for LVDS/TTL outputs. Bypass to system ground with a 0.1uF capacitor.
CH3P_LV_O/G2	96	AO	LVDS data, shared with LVTTL Display Port G2
CH3N_LV_O/G3	97	AO	LVDS data, shared with LVTTL Display Port G3
CLKP_LV_O/G4	98	AO	LVDS Clock+, Shared with LVTTL Display Port G4
CLKN_LV_O/G5	99	AO	LVDS Clock-, Shared with LVTTL Display Port G5
CH2P_LV_O/G6	100	AO	LVDS data, shared with LVTTL Display Port G6
CH2N_LV_O/G7	101	AO	LVDS data, shared with LVTTL Display Port G7
CH1P_LV_O/B0	102	AO	LVDS data, shared with LVTTL Display Port B0
CH1N_LV_O/B1	103	AO	LVDS data, shared with LVTTL Display Port B1
CH0P_LV_O/B2	104	AO	LVDS data, shared with LVTTL Display Port B2
CH0N_LV_O/B3	105	AO	LVDS data, shared with LVTTL Display Port B3
AVSS_OUT_LV	106	AG	Ground for LVDS/TTL outputs. Tie directly to system ground.
AVDD_OUT_LV_3.3	107	AP	3.3V supply for LVDS/TTL outputs. Bypass to system ground with a 0.1uF capacitor.

Table 2: 656 Video Port

Pad Name	Pin	I/O	Description
GPIO_24/VDA[0]	215	IO	GPIO_24/656 Video Data[0] [5V-tolerant, internal pull-down]
GPIO_25/VDA[1]	216	IO	GPIO_25/656 Video Data[1] [5V-tolerant, internal pull-down]
GPIO_26/VDA[2]	217	IO	GPIO_26/656 Video Data[2] [5V-tolerant, internal pull-down]
GPIO_27/VDA[3]	218	IO	GPIO_27/656 Video Data[3] [5V-tolerant, internal pull-down]
GPIO_28/VDA[4]	219	IO	GPIO_28/656 Video Data[4] [5V-tolerant, internal pull-down]
GPIO_29/VDA[5]	220	IO	GPIO_29/656 Video Data[5] [5V-tolerant, internal pull-down]
GPIO_30/VDA[6]	221	IO	GPIO_30/656 Video Data[6]

Free Datasheet http://www.datasheet4u.com/

Pad Name	Pin	I/O	Description
			[5V-tolerant, internal pull-down]
GPIO_31/VDA[7]	222	IO	GPIO_31/656 Video Data[7] [5V-tolerant, internal pull-down]
VCLK	223	I	Video port data clock input. [5V-tolerant, internal pull-down]

Table 3: 16-bit Video Input

Pin Name	No	I/O	Description
ITU601_4/GPIO_36	2	IO	GPIO_36/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_3/GPIO_35	3	IO	GPIO_35/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_2/GPIO_34	4	IO	GPIO_34/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_1/GPIO_33	5	IO	GPIO_33/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_0/GPIO_32	6	IO	GPIO_32/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_DE	232	I	ITUR-BT601 Data Enable input [5V-tolerant, internal pull-down]
ITU601_FLD	233	I	ITUR-BT601 field detect input [5V-tolerant, internal pull-down]
ITU601_CLK	234	I	ITUR-BT601 clock input [5V-tolerant, internal pull-down]
ITU601_HS	237	I	ITUR-BT601 horizontal sync input [5V-tolerant, internal pull-down]
ITU601_VS	238	I	ITUR-BT601 vertical sync input [5V-tolerant, internal pull-down]
ITU601_15/GPIO_47	239	IO	GPIO_47/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_14/GPIO_46	240	IO	GPIO_48/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_13/GPIO_45	248	IO	GPIO_45/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_12/GPIO_44	249	IO	GPIO_44/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_11/GPIO_43	250	IO	GPIO_43/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_10/GPIO_42	251	IO	GPIO_42/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_9/GPIO_41	252	IO	GPIO_41/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_8/GPIO_40	253	IO	GPIO_40/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_7/GPIO_39	254	IO	GPIO_39/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_6/GPIO_38	255	IO	GPIO_38/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_5/GPIO_37	256	IO	GPIO_37/ ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]

Free Datasheet http://www.datasheet4u.com/

Table 4: Analog Input Port

Pad Name	Pin	I/O	Description
VSSA_ADC	174	AG	Analog ground. Must be directly connected to the system ground.
BLUE2+	175	AI	Positive analog input for Blue2 channel.
VDDA_ADC_3.3	176	AP	Analog power (3.3V) for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Bypass to system ground with a 0.1uF capacitor.
SOGMCSS2	177	AI	Green2 input for Sync-On-Green sync tip clamping. If Sync-On-Green (SoG) or Sync-On-Y (SoY) is not required then SOG_MCSS pin should be left unconnected.
GREEN2+	178	AI	Positive analog input for Green2 channel.
VSSA_ADC	179	AG	Analog ground. Must be directly connected to the system ground.
RED2+	180	AI	Positive analog input for Red2 channel.
VSSA_ADC	181	AG	Analog ground. Must be directly connected to the analog system ground.
BLUE-	182	AI	Common negative analog input for Blue1/Blue2 channel.
GREEN-	183	AI	Common negative analog input for Green1/Green2 channel.
RED-	184	AI	Common negative analog input for Red1/Red2 channel.
VSSA_ADC	185	AG	Analog ground. Must be directly connected to the analog system ground.
BLUE1+	186	AI	Positive analog input for Blue1 channel.
VDDA_ADC_3.3	187	AP	Analog power (3.3V) for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Bypass to system ground with a 0.1uF capacitor.
SOGMCSS1	188	AI	Green1 input for Sync-On-Green sync tip clamping. If Sync-On-Green (SoG) or Sync-On-Y (SoY) is not required then SOG_MCSS pin should be left unconnected.
GREEN1+	189	AI	Positive analog input for Green1 channel.
VDDA_ADC_3.3	190	AP	Analog power (3.3V) for ADC analog blocks that are shared by all three channels. Includes bandgap reference, master biasing and full scale adjust. Bypass to system ground with a 0.1uF capacitor.
RED1+	191	AI	Positive analog input for Red1 channel.
VSSA_ADC	192	AG	Analog ground. Must be directly connected to the system ground.
VSS1_ADC	196	AG	Digital GND for ADC clocking circuit. Must be directly connected to the system ground.
VDD1_ADC_1.8	197	AP	Digital power (1.8V) for ADC encoding logic. Bypass to system ground with a 0.1uF capacitor.

Table 5: Analog Input HS/VS

Pad Name	Pin	I/O	Description
HSYNC2	168	I	ADC input horizontal sync or composite sync [CSYNC2] input channel 2. [Input, programmable schmitt trigger, 5V-tolerant]
VSYNC2	169	I	ADC input vertical sync channel 2. [Input, programmable schmitt trigger, 5V-tolerant]]
HSYNC1	172	I	ADC input horizontal sync or composite sync [CYSYNC1] input1. [Input, programmable schmitt trigger, 5V-tolerant]
VSYNC1	173	I	ADC input vertical sync input channel 1 [Input, programmable schmitt trigger, 5V-tolerant]]

Free Datasheet http://www.datasheet4u.com/

Table 6: DVI Receiver

Pad Name	Pin	I/O	Description
VSSA_DVI	129	AG	Analog GND for internal biasing circuits. Must be connected directly to the system ground.
REXT	130	AI	External termination resistor. A 1%, 250 Ohm resistor should be connected from this pin to VDDA_DVI_3.3 pin.
VDD_DVI_1.8	131	AP	VDD (1.8V) for DVI input logic circuits. Bypass to system ground with a 0.1uF capacitor.
VSSA_DVI	132	AG	Analog GND for internal biasing circuits. Must be connected directly to the system ground.
RX2+	133	AI	DVI input channel 2 positive
RX2-	134	AI	DVI input channel 2 negative
VDDA_DVI_3.3	135	AP	Analog VDD (3.3V) for internal biasing circuits. Bypass to system ground with a 0.1uF capacitor.
RX1+	136	AI	DVI input channel 1 positive
RX1-	137	AI	DVI input channel 1 negative
VSSA_DVI	138	AG	Analog GND for DVI receiver. Must be connected directly to the system ground.
VDD_DVI_1.8	139	AP	VDD (1.8V) for DVI input logic circuits. Bypass to system ground with a 0.1uF capacitor.
VSSA_DVI	140	AG	Analog GND for DVI receiver. Must be connected directly to the system ground.
RX0+	141	AI	DVI input channel 0 positive
RX0-	142	AI	DVI input channel 0 negative
VDDA_DVI_3.3	143	AP	Analog VDD (3.3V) for DVI input analog pll circuits. Bypass to system ground with a 0.1uF capacitor.
RXC+	144	AI	DVI clock input positive side
RXC-	145	AI	DVI clock input negative side
VSS_DVI	146	AG	Digital GND for DVI PLL. Tie directly to system ground.
VDD_DVI_1.8	147	AP	VDD (1.8V) for DVI input logic circuits. Bypass to system ground with a 0.1uF capacitor.

Table 7: CLOCKS

Pad Name	Pin	I/O	Description
VBUFC_RPLL	198	AO	Analog test pin for clocks, RCLK pll, DVI pll and LVDS PLL. Bypass to system ground with a 0.1uF capacitor.
VDD_RPLL_1.8	199	AP	1.8V digital core power for RCLK. Bypass to system ground with a 0.1uF capacitor.
VSS_RPLL	200	AG	Ground for the DDS Reference PLL and digital core. Tie directly to system ground.
XTAL	201	AO	Crystal oscillator output. TCLK and XTAL use same pad cell because the PDX003DG oscillator has 2 pads in it
TCLK	202	AI	Reference clock (TCLK) from the 14.3MHz crystal or TTL oscillator.
AVDD_RPLL_3.3	203	AP	Analog power (3.3V) for the Reference DDS PLL. Bypass to system ground with a 0.1uF capacitor.

Free Datasheet http://www.datasheet4u.com/

Table 8: Digital Power and Ground

Pad Name	Pin	I/O	Description
RVDD_3.3	7 26 35 46 65 114 151 161 167 224 247	P	Ring VDD, 3.3V. All power pins must be bypassed to system ground with a 0.1uF ceramic capacitor placed in close proximity of the pin.
CVDD_1.8	30 66 113 123 170 213 235 246	P	Core VDD, 1.8V. All power pins must be bypassed to system ground with a 0.1uF ceramic capacitor placed in close proximity of the pin.
CRVSS	1 14 25 34 47 57 67 73 78 112 124 150 156 162 171 212 225 236 245	G	Ring/Core shared VSS. Tie directly to the system ground.

Table 9: System Interface

Pad Name	Pin	I/O	Description
PPWR	79	O	Panel Power Control. To be used with PBIAS for correct power up/down sequencing (timing is user programmable). [Tri-state output]
PBIAS	80	O	Panel Bias Control (backlight enable). To be used with PPWR for correct power up/down sequencing (timing is user programmable). [Tri-state output]
GPIO_10/B4	108	IO	GPIO_10; shared with LVTTL Display Port Blue 4; [5V-tolerant, internal pull-down]
GPIO_11/B5	109	IO	GPIO_11; shared with LVTTL Display Port Blue 5; [5V-tolerant, internal pull-down]
GPIO_12/B6	110	IO	GPIO_12; shared with LVTTL Display Port Blue 6; [5V-tolerant, internal pull-down]
GPIO_13/B7	111	IO	GPIO_13; shared with LVTTL Display Port Blue 7; [5V-tolerant, internal pull-down]
GPIO_14/DCLK	115	IO	GPIO_14; shared with LVTTL Display Port DCLK; [5V-tolerant, internal pull-down]
GPIO_15/DEN	116	IO	GPIO_15; shared with LVTTL Display Port DEN; [5V-tolerant, internal pull-down]
GPIO_16/DHS	117	IO	GPIO_16; shared with LVTTL Display Port DHS [5V-tolerant, internal pull-down]
GPIO_17/DVS	118	IO	GPIO_17; shared with LVTTL Display Port DVS [5V-tolerant, internal pull-down]
GPIO_18/ SCL_0(2W_Mst)	119	IO	GPIO_18; shared with TWO_WIRE Master_0 Clock [Schmitt trigger, 5V-tolerant]
GPIO_19/SDA_0(2W_Mst)	120	IO	GPIO_19; shared with TWO_WIRE Master_0 Data [Schmitt trigger, 5V-tolerant]

Free Datasheet http://www.datasheet4u.com/

Pad Name	Pin	I/O	Description
GPIO_20/SCL_1(2W_Mst)	121	IO	GPIO_20; shared with TWO_WIRE Master_1 Clock [Schmitt trigger, 5V-tolerant]
GPIO_21/SDA_1(2W_Mst)	122	IO	GPIO_21; shared with TWO_WIRE Master_1 Data [Schmitt trigger, open drain, 5V-tolerant] Requires external pull up
DDC_SCL_CH2	148	IO	DDC2Bi Channel 2 clock; [Schmitt trigger, 5V-tolerant]
DDC_SDA_ CH2	149	IO	DDC2Bi Channel 2 data; [Schmitt trigger, 5V-tolerant]
DDC_SCL_ CH1	152	IO	DDC2Bi Channel 1 clock; [Schmitt trigger, 5V-tolerant]
DDC_SDA_ CH1	153	IO	DDC2Bi Channel 1 data, [Schmitt trigger, 5V-tolerant]
UART_DI	154	IO	UART Data Input [5V-tolerant, internal pull-down]
UART_DO/BOOT[3]	155	IO	UART Data Output, Shared functions: BOOT[3] [5V-tolerant, internal pull-down]
GPIO_7/JTAG_MODE	157	IO	GPIO_7 or JTAG Boundary Scan MODE [5V-tolerant, internal pull-up]
GPIO_6/JTAG_CLK	158	IO	GPIO_6 or JTAG Boundary Scan CLK [5V-tolerant, internal pull-up]
GPIO_5/JTAG_TDI	159	IO	GPIO_5 or JTAG Boundary Scan TDI [5V-tolerant, internal pull-up]
GPIO_4/JTAG_TDO	160	IO	GPIO_4 or JTAG Boundary Scan TDO [5V-tolerant, internal pull-up]
GPIO_3/JTAG_RESET	163	IO	GPIO_3 or JTAG Boundary Scan Reset [5V-tolerant, internal pull-up]
GPIO_2	164	IO	GPIO_2 [5V-tolerant, internal pull-down]
GPIO_49	165	IO	GPIO_49 [Open drain 5V-tolerant] Requires external pull up
GPIO_48	166	IO	GPIO_48 [5V-tolerant]
RESETn	204	IO	Hardware Power-On-Reset out (active low), and reset button input. Reset pulse output of typ. 150ms.
GPIO_22/INT1	211	IO	GPIO_22; shared with Interrupt Input 1; also shared with Interrupt Out [5V-tolerant, internal pull-down]
GPIO_23/INT0	214	IO	GPIO_23; shared with Interrupt Input 0 [5V-tolerant, internal pull-down]
GPIO_0/DDC_SCL_0	230	IO	GPIO_0/DDC_SCL Shared with Two_Wire Slave (DDC2B) clock input. [Schmitt trigger, 5V-tolerant]
GPIO_1/DDC_SDA_0	231	IO	GPIO_1/DDC_SDA Shared with Two_Wire Slave (DDC2B) data i/o. [Schmitt trigger, 5V-tolerant]
PWM0/BOOT[5]	241	IO	PWM0; shared with BOOT[5]; [5V-tolerant, internal pull-down]
PWM1/BOOT[4]	242	IO	PWM1; shared with BOOT[4]; [5V-tolerant, internal pull-down]
GPO_8/PWM2/BOOT[6]	243	IO	GPO_8; shared with PWM2 output; shared with BOOT[6] input. [5V-tolerant, internal pull-down]
GPO_9/PWM3/BOOT[7]	244	IO	GPO_9/PWM3 [5V-tolerant, internal pull-down]
GPO_0	69	O	GPO. Do not connect when not used
GPO_1	70	O	GPO. Do not connect when not used
GPO_2	71	O	GPO. Do not connect when not used
GPO_3	72	O	GPO. Do not connect when not used
GPO_4	74	O	GPO. Do not connect when not used
GPO_5	75	O	GPO. Do not connect when not used
GPO_6	77	O	GPO. Do not connect when not used
GPO_7	126	O	GPO. Do not connect when not used

Free Datasheet http://www.datasheet4u.com/

Table 10: SDRAM Interface

Pad Name	Pin	I/O	Description
DQ7_A	8	IO	Data 7 for first 1Mx16 SDRAM
DQ6_A	9	IO	Data 6 for first 1Mx16 SDRAM
DQ5_A	10	IO	Data 5 for first 1Mx16 SDRAM
DQ4_A	11	IO	Data 4 for first 1Mx16 SDRAM
DQ3_A	12	IO	Data 3 for first 1Mx16 SDRAM
DQ2_A	13	IO	Data 2 for first 1Mx16 SDRAM
DQ1_A	15	IO	Data 1 for first 1Mx16 SDRAM
DQ0_A	16	IO	Data 0 for first 1Mx16 SDRAM
DQ15_A	17	IO	Data 15 for first 1Mx16 SDRAM
DQ14_A	18	IO	Data 14 for first 1Mx16 SDRAM
DQ13_A	19	IO	Data 13 for first 1Mx16 SDRAM
DQ12_A	20	IO	Data 12 for first 1Mx16 SDRAM
DQ11_A	21	IO	Data 11 for first 1Mx16 SDRAM
DQ10_A	22	IO	Data 10 for first 1Mx16 SDRAM
DQ9_A	23	IO	Data 9 for first 1Mx16 SDRAM
DQ8_A	24	IO	Data 8 for first 1Mx16 SDRAM
WE#	27	O	SDRAM write enable. This signal is active low
CAS#	28	O	SDRAM column address strobe. This signal is active low
RAS#	29	O	SDRAM row address strobe. This signal is active low
BA	31	O	SDRAM clock enable. This signal is active high
MCLK	32	O	SDRAM clock. This signal is rising edge active
A9	33	IO	SDRAM Address 9
A8	36	IO	SDRAM Address 8
A7	37	IO	SDRAM Address 7
A6	38	IO	SDRAM Address 6
A5	39	IO	SDRAM Address 5
A4	40	IO	SDRAM Address 4
A3	41	IO	SDRAM Address 3
A2	42	IO	SDRAM Address 2
A1	43	IO	SDRAM Address 1
A0	44	IO	SDRAM Address 0
A10	45	IO	SDRAM Address 10
DQ7_B	48	IO	Data 7 for second 1Mx16 SDRAM
DQ6_B	49	IO	Data 6 for second 1Mx16 SDRAM
DQ5_B	50	IO	Data 5 for second 1Mx16 SDRAM
DQ4_B	51	IO	Data 4 for second 1Mx16 SDRAM
DQ3_B	52	IO	Data 3 for second 1Mx16 SDRAM
DQ2_B	53	IO	Data 2 for second 1Mx16 SDRAM
DQ1_B	54	IO	Data 1 for second 1Mx16 SDRAM
DQ0_B	55	IO	Data 0 for second 1Mx16 SDRAM
DQ15_B	56	IO	Data 15 for second 1Mx16 SDRAM
DQ14_B	58	IO	Data 14 for second 1Mx16 SDRAM
DQ13_B	59	IO	Data 13 for second 1Mx16 SDRAM
DQ12_B	60	IO	Data 12 for second 1Mx16 SDRAM
DQ11_B	61	IO	Data 11 for second 1Mx16 SDRAM
DQ10_B	62	IO	Data 10 for second 1Mx16 SDRAM
DQ9_B	63	IO	Data 9 for second 1Mx16 SDRAM
DQ8_B	64	IO	Data 8 for second 1Mx16 SDRAM

Free Datasheet http://www.datasheet4u.com/

Pad Name	Pin	I/O	Description
DQM	68	O	SDRAM data mask

Table 11: General-Purpose LBADC

Pad Name	Pin	I/O	Description
LBADC_RTN/GND	205	AG	Analog Ground for low bandwidth ADC. This package pin is shared with Reference Feedback pad. Tie directly to system ground.
LBADC_IN3	206	AI	Analog input 3 to LB-ADC analog multiplexer
LBADC_IN2	207	AI	Analog input 2 to LB-ADC analog multiplexer
LBADC_IN1	208	AI	Analog input 1 to LB-ADC analog multiplexer
LBADC_VDD_3.3	209	AP	Analog 3.3V supply for low bandwidth-ADC. Bypass to system ground with a 0.1uF capacitor.

Table 12: SPI ROM

Pin Name	No	I/O	Description
SPI_CSn/BOOT[0]	226	IO	SPI ROM chip select Shared functions: BOOT[0]
SPI_CLK/BOOT[1]	227	IO	SPI ROM Clock output Shared functions: BOOT[1]
SPI_DI	228	IO	SPI ROM Data input
SPI_DO/BOOT[2]	229	IO	SPI ROM Data output Shared function: BOOT[2]

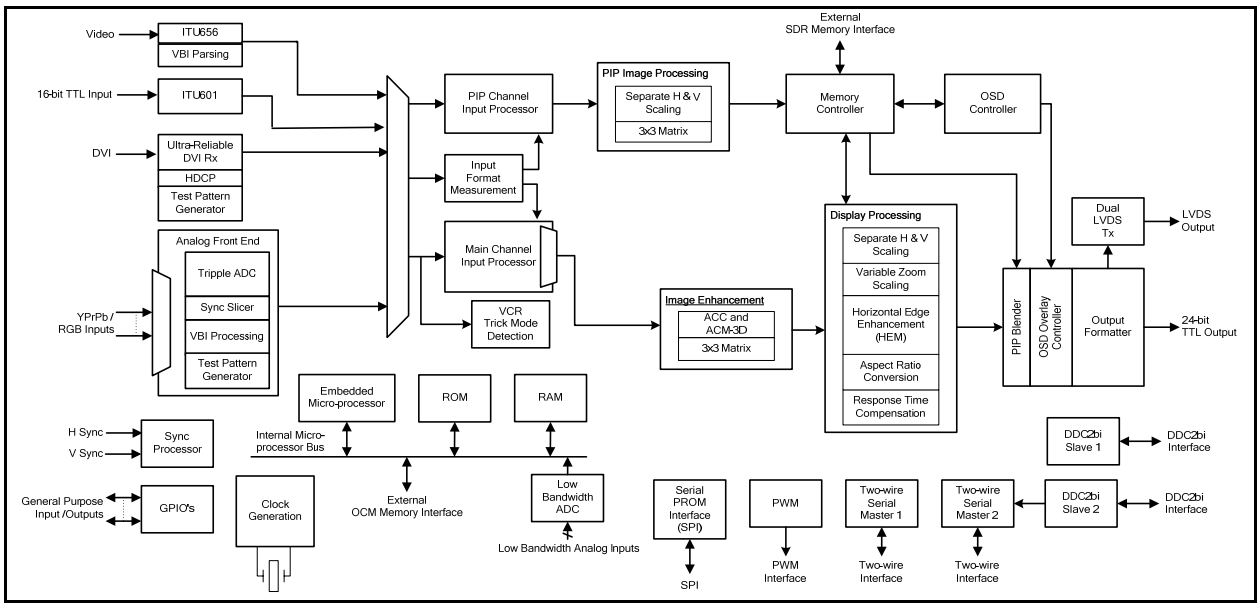
Table 13: Scan Test

Pin Name	No	I/O	Description
SCAN_EN	125	I	Scan test enable [Schmitt trigger with internal pull-down]
JTAG_BS_EN	210	I	Boundary scan test enable. 0 = no JTAG; 1 = enable JTAG functions on pins 194, 197-200. [Schmitt trigger with internal pull-down]

Free Datasheet http://www.datasheet4u.com/

4 Functional Description

Figure 3: Functional Block Diagram



4.1 Bootstrap Configuration

During hardware reset pins BOOT[7..0] are configured as inputs. On the rising edge of RESETn, the value on these pins are latched and stored. The latched values configure the hardware to certain configuration without any software interaction. These values are software readable by the on-chip microcontroller. Install a 10K pull-up resistor to indicate a '1', otherwise install a 10K pull-down resistor to indicate a '0'. This ensures correct operation under all conditions, even though these boot-strap pins have internal 60K pull-downs.

Free Datasheet http://www.datasheet4u.com/

Table 14: Bootstrap Signals

Pin	Pin Name, Signal Name	I/O	Shared with	Description
226	BOOT[0], OCM_BUS_SEL[0]	I	SPI_CSn	Interface Select. Determines the interface to control this device and configures JTAG access 00 = Internal Micro, SPI as ROM. Internal ROM on, and mapped to top 32K of OCM address range. OCM boot will be from internal ROM code. (Recommended) 01 = Internal Micro, Internal ROM is overlayed with external ROM. Internal ROM off. This is debug mode with the external ROM mapped to the entire upper 512K of the OCM address range. OCM boot will be from external ROM code. 10, 11 = Reserved for factory testing
227	BOOT[1], OCM_BUS_SEL[1]	I	SPI_CLK	See OCM_BUS_SEL[0]
229	BOOT[2], OSC_SEL	I	SPI_DO	Selection of TCLK source 0 = Xtal and internal oscillator (recommended) 1 = TTL oscillator (input on TCLK pin)
155	BOOT[3], ICD_SEL	I	UART_DO	0 = In circuit debugger is mapped onto the DDC_SCL_CH2 and DDC_SDA_CH2 pins. 1 = In circuit debugger is mapped onto the DDC_SCL_CH1 and DDC_SDA_CH1 pins.
242	BOOT[4], OCM_24BIT_ADDR_EN	I	PWM1	0 = OCM is booting in 20 bit addressing mode. 1 = OCM is booting in 24 bit addressing mode.
241	BOOT[5], TCLK_SEL[0]	I	PWM0	Checked by internal ROM firmware to select TCLK frequency. See BOOT[7] below.
243	BOOT[6], ATMEL_EN	I	GPO_8/PWM2	0 – standard SPI external memory interface; 1 – ATMEL data flash external memory interface.
244	BOOT[7], TCLK_SEL[1]	I	GPO_9/PWM3	Checked by internal ROM firmware to select TCLK frequency. TCLK_SEL[1:0] = TCLK Frequency 00 = 14.318 Mhz; 01 = 20 Mhz; 10 = 24 Mhz; 11 = 19.661 Mhz

Free Datasheet http://www.datasheet4u.com/

4.2 Chip Initialization

4.2.1 Power Sequencing

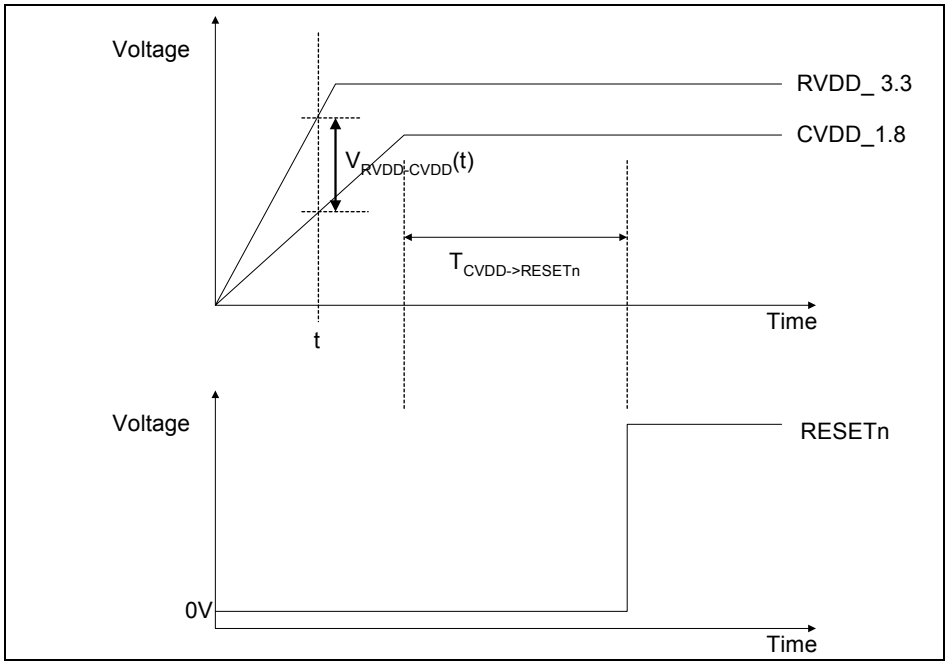
At any time during the power-up sequence the actual voltage of the ring power supply (RVDD_3.3) should always be equal to or higher than the actual voltage of the core power supply (CVDD_1.8). In mathematical terms, $V_{RVDD\_3.3} >= V_{CVDD\_1.8}$ at all times.

In addition, the system designer must ensure that the 1.8V core VDD supply must be active for at least 1ms before the rising edge of the chip RESETn signal during the chip power-up sequence. The rising edge of RESETn signal is used to latch the bootstrap configurations, so its correct timing relationship to the core VDD is critical for correct chip operation.

Table 15: Power Sequencing Requirements

Parameter	Min	Typ	Max
VRVDD-CVDD(for all t>0)	0V		
TCVDD->RESETn		100ms	

Figure 4: Correct Power Sequencing



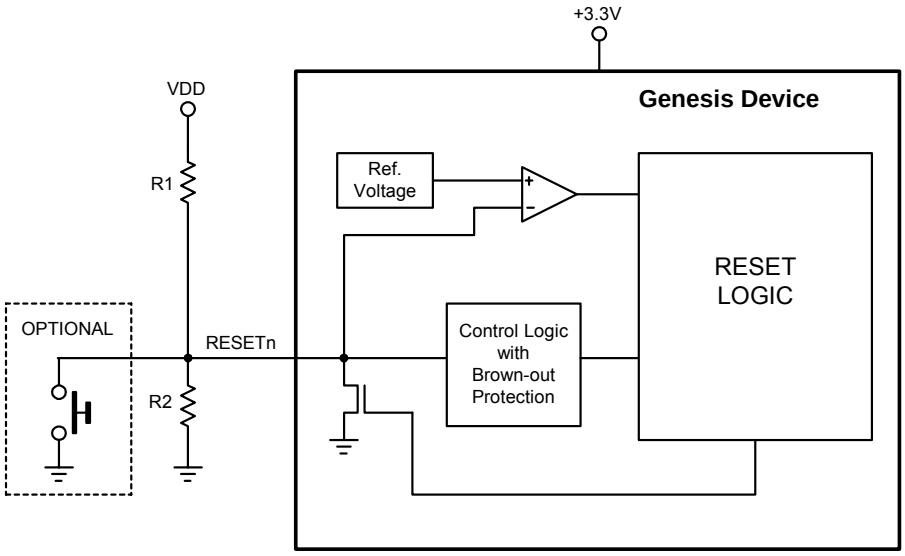
Free Datasheet http://www.datasheet4u.com/

4.2.2 Hardware Reset

This device has an integrated internal reset pulse generator, so that an external reset IC is not required.

The internal circuitry of the RESET is shown below.

Figure 5: Internal RESET Circuitry



The internal reset pulse generator performs hardware reset under the following conditions:

- During system power-up, after the RVDD_3.3 voltage has reached threshold Vt.
- In the event RVDD_3.3 voltage drops below threshold Vt for more than approximately 200ns.
- Manually holding the RESETn pin low for a minimum of 1ms.

The active-low reset pulse on RESETn pin generated by the internal reset pulse generator is around 100ms in duration. TCLK input must be applied during and after the reset. When the reset period is complete, and RESETn state becomes high, and the reset sequence is as follows:

1. Reset all registers of all types to their default state (this is 00h unless otherwise specified in the Register Listing).

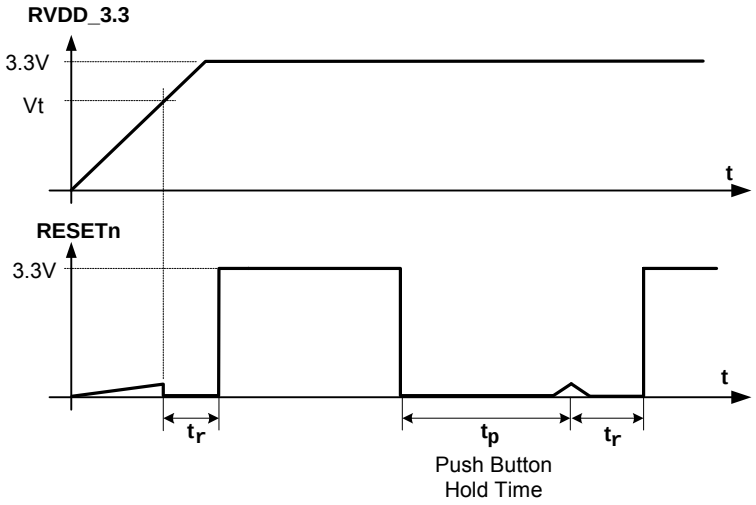
2. Force each clock domain into reset. This continues for 64 local clock domain cycles following the de-assertion of RESETn.

3. Operate the OCM_CLK domain at the TCLK frequency.

The following figure shows the relationship between AVDD_3.3V and RESETn during system power-up.

Free Datasheet http://www.datasheet4u.com/

Figure 6: Power-up Reset Sequence Between RVDD_3.3 and RESETn Pin



NOTE: Vt is the power-up reset threshold voltage, Tr is the reset pulse duration, and Tp is the push-button hold time (the duration of holding RESETn pin low).

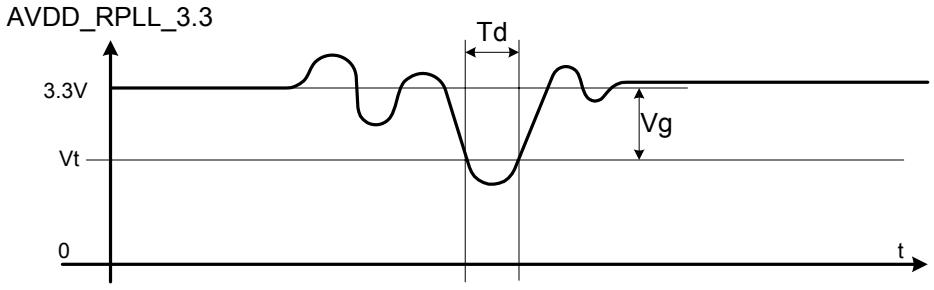
The power-on reset specifications are listed in the following table.

Table 16: Power-On Reset Specification

Description	Symbol	Min.	Typical	Max
Power-on reset threshold voltage	Vt	2.10V	2.20V	2.40V
Reset pulse duration	Tr	80ms	100ms	120ms
Push-button hold time	Tp	1ms		

There is a glitch filter in the internal reset pulse generator that ignores the RVDD_3.3 power line glitch if the glitch duration is shorter than approximately 200ns, regardless of the magnitude of the glitch. However, if RVDD_3.3V voltage drops below the threshold Vt for more than 200ns, reset will be asserted: RESETn will become low. The following figure illustrates the RVDD_3.3V glitch.

Figure 7: Reset Power Supply Glitch



Td = Duration of dip glitch at V_t
Vg = Amplitude of dip glitch

Free Datasheet http://www.datasheet4u.com/

Table 17: RVDD_3.3V Glitch-Induced Reset Specifications

Description	Symbol	Min.	Typical	Max
RVDD_3.3V glitch duration	Td	200ns		
RVDD_3.3V glitch amplitude	Vg	0.9V*		1.2V*

* The RVDD_3.3V voltage must fall by more than Vg below the supply voltage (3.3V nominal) for the reset to assert (RESETn becomes low). For example, RVDD_3.3V voltage level must fall below at least 2.4V (3.3V – 0.9V) in order for reset to assert.

4.3 Clock Generation

This device is designed to use a single crystal. All internal clocks required for the operation of the chip are generated internally using analog and digital PLL's . The PLL's use TCLK as a reference frequency. TCLK is generated using an external crystal with the chip's internal oscillator.

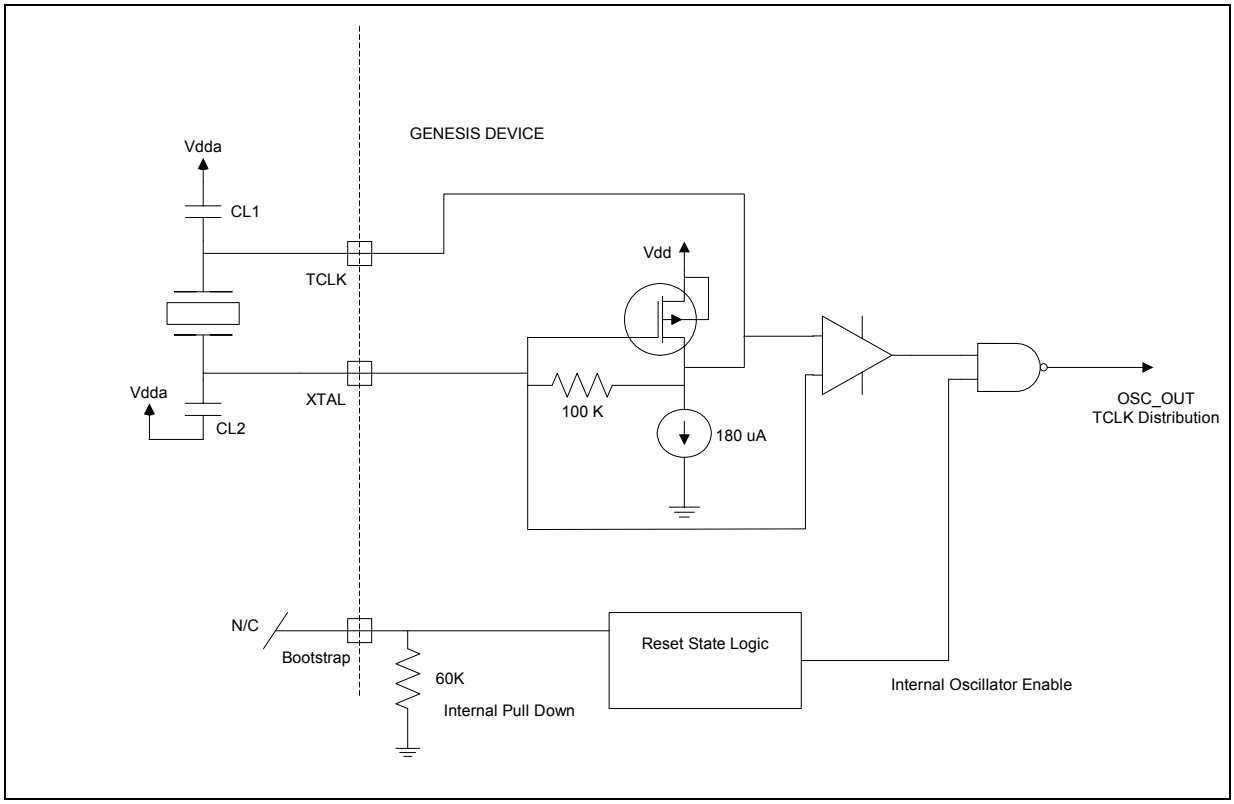
4.3.1 Using the Internal Oscillator with External Crystal

The oscillator circuit is designed to provide a very low jitter and very low harmonic clock to the internal circuitry of the chip. An Automatic Gain Control (AGC) circuit is used to insure startup and operation over a wide range of conditions. The oscillator circuit also minimizes the overdrive of the crystal to reduce the aging of the crystal.

When the internal oscillator is enabled a crystal resonator is connected between TCLK and the XTAL with the appropriately sized loading capacitors C_{L1} and C_{L2}. The size of C_{L1} and C_{L2} are determined from the crystal manufacturer's specification and by compensating for the parasitic capacitance of the Genesis device and the printed circuit board traces. The loading capacitors are terminated to the analog VDD power supply. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to ground, thus minimizing TCLK jitter.

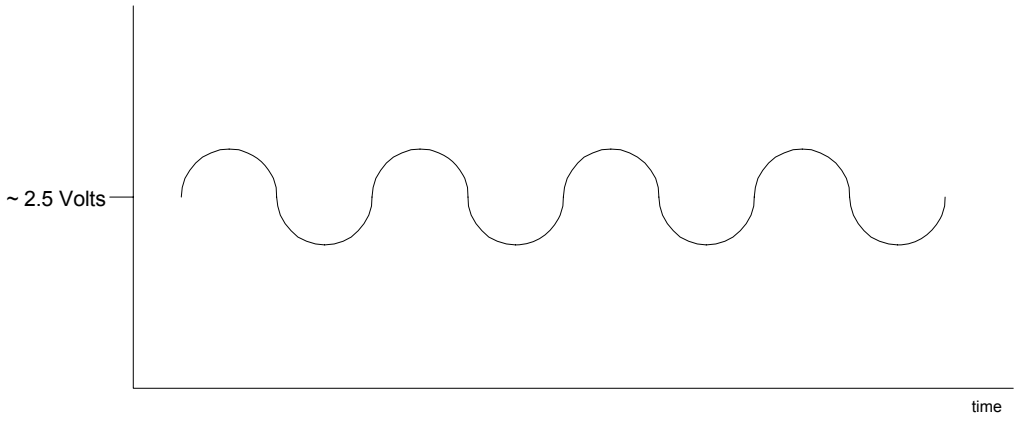
Free Datasheet http://www.datasheet4u.com/

Figure 8: Using the Internal Oscillator with External Crystal



The TCLK oscillator uses a Pierce Oscillator circuit. The output of the oscillator circuit, measured at the TCLK pin, is an approximate sine wave with a bias of about 2 volts above ground. The output of the oscillator is connected to a comparator that converts the sine wave to a square wave. The comparator requires a minimum signal level of about 50-mV peak to peak to function correctly. The output of the comparator is buffered and then distributed to the internal circuits.

Figure 9: Internal Oscillator Output



Free Datasheet http://www.datasheet4u.com/

4.3.2 Clock Synthesis

All internal clocks required for proper chip operation are synthesized internally within the gm5862H.

1. Main Timing Clock (TCLK) is the output of the chip internal crystal oscillator. TCLK is derived from the TCLK/XTAL pad input. Max = 24MHz
2. Reference Clock (RCLK) synthesized by RCLK PLL using TCLK or EXTCLK as the reference. This clock is used as a reference clock in generating most of the internal frequencies. It is important that this clock is stable with very low jitter. Factory recommended frequency is 200MHz.
3. Input Source Clock (SDDS_CLK) synthesized by SDDS PLL using input HS as the reference. The SDDS uses RCLK as a reference clock to drive its internal digital logic. Max = 195MHz.
4. DVI Output Clock (DVI_CLK) synthesized by DVI receiver PLL using RC+/RC-as the reference. DVI Clock Max = half 165 MHz.
5. Digital Input Clock Domain for ITU656 video input (DIP_CLK). Max = 80MHz
6. Digital input Clock Domain for ITU601 input (ITU601_CLK). Single edged maximum = 74.25MHz and Dual edge Maximum = 148.5MHz
7. Fixed Frequency Clock (FCLK) synthesized by FDDS. Used as Host Interface and On-chip Micro-controller Clock (OCM_CLK). Max = 100MHz
8. Memory Clock synthesized by MDDS. Used as MEMC_CLK domain driver. Also typically drives the LBUF_CLK. Max = 187 MHz.
9. Display Clock (DDDS_CLK) synthesized by DDDS PLL using IMP_CLK as the reference. The IMP_CLK is the clock from the selected main channel video source. The DDDS also uses the RCLK to drive internal digital logic.

4.4 Analog Input Port (AIP)

The AIP support dual analog inputs with separate sets of Hsync, Vsync and Composite/SOG inputs. An integrated mux selects which set of analog inputs connect to the integrated ADC.

Analog Front End is responsible for selecting and capturing the desired analog input graphics/video stream. The ADC can be used to sample analog signals in RGB as well as the YPbPr color space, in which case the digital color controls are used to convert these signals back to the RGB color domain for display on the LCD panel.

When a source is a video input stream (YPbPr) the AIP directs inputs through an analog multiplexer to integrated anti-alias filters before the analog to digital conversion (ADCs). These integrated features eliminate the need for any external devices (anti-alias-filters, analog multiplexers) between the input connector and the analog input port.

Free Datasheet http://www.datasheet4u.com/

The AIP block also contains the sync processor block which processes digital separate and digital composite syncs. For processing SOG/SOY signals the Analog Sync Extractor, within the ADC block is utilized.

The VBI section of the AIP block extracts and decodes the VBI data from the analog data stream. This data is sent to the internal On-chip Microcontroller for further processing.

4.4.1 Analog to Digital Converter (ADC)

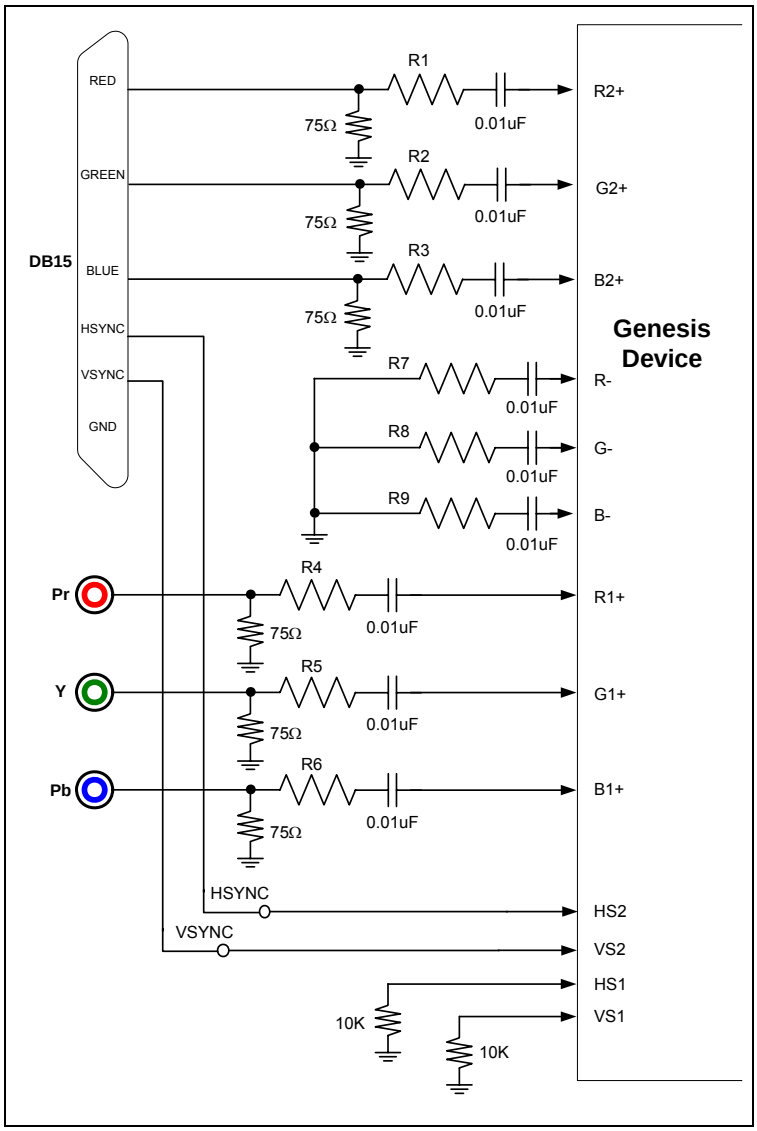
The following section describes analog RGB signal connections.

Table 18: Pin Connection for RGB Input with HSYNC/VSYNC

Pin Name	ADC Signal Name
RED1+	Red/Pr Channel 1
RED2+	Red/Pr Channel 2
GREEN1+	Green/Y Channel 1
GREEN2+	Green/Y Channel 2
BLUE1+	Blue/Pb Channel 1
BLUE2+	Blue/Pb Channel 2
RED-	Terminate as illustrated in the figure below.
GREEN-	Terminate as illustrated in the figure below.
BLUE-	Terminate as illustrated in the figure below.
HSYNC	Horizontal Sync. Terminate as illustrated in the figure below.
VSYNC	Vertical Sync. Terminate as with HSYNC illustrated in the figure below.

Free Datasheet http://www.datasheet4u.com/

Figure 10: Example ADC Signal Terminations



It is important to follow the recommended layout guidelines for graphics signal interfacing from compatible sources (see the system layout guidelines).

4.4.2 Schmitt Trigger

Integrated Schmitt triggers are used for improving the rising and falling edges of the analog Horizontal and Vertical Sync signals. This eliminates the need for using external Schmitt components in the system design. Typical behavior of an integrated Schmitt circuit is shown in the following figure. The integrated Schmitt circuit has 2 sets of threshold voltages for ViH and ViL, which together allows four different hysteresis levels. The Schmitt threshold levels of integrated circuits are in compliance with standard CMOS and TTL input signals. A programmable option is provided in the software for the selection of Schmitt levels.

Free Datasheet http://www.datasheet4u.com/

Figure 11: Schmitt Circuit Timing Diagram

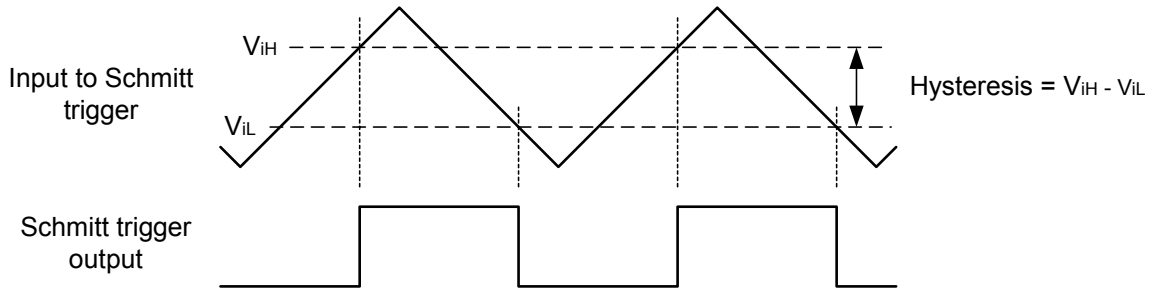


Table 19: Schmitt Circuit Thresholds

Description	Programmed Threshold Level	Static Thresholds (measured with a DC voltage)			Dynamic Thresholds (10KHz triangular waveform)		
		Min	Typ	Max	Min	Typ	Max
Low-to-High	Vih[V] = 2.5	2.16	**2.5**	2.64	2.06	**2.34**	2.62
	Vih[V] = 2.0	1.82	**1.99**	2.16	1.72	**1.92**	2.1
High-to-Low	Vil [V] = 1.5	1.3	**1.5**	1.84	1.1	**1.36**	1.58
	Vil [V] = 0.8	0.74	**0.8**	0.91	0.52	**0.6**	0.73

4.4.3 DC Restoration

The various analog inputs generated from different graphics sources may have DC offsets. It is necessary to remove the DC offsets by AC coupling these signals through capacitive filters as recommended in the earlier diagram. Analog Front End provides means to remove DC offsets so that the entire dynamic range of the ADC can be fully utilized. Typically, this is achieved by clamping the input signal during the horizontal back porch region. Full control over any such clamping pulse is provided so that the position and size can be controlled via programmable registers.

4.4.4 Sync Extraction

The composite sync pattern may be input on either the HSync input pin or be embedded into GREEN channel. An internal sync stripper is responsible for extracting composite sync signals or SOG signals. Input measurement circuitry is used to determine the polarity and whether the sync signals are separate Hsync / VSync, composite sync or Sync-on-Green.

This device has the capability to support the following types of SOG and CSYNC inputs without having to use external components. The signals below show the negative types of SOG and CSYNC signals (positive types are also supported).

Free Datasheet http://www.datasheet4u.com/

4.4.5 ADC Characteristics

Table 20: ADC Characteristics

	MIN	TYP	MAX	NOTE
Track & Hold Amp Bandwidth			290 MHz	Guaranteed by design. Note that the Track & Hold Amp Bandwidth is programmable. 290 MHz is the maximum setting.
Full Scale Adjust Range at RGB Inputs	0.55 V		0.90 V	
Full Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output. Independent of full scale RGB input.
Zero Scale Adjust Sensitivity		+/- 1 LSB		Measured at ADC Output.
Sampling Frequency (Fs)	13.5 MHz		205 MHz	
Differential Non-Linearity (DNL)		+/-0.5 LSB	+/-0.9 LSB	Fs = 205 MHz
No Missing Codes				Guaranteed by test.
Integral Non-Linearity (INL)		+/- 1.5 LSB		Fs = 205 MHz
Channel to Channel Matching		+/- 0.5 LSB		

Input formats with resolutions or refresh rates higher than that supported by the LCD panel are displayed as recovery modes only. This is called RealRecovery™. For example, it may be necessary to shrink the image. This may introduce image artifacts. However, the image is clear enough to allow the user to change the display properties.

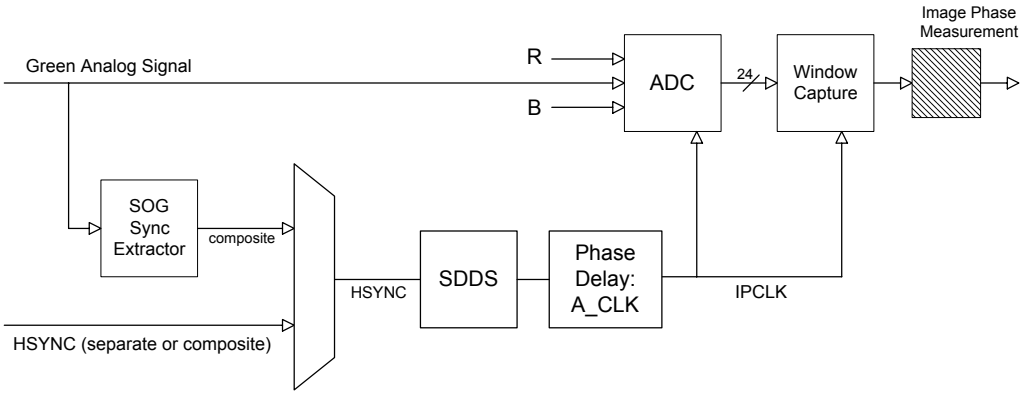
The ADC has a built in clamp circuit for AC-coupled inputs. By inserting series capacitors (~10 nF), the DC offset of an external video source can be removed. The clamp pulse position and width are programmable.

4.4.6 Clock Recovery Circuit

The Source Direct Digital Synthesis (SDDS) clock recovery circuit generates the clock used to sample analog RGB data (IP_CLK or source clock). This circuit is locked to the HSYNC of the incoming video signal.

Patented digital clock synthesis technology makes the clock circuits resistant to temperature/voltage drift. Using Direct Digital Synthesis (DDS) technology, the clock recovery circuit can generate any IP_CLK clock frequency within the range of 25MHz to 205MHz.

Figure 12: Clock Recovery



Free Datasheet http://www.datasheet4u.com/

4.4.7 Sampling Phase Adjustment

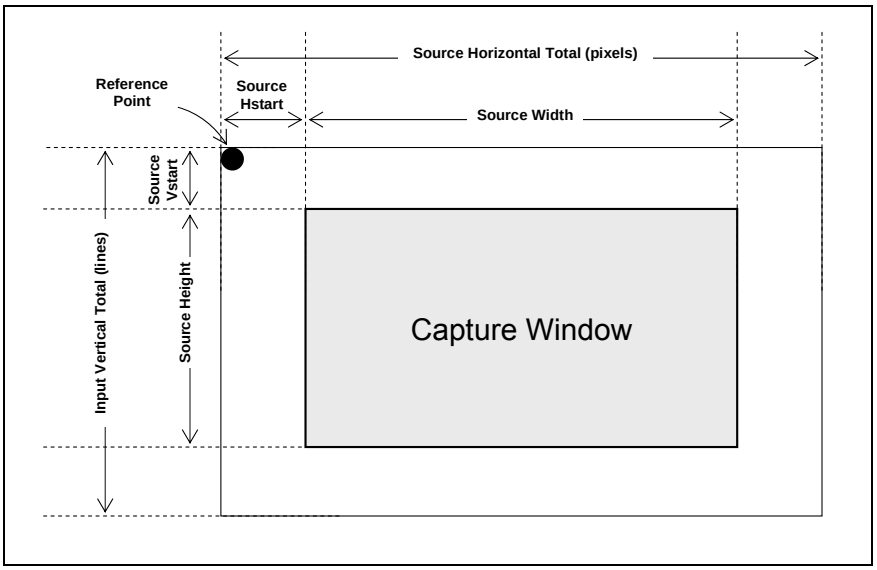
The programmable ADC sampling phase is adjusted by delaying the SDDS clock with respect to the HSYNC input. The accuracy of the sampling phase is checked and the result is read from a register. This feature enables accurate auto-adjustment of the ADC sampling phase.

4.4.8 ADC Capture Window

The capture window is defined by IP_CLKs (equivalent to a pixel count) in the horizontal direction, and defined by lines in the vertical direction. All parameters beginning with "Source" are programmed registers values.

NOTE: The Input Vertical Total is determined solely by the input and is not a programmable parameter.

Figure 13: ADC Capture Window



The Reference Point in the ADC Capture Window figure marks the leading edge of the first internal HSYNC following the leading edge of an internal VSYNC. Both the internal HSYNC and the internal VSYNC are derived from external HSYNC and VSYNC inputs.

Horizontal parameters are defined in terms of single pixel increments relative to the internal horizontal sync. Vertical parameters are defined in terms of single line increments relative to the internal vertical sync.

ADC interlaced inputs may be programmed to automatically determine the field type (even or odd) from the VSYNC/HSYNC relative timing. For more information see the Input Format Measurement section.

Free Datasheet http://www.datasheet4u.com/

4.5 Digital Visual Interface (DVI) Input Port

The Ultra-Reliable DVI™ receiver block is compliant with DVI 1.0 single link specifications. Digital Visual Interface (DVI) is a standard. This block supports an input clock frequency ranging from 20 MHz to 165 MHz.

4.5.1 DVI Receiver Characteristics

Table 21: DVI Receiver Characteristics

	MIN	TYP	MAX	NOTE
DC Characteristics				
Differential Input Voltage	150mV		1200mV	
Input Common Mode Voltage	AVDD –300m V		AVDD -37mV	
Behavior when Transmitter Disable	AVDD -10mV		AVDD +10mV	
AC Characteristics				
Input clock frequency	20 MHz		165 MHz	
Input differential sensitivity (Peak-to-peak)	150mV			
Max differential input (peak-to-peak)			1560 mV	
Allowable Intra-Pair skew at Receiver			250 ps	Input clock = 160 MHz
Allowable Inter-Pair skew at Receiver			4.0 ns	

It is important to follow the recommended layout guidelines for these signals.

4.5.2 High-Bandwidth Digital Content Protection (HDCP)

The HDCP system allows authentication of a video receiver by a video transmitter, decryption of transmitter-encoded video data by the receiver, and periodic renew-ability of authentication during transmission. The circuitry is implemented to allow full support of the HDCP 1.0 protocol for DVI inputs.

For enhanced security, Genesis provides a means of storing and accessing the secret key given to individual monitor units in an encrypted format.

Further details of the protocol and theory of the system can be found in the High-bandwidth Digital Content Protection System specification (see www.digital-cp.com).

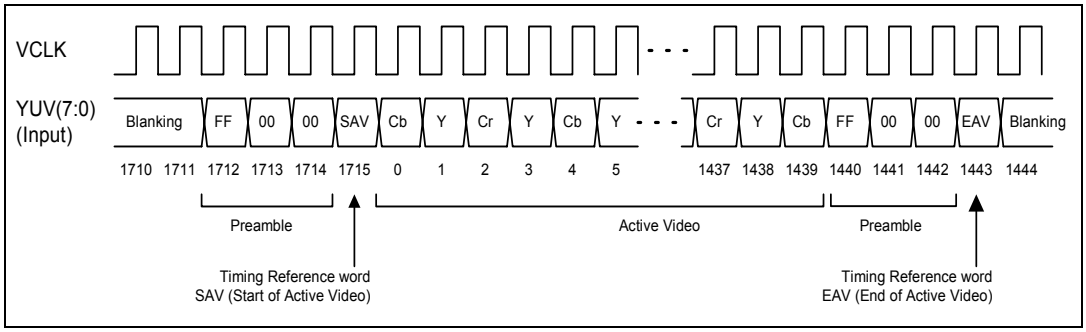
4.6 Video Input Port for ITU656 Sources (VIP)

The Digital Input Port supports ITU656 digital video format. The VIP connects to commercially available NTSC or PAL video decoders. ITU-BT656 video format consists of pixel clock and 8-bits of data. The VIP port allows for MSB – LSB data swapping to facilitate interfacing to a variety of external video decoders. It has also a built in programmable clock delay circuitry to compensate for timing skew between the video clock and the data, which would otherwise cause undesirable noise on the screen.

No separate HSYNC, VSYNC signals are required. The internal 656 decoder extracts these from the embedded timing data as shown below.

Free Datasheet http://www.datasheet4u.com/

Figure 14: ITU-R BT656 Input



YCbCr input is always automatically clamped to restrict the input data to ITU-R BT601 levels:

- Y Bottom clamping: Y data < 16 is clamped to 16
- Y Top clamping: Y data >235 is clamped to 235
- CbCr Bottom clamping: CbCr data < 16 is clamped to 16
- CbCr Top clamping: CbCr data > 240 is clamped to 240

4.7 16-bit TTL Input

This TTL input supports 16-bit 4:2:2 YCbCr or YPbPr format.

Figure 15: 8-bit 4:2:2 YCbCr/YPbPr

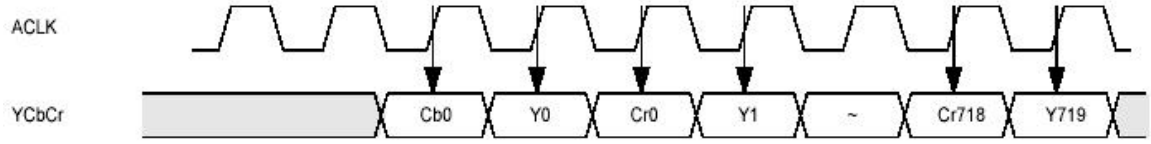
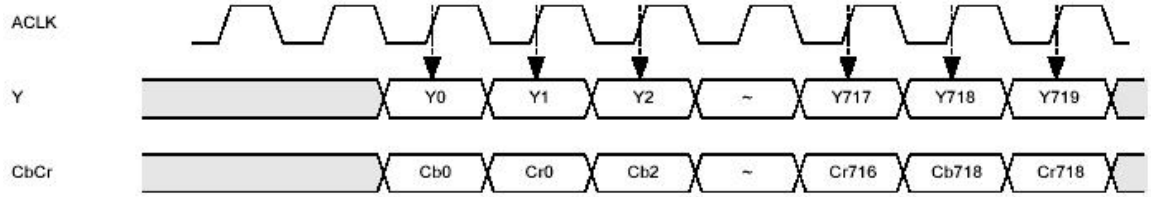


Figure 16: 16-bit 4:2:2 YCbCr/YPbPr



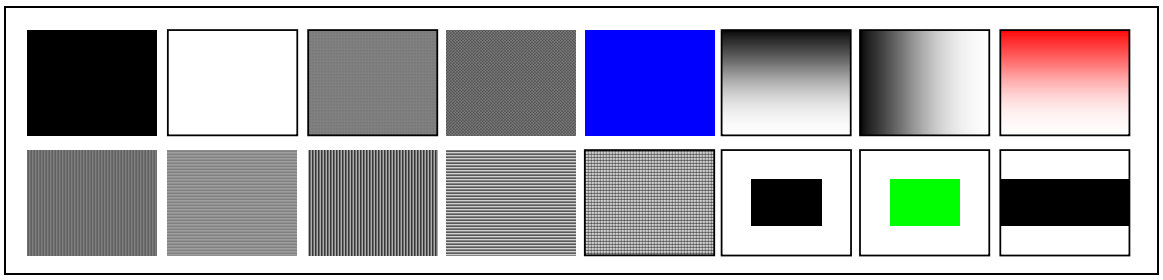
4.8 Test Pattern Generator (TPG)

Once programmed, the integrated test pattern generator can replace a video source (e.g. a PC) during factory calibration and test. This simplifies the test procedure and eliminates the possibility of image noise being injected into the system from the source. Foreground and background colors are programmable, and the OSD controller can be used to produce other patterns. It can be also used as a diagnostic tool during product development.

Free Datasheet http://www.datasheet4u.com/

Each input block is equipped with its own TPG. The TPG within the Analog Input Block (AIP) can operate in free-run stand alone mode without any external source connected. The DVI and the VIP ports require a source with a valid timing to be connected. The timing of the input source is used for correct output timing generation, while displaying the selected test pattern.

Figure 17: Built-in Test Pattern Examples



4.9 Input Format Measurement

Input Format Measurement (IFM) is provided on both Main and PIP channels. The IFM block provides the capability of measuring the horizontal and vertical timing parameters of the input video source (HS/VS period, pulse duration, polarity, number of vertical lines within the input field/frame etc.). This information is used to determine the input graphics/video format and to detect any changes in the input format, therefore facilitating mode setup. It is also capable of detecting the field type of interlaced video formats.

Horizontal measurements are measured in terms of the selected IFM_CLK (either TCLK or RCLK/4), while vertical measurements are measured in terms of HSYNC pulses (number of lines).

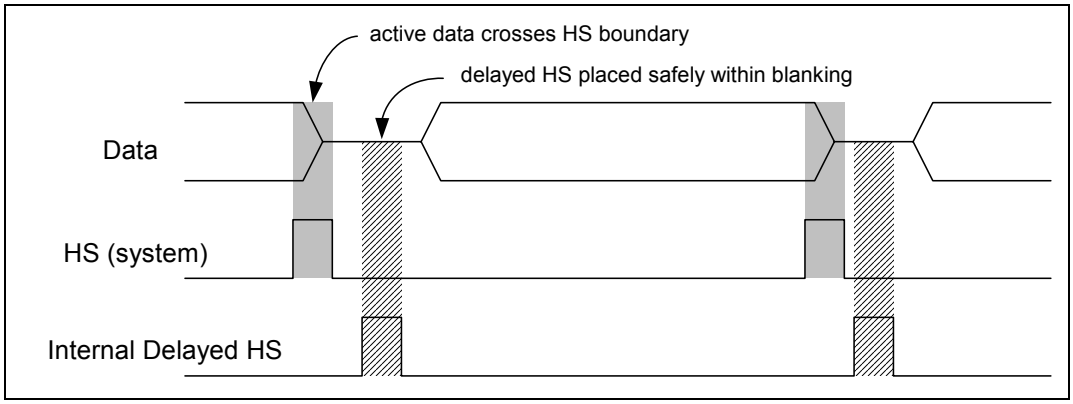
The IFM features a programmable reset, separate from the regular soft reset. This reset disables the IFM, reducing power consumption. The IFM is capable of operating during power down mode.

4.10 HSYNC / VSYNC Delay

The active input region captured is specified with respect to internal HSYNC and VSYNC. By default, internal syncs are equivalent to the HSYNC and VSYNC at the input pins and thus force the captured region to be bounded by external HSYNC and VSYNC timing. However, an internal HSYNC and VSYNC delay feature removes this limitation. The HSYNC and VSYNC delay is used for image positioning of ADC input data. HSYNC is delayed by a programmed number of selected input clocks, while the VSYNC is delayed by a programmed number of selected input lines.

Free Datasheet http://www.datasheet4u.com/

Figure 18: Active Data Crosses HSYNC Boundary



4.11 Horizontal and Vertical Measurement

The IFM is able to measure the horizontal period and active high pulse width of the HSYNC signal, in terms of the selected clock period (either TCLK or RCLK/4.). Horizontal measurements are performed on only a single line per frame (or field). The line used is programmable. It is able to measure the vertical period and VSYNC pulse width in terms of rising edges of HSYNC. Once enabled, measurement begins on the rising VSYNC and is completed on the following rising VSYNC. Measurements are made on every field / frame until disabled.

4.12 Format Change Detection

The IFM is able to detect changes in the input format relative to the last measurement and then alert both the system and the on-chip microcontroller. The microcontroller sets a measurement difference threshold separately for horizontal and vertical timing. If the current field / frame timing is different from the previously captured measurement by an amount exceeding this threshold, a status bit is set. An interrupt can also be programmed to occur.

4.13 IFM Watchdog

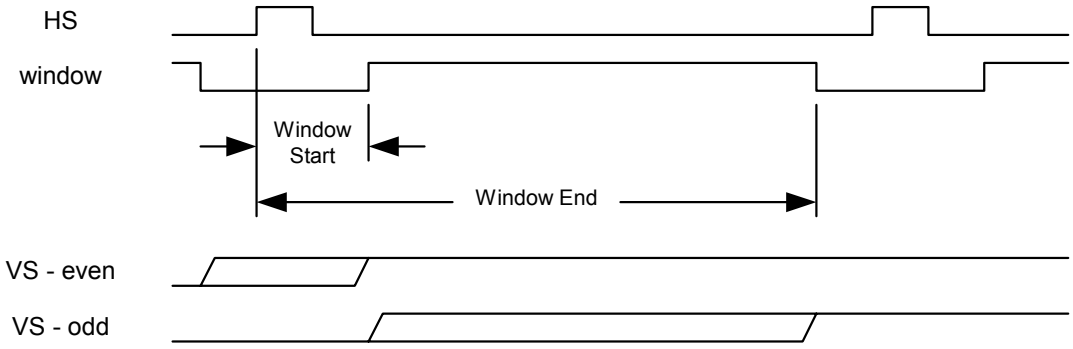
The watchdog monitors input VSYNC and HSYNC. When any HSYNC period exceeds the programmed timing threshold (in terms of the selected IFM_CLK), the counter times out indicating loss of sync. When any VSYNC period exceeds the programmed timing threshold (in terms of HSYNC pulses), the VSYNC watchdog counter times out indicating loss of sync. Both of these events set individual register bits. The time-out status can be read by the OCM, or an interrupt can also be programmed to occur under this condition.

Free Datasheet http://www.datasheet4u.com/

4.14 Internal Odd/Even Field Detection

The IFM has the ability to perform field decoding of interlaced inputs to the ADC. The user specifies start and end values to outline a "window" relative to HSYNC. If the VSYNC leading edge occurs within this window, the IFM signals the start of an ODD field. If the VSYNC leading edge occurs outside this window, an EVEN field is indicated (the interpretation of odd and even can be reversed). The window start and end points are selected from a predefined set of values.

Figure 19: ODD/EVEN Field Detection



4.15 Input Pixel Measurement

Pixel measurement functions are provided to assist in configuring system parameters such as pixel clock, SDDS sample clocks per line and phase setting, centering the image, or adjusting the contrast and brightness.

4.16 Image Boundary Detection

Image boundary detection is used when programming the Active Window and centering the image. Functions perform measurements on the incoming data to determine the image boundary. This information is then used for correctly positioning the image on the display.

4.17 Image Auto Balance

Image auto balance functions perform MIN and MAX pixel value measurements on the input data that is used to set up the ADC for maximum dynamic luminance range, while ensuring that gray scales are properly displayed on the display, without white-clipping.

Free Datasheet http://www.datasheet4u.com/

4.18 Instant Auto™

Instant Auto (patent-pending) is a new auto image adjustment technology from Genesis Microchip. It automatically configures frequency and phase based on the features of the incoming video signal.

Instant Auto advantages:

- Performs auto adjustments faster and more accurately than current conventional methods.
- Performs auto adjustments on full width and partial width images.
- Performs auto adjustments on DOS screens and moving images such as screen savers and motion pictures.

For further information, refer to the *Instant Auto Application Brief* (C5621-APB-01).

4.19 Intelligent Image Processing

4.19.1 Horizontal and Vertical Shrink

To preserve memory bandwidth, in certain situations a shrink function may be performed on the input data, prior to sending this data to the SDRAM. This is an arbitrary horizontal/vertical reduction to between (50% + 1 pixel/line) to 100% of the input. For example, this allows UXGA 1600x1200 pixels to be displayed as SXGA 1280x1024. This is useful to allow the user to use Windows Display Properties to reduce the screen resolution if it is higher than that of the display.

4.19.2 Variable Zoom Scaling

The scaling engine uses an advanced multi-tap, non-linear scaling engine, which uses FIR filter technique and can accept nearly any input resolution and can scale it to any output resolution, in a range from one-half reduction to a 256-fold expansion. Scaling is highly configurable, with options to scale in both horizontal and vertical directions with different methods. The scalar must scale nearly any signal input to accommodate nearly any panel input. Moreover, it provides high quality scaling of real time video and graphics images. An input field/frame is scalable in both the vertical and horizontal dimensions.

Interlaced fields may be spatially de-interlaced by vertically scaling and repositioning the input fields to align with the output display's pixel map.

4.19.3 Programmable Sharpening Filter

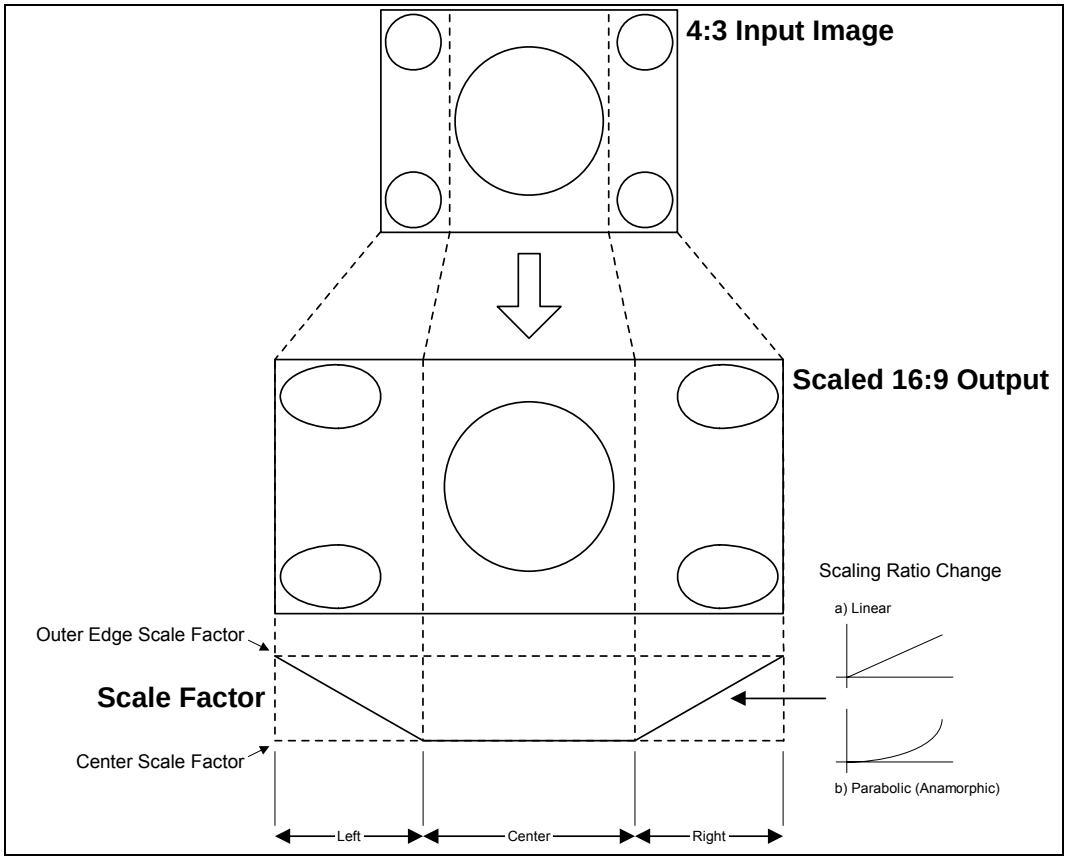
The coefficients used in the scaling engine are programmable and can be used to perform sharpening. For example, font edges can be enhanced in text or spreadsheet applications, or motion video images can be sharpened. This is available at any scale factor, or when scaling is not required (i.e. 1:1 mode).

Free Datasheet http://www.datasheet4u.com/

4.19.4 Non-linear Scaling (Panoramic)

The input image is separated into three zones horizontally; left, center and right. The center zone is scaled at a programmable fixed ratio. The left and right zones have a programmable changing scale factor that changes from left to right. The function of scale ratio change can either be linear or parabolic. This feature is available on the main channel only.

Figure 20: Non-Linear Scaling of a 4:3 to 16:9 aspect ratio conversion



4.19.5 Format and Aspect Ratio Conversion

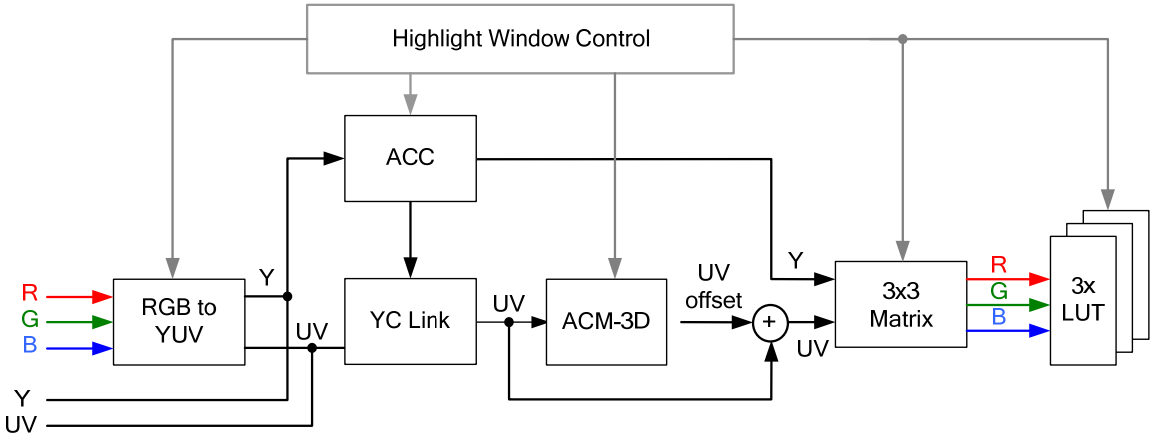
This device incorporates zoom/shrink scalers use an advanced scaling technique proprietary to Genesis Microchip Inc., providing simultaneous high quality scaling of real time video and graphics images on both channels. An input field/frame is scalable arbitrarily in both the vertical and horizontal dimensions.

Free Datasheet http://www.datasheet4u.com/

4.20 Advanced Digital Color Controls

The digital color controls consist of the components shown in the following figure.

Figure 21: Digital Color Controls Data Path



4.20.1 Adaptive Contrast and Color (ACC)

Most video content is tailored for display on CRTs or in movie theatres. However, CRT monitors have a wider dynamic range than LCD monitors. Therefore, it is desirable to enhance the luminance and chrominance dynamic range when video is displayed using LCD monitors.

ACC enhances the contrast of the image to account for this. This makes dark pixels darker and bright pixels brighter, thus enhancing the overall contrast of the image. In addition, the contrast enhancement is adaptive. This is done by calculating the running average of the luminance content of several images, divided up into multiple luminance ranges (comprising a histogram). This histogram is then used to select the weighting coefficients for the corresponding user programmable transfer functions. The running average may be applied over a programmable number of frames. ACC can be applied within a highlight window or over the full display area.

This allows for creating variety of Theme Modes than can be used for different viewing preferences and can be used to differentiate among different product brands.

4.20.2 Active Color Management 3D (ACM-3D)

Active Color Management Three Dimension provides six axis color controls to give stunning color quality. It provides control of global color parameters like hue, saturation and contrast, and local color changes such as skin tone adjustment, green enhance, or blue stretch without effecting overall color of the picture. It can be applied within a highlight window or over the full display area.

Free Datasheet http://www.datasheet4u.com/

4.20.3 3x3 Matrix

The purpose of the 3x3 matrix is to convert the YUV color space back into RGB color space after ACC/ACM processing. The 3x3 matrix also allows for implementation of global contrast, brightness as well as TV-style hue and saturation adjustments via on-screen-display menus. There are two 3x3 Matrix blocks available, one for the Main and one for the PIP channel.

Since it is also possible that the color space inside and outside of the highlight window is different, two sets of coefficients are provided for proper conversion to the RGB color space: one for inside and one for outside of the highlight window. This feature is available for the main channel only.

4.20.4 Color Standardization and sRGB Support

Internet shoppers may be very picky about what color they experience on the display. RealColor™ digital color controls can be used to make the color response of an LCD monitor compliant with standard color definitions, such as sRGB. sRGB is a standard for color exchange proposed by Microsoft and HP (see www.srgb.com). RealColor controls can be used to make LCD monitors sRGB compliant, even if the native response of the LCD panel itself is not. For more information on sRGB compliance using Genesis devices please refer to the sRGB application brief C5115-APB-02A.

4.20.5 Video Windowing

Often video content (e.g. movie from DVD) is displayed in a portion of the display while the operating system's desktop appears in the remainder. In this case it is desirable to have different color controls in the various regions of the display. For example, the user may desire that the desktop is sRGB compliant while performing hue or saturation adjustments in the region containing the video content. To perform such adjustments the 3x3 color controls and the gamma tables may be separately controlled inside and outside a defined rectangle. The coordinates of the rectangle may be provided by the operating system (and communicated using DDC2Bi) or selected by the user (using the OSD).

4.21 Video Enhancement

4.21.1 Enhancement Filters

This device provides image enhancement filters to enhance high frequency components in the video processing channel. Different levels of sharpening can be implemented by selecting different programmable coefficients for the horizontal sharpening filters.

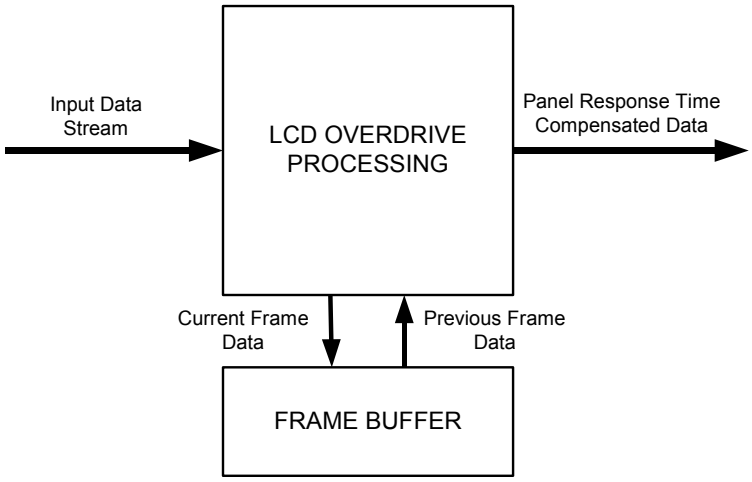
4.21.2 LCD Response Time compensation

Liquid crystal material speeds differ between panels and the technologies of driving each panel vary, a unique Look Up Table (LUT) is required for each panel for optimum response time calibration. The LCD overdrive processor is a recursive

Free Datasheet http://www.datasheet4u.com/

technology based compensation for poor liquid crystal response time. This is to prevent smearing of video images which require image change response times at the same or faster rate than that of the incoming video frame rate of 50 or 60 Hz. Based on the measurement of the LCD panel chosen for the display, a look up table will be generated for every type of panel. This look up table is calibrated for each individual panel to create a unique compensation for each different LCD panel

Figure 22: LCD Response Time Compensation



4.22 External Memory Interface

The external memory interface controls the access to the Single Data Rate (SDR) SDRAM for the PIP display window, the frame rate converter, Response Time Compensator and Aspect Ratio Converter. An arbitrator controls the write and read operations based on the status of the FIFOs present at each read and write channel, ensuring that underflow of FIFOs do not occur. Adequate depths of the FIFOs ensure no overflow occurs. 32Mbits of SDRAM memory is required for full functionality of the chip. The external memory interface supports one or two 1M x 16 SDR SDRAMs. The external memory interface supports SDRAM operation speeds up to 187MHz.

Please refer to application note C5961-APN-01. This application note covers details about different video features and image enhancements that can be enabled depending on the external memory configurations (memory capacity, speed and bandwidth), input and output resolutions.

4.22.1 Supported SDR Devices

This device operates seamlessly with commercially available 1Mx16 SDR SDRAM and 2Mx32 SDRAM devices operating at 187MHz.

Free Datasheet http://www.datasheet4u.com/

4.22.2 Adjustable Frame Store Interface Parameters

A full set of registers is provided to optimize the timing parameters for a particular memory interface. Most will not require adjustment as the process of initialization is automated.

4.23 Frame Rate Conversion

Frame rate conversion is required when there is a difference between the refresh rates between the main and the PIP channels. In such cases the frame rate of the PIP channel is frame rate converted to match that of the main channel. Another example of the FRC is when the displaying panel can't support the frame rate of the incoming video. For example a source with a vertical refresh rate of 75Hz, in order to be properly displayed on a panel that can support a max of 60Hz refresh rate, must be frame rate converted to 60Hz rate.

NOTE: All other features are disabled if there is frame rate conversion required in the MAIN channel.

4.24 Picture-in-Picture – PIP Channel Processing

This device allows a flexible picture-in-picture (PIP) display configuration whereby either the graphics or video channel may act as the PIP source to overlay over the other channel. Any one of the inputs (dual inputs to the ADC, DVI, DIP) may be multiplexed to either channel.

The PIP display window can be placed arbitrarily in the main display window. The size of the PIP display window is fully programmable up to 640x480 pixels. The PIP display allows 16 levels of blending within the PIP window either with a specified background color or the main channel.

This device can support viewing of both video and graphics in a side-by-side format. The maximum widow size for the side-by-side is 960x600 pixels each. In this mode, the video input will always be processed by the main channel while the graphics input will be processed by the PIP channel.

Using external memory, the PIP channel image data can be frame rate converted so that it matches the refresh rate of the main image and can subsequently be merged in various picture arrangements.

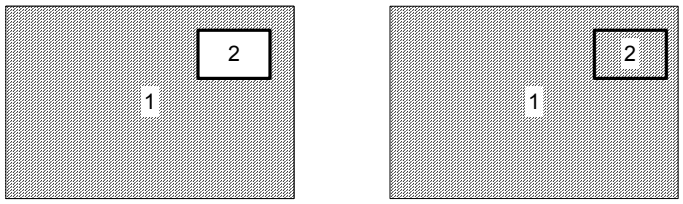
The PIP channel contains a separate 3x3 color matrix to allow for different color settings in the PIP channel from the main channel.

4.24.1 PIP Border and Blending

The PIP display mode consists of two windows with one smaller window sitting on top of the other. This smaller window is called the PIP window. Its size and position are fully programmable up to 640x480 pixels. The transparency (blend) level of the PIP window is adjustable up to 16 levels.

Free Datasheet http://www.datasheet4u.com/

Figure 23: PIP Example



This device incorporates hardware support for the PIP-border. The PIP border size, color and on/off status is programmable.

4.25 Output Display Port (ODP)

The Output Display Port provides data and control signals that permit this device to connect to a variety of flat panel devices using a dual channel LVDS / 24-bit TTL interface. The output interface is configurable for single or dual wide LVDS in 18 or 24-bit RGB pixels format. All display data and timing signals are synchronous with the DCLK display clock. The integrated LVDS transmitter is programmable to allow the data and control signals to be mapped into any sequence depending on the specified receiver format. DC balanced operation is supported as described in the Open LDI standard.

4.25.1 Display Synchronization

Display synchronization mode support:

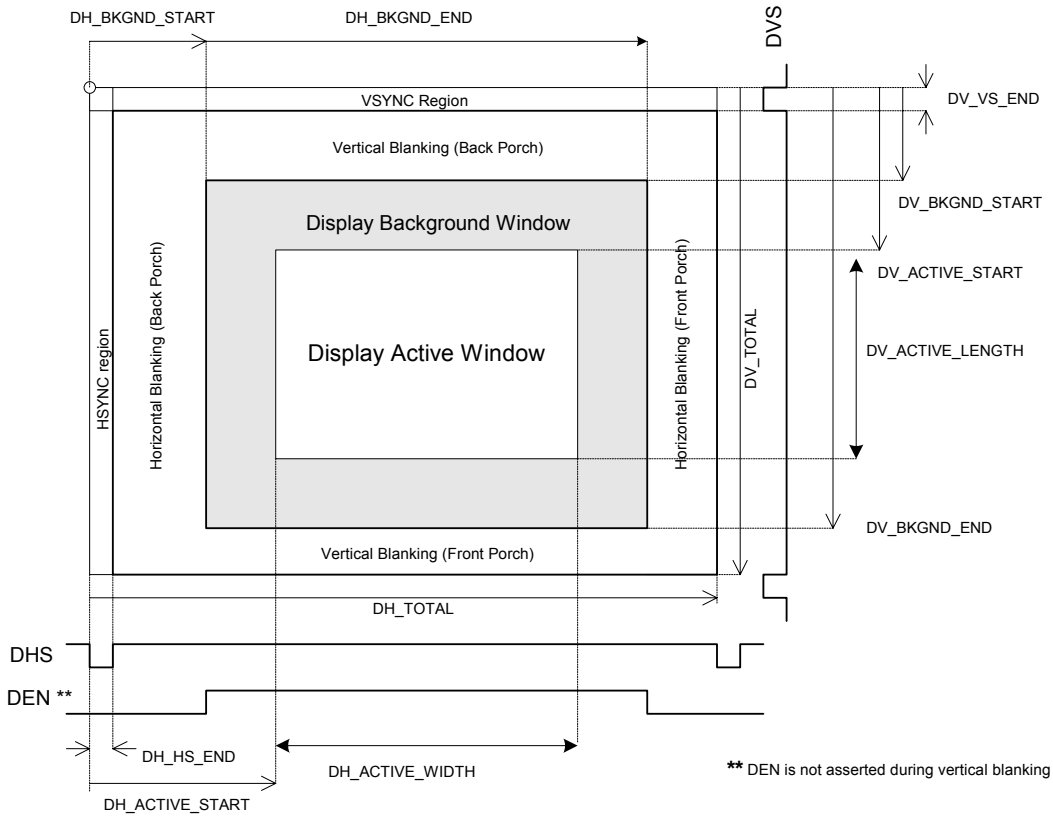
- **Frame Sync Mode:** The display frame rate is synchronized to the input frame or field rate. This mode is used for standard operation.
- **Free Run Mode:** No synchronization. This mode is used when there is no valid input timing (i.e. to display OSD messages or a splash screen) or for testing purposes. In free-run mode, the display timing is determined only by the values programmed into the display window and timing registers.

4.25.2 Display Timing Programming

Horizontal values are programmed in single-pixel increments relative to the leading edge of the horizontal sync signal. Vertical values are programmed in line increments relative to the leading edge of the vertical sync signal.

Free Datasheet http://www.datasheet4u.com/

Figure 24: Display Windows and Timing



4.25.3 Gamma Look-up Table (LUT)

Each pixel of a displayed cell is resolved to an 8-bit color code. An 8 to 10-bit look-up table (LUT) for each input color channel is intended for Gamma correction and to compensate for a non-linear response of the LCD panel. A 10-bit output minimizes the quantization errors in dark luminance ranges ensuring more accurate color representation. The LUT is user-programmable to provide an arbitrary transfer function. Gamma correction occurs after the zoom / shrink scaling block. If bypassed, the LUT does not require programming.

4.25.4 Output Dithering

The Gamma LUT outputs a 10-bit value for each color channel. This value is dithered down to either 8-bits for 24-bit per pixel panels, or 6-bits for 18-bit per pixel panels. In this way it is possible to display 16.7 million colors on a LCD panel with 6-bit column drivers.

The benefit of dithering is that the eye tends to average neighboring pixels and a smooth image free of contours is perceived. Dithering works by spreading the quantization error over neighboring pixels both spatially and temporally. Two

Free Datasheet http://www.datasheet4u.com/

dithering algorithms are available: random or ordered dithering. Ordered dithering is recommended when driving a 6-bit panel.

All gray scales are available on the panel output whether using 8-bit panel (dithering from 10 to 8 bits per pixel) or using 6-bit panel (dithering from 10 down to 6 bits per pixel).

4.25.5 LVDS Transmitter

Two LVDS channels (A and B) are available to transmit data and timing information to the display device.

NOTE: For single wide LVDS usage the LVDS even channel must be used. The following tables show the available LVDS mappings.

An integrated LVDS transmitter with programmable input to output configuration is provided to enable drive of all known panels. The LVDS transmitter can support the following:

- Single pixel mode
- 24-bit panel mapping to the LVDS channels
- 18-bit panel mapping to the LVDS channels
- Programmable channel swapping (the clocks are fixed)
- Programmable channel polarity swapping

Table 22: Supported LVDS 24-bit Panel Data Mappings

Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	R6, R7, G6, G7, B6, B7, RES

Channel 0	R2, R3, R4, R5, R6, R7, G2
Channel 1	G3, G4, G5, G6, G7, B2, B3
Channel 2	B4, B5, B6, B7, PHS, PVS, PDE
Channel 3	R0, R1, G0, G1, B0, B1, RES

Table 23: Supported LVDS 18-bit Panel Data Mapping

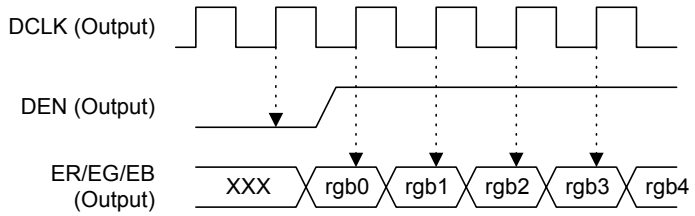
Channel 0	R0, R1, R2, R3, R4, R5, G0
Channel 1	G1, G2, G3, G4, G5, B0, B1
Channel 2	B2, B3, B4, B5, PHS, PVS, PDE
Channel 3	Disabled for this mode

The LVDS transmitter may be configured to operate in DC and non-DC balance mode.

Free Datasheet http://www.datasheet4u.com/

4.25.6 Single Pixel TTL Output

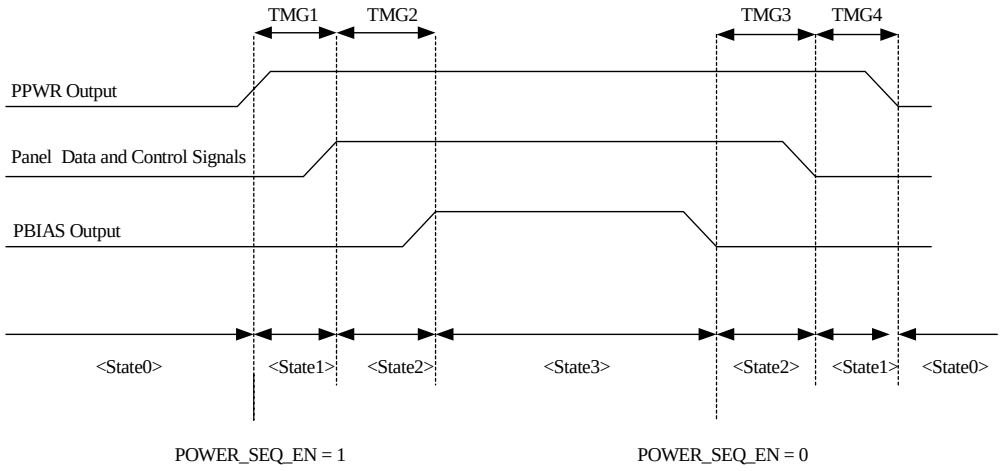
Figure 25: Single Pixel Width Display Data



4.25.7 Panel Power Sequencing (PPWR, PBIAS)

Two dedicated outputs PPWR and PBIAS are used to control LCD power sequencing once data and control signals are stable. The timing of these signals is fully programmable.

Figure 26: Panel Power Sequencing



4.26 Energy Spectrum Management® (ESM)

High spikes in the EMI power spectrum may cause LCD monitor products to violate emissions standards. This device has many features that can be used to reduce electromagnetic interference (EMI). These include drive strength control and clock spectrum modulation. These features help to eliminate the costs associated with EMI reducing components and shielding.

4.27 On-Screen Display (OSD)

This device incorporates a fully programmable, high-quality OSD controller. The graphics are divided into “cells” of programmable size. The cells are stored in an on-

Free Datasheet http://www.datasheet4u.com/

chip static RAM (16K bytes) and can be stored as 1-bit per pixel data, 2-bit per pixel data or 4-bit per pixel data.

Some general features of the OSD controller include:

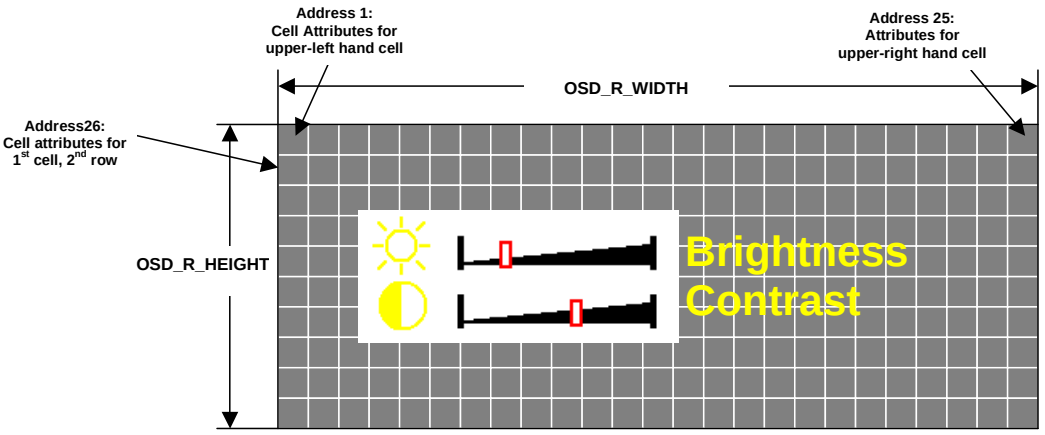
- **Two OSD Rectangles –** The OSD can appear in two separately defined rectangular regions.
- **OSD Position –** The OSD menu can be positioned anywhere on the display region. The reference point is Horizontal and Vertical Display Background Start (DH_BKGND_START and DV_BKGND_START).
- **OSD Stretch –** The OSD image can be stretched horizontally and/or vertically by a factor of two. Pixel and line replication is used to stretch the image.
- **OSD Blending** – Sixteen levels of blending are supported for selected colors in the character-mapped.

4.27.1 On-Chip OSD SRAM

The on-chip static RAM (32K bytes) stores the cell map, cell definitions, and attribute map. The OSD SRAM is shared by the on-chip microcontroller as part of its normal addressable memory space.

In memory, the cell map is organized as an array of words, each defining the attributes of one visible character on the screen starting from upper left of the visible character array. These attributes specify which character to display, whether it is stored as 1, 2 or 4 bits per pixel, the foreground and background colors, blinking, etc. Registers are used to define the visible area of the OSD image.

Figure 27: OSD Cell Map



Cell definitions are stored as bit map data. On-chip registers point to the start of 1-bit per pixel definitions, 2-bit per pixel definitions and 4-bit per pixel definitions respectively.

Note that the cell map and the cell definitions share the same on-chip RAM. Thus, the size of the cell map can be traded off against the number of different cell definitions. In particular, the size of the OSD image and the number of cell definitions must fit in RAM.

Free Datasheet http://www.datasheet4u.com/

4.28 On-Chip Microcontroller (OCM)

The OCM executes a firmware program running from external serial peripheral interface (SPI) ROM. A serial peripheral interface is provided for use with a serial FLASH ROM and a cache controller inside the device. This port connects directly to standard, commercially available SPI ROM or programmable SPI FLASH ROM devices. SPI flash ROMs up to 512KB is supported.

4.28.1 In-System-Programming (ISP) of External FLASH ROM

In is possible to program the serial ROM devices via the standard UART or by using DDC2Bi protocol. Hardware is provided by Genesis Microchip to interface the programming host with the system being programmed. The embedded boot firmware (see the Embedded Bootstrap Function section) performs the programming of external flash ROM.

4.28.2 Serial Peripheral Interface for SPI Flash ROM

This device supports SPI Serial Flash ROM up to 4M-bits through SPI pins, SPI_CSn, SPI_CLK, SPI_DO and SPI_DI. The SPI interface should be configured as follows.

SPI_CSn <-> CE# of SPI ROM

SPI_CLK <-> SCK of SPI ROM

SPI_DO <-> SI of SPI ROM

SPI_DI <-> SO of SPI ROM

Pins of WP# and HOLD# of SPI ROM are options for controlling the SPI ROM. WP# if pulled low will disable writing to the ROM. HOLD# is used when multiple devices are used in daisy-chain configuration. They can be pulled-high all the time to disable their functions or they can be controlled with GPIOs for more flexibility. Refer to SPI ROM specifications for details.

4.28.3 UART Interface

The OCM has an integrated Universal Asynchronous Remote Terminal (UART) port that can be used as a factory debug port. In particular, the UART can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System-Programming).

4.28.4 DDC2Bi Interface

Hardware support is provided for DDC2Bi communication over the DDC channel of either the analog or DVI input ports. The specification for the DDC2Bi standard can be obtained from VESA (www.vesa.org). The DDC2Bi port can be used as a factory debug port or for field programming. In particular, the DDC2Bi port can be used to 1) read / write chip registers, 2) read / write to NVRAM, and 3) read / write to FLASH ROM (In-System-Programming).

Free Datasheet http://www.datasheet4u.com/

The factory programming or test station connects to this device through the Direct Data Channel (DDC) of the DSUB15 or DVI connectors. For example, the PC can make display test patterns (see the Test Pattern Generator section) A camera can be used to automate the calibration of the LCD panel.

Two pairs of pins are available for DDC2Bi communication. For DDC2Bi communication over the analog VGA connector pins DDC_SCL_CH1 and DDC_SDA_CH1 should be connected to the DDC clock and data pins of the analog DSUB15 VGA connector. For DDC2Bi communication over the DVI connector pins DDC_SCL_CH2 and DDC_SDA_CH2 should be connected to the DDC clock and data pins of the DVI connector. This device contains serial to parallel conversion hardware that is then accessed by firmware for interpretation and execution of the DDC2Bi command set.

Note that DDC2Bi can only be activated on only one of the inputs at a time. The port activated by default is specified using the bootstrap value of BOOT[3]/ICD_SEL. Firmware may overwrite the default setting by register programming.

4.28.5 JTAG Interface

A JTAG interface is provided to allow in-circuit firmware debugging. This is done using a JTAG port. This port is available on the following signals:

- JTAG_RESET
- JTAG_TDO
- JTAG_TDI
- HOST_SCL (JTAG_CLK)
- HOST_SDA (JTAG_MODE)

Also, a 2-wire to JTAG bridge circuit is provided to allow JTAG commands to be issued using only two pins HOST_SCL and HOST_SDA.

4.28.6 General Purpose Inputs and Outputs (GPIO)

There are 49 potential general-purpose input/output (GPIO) pins. Not all may be available depending on shared functionality of particular pins. These are used by the OCM to communicate with other devices in the system such as keypad buttons, NVRAM, LED's, audio DAC, etc. Each GPIO has independent direction control and open drain enable for reading and writing. Note that some GPIO pins have alternate functionality.

Free Datasheet http://www.datasheet4u.com/

Table 24: GPIO and Alternate Functions

Pin Name	Pin Number	Alternate function
GPIO_23/INT0	214	Interrupt Input 0. [5V-tolerant, internal pull-down]
GPIO_24/VDA[0]	215	656 Video Data[0]. [5V-tolerant, internal pull-down]
GPIO_25/VDA[1]	216	656 Video Data[1]. [5V-tolerant, internal pull-down]
GPIO_26/VDA[2]	217	656 Video Data[2]. [5V-tolerant, internal pull-down]
GPIO_27/VDA[3]	218	656 Video Data[3]. [5V-tolerant, internal pull-down]
GPIO_28/VDA[4]	219	656 Video Data[4]. [5V-tolerant, internal pull-down]
GPIO_29/VDA[5]	220	656 Video Data[5]. [5V-tolerant, internal pull-down]
GPIO_30/VDA[6]	221	656 Video Data[6]. [5V-tolerant, internal pull-down]
GPIO_31/VDA[7]	222	656 Video Data[7]. [5V-tolerant, internal pull-down]
GPIO_10/B4	108	LVTTL Display Port Blue 4; [5V-tolerant, internal pull-down]
GPIO_11/B5	109	LVTTL Display Port Blue 5; [5V-tolerant, internal pull-down]
GPIO_12/B6	110	LVTTL Display Port Blue 6; [5V-tolerant, internal pull-down]
GPIO_13/B7	111	LVTTL Display Port Blue 7; [5V-tolerant, internal pull-down]
GPIO_14/DCLK	115	LVTTL Display Port DCLK; [5V-tolerant, internal pull-down]
GPIO_15/DEN	116	LVTTL Display Port DEN; [5V-tolerant, internal pull-down]
GPIO_16/DHS	117	LVTTL Display Port DHS [5V-tolerant, internal pull-down]
GPIO_17/DVS	118	LVTTL Display Port DVS [5V-tolerant, internal pull-down]
GPIO_18/ SCL_0(2W_Mst)	119	TWO_WIRE Master_0 Clock [Schmitt trigger, 5V-tolerant]
GPIO_19/SDA_0(2W_Mst)	120	TWO_WIRE Master_0 Data [Schmitt trigger, 5V-tolerant]
GPIO_20/SCL_1(2W_Mst)	121	TWO_WIRE Master_1 Clock [Schmitt trigger, 5V-tolerant]
GPIO_21/SDA_1(2W_Mst)	122	TWO_WIRE Master_1 Data [Schmitt trigger, 5V-tolerant]
GPIO_7/JTAG_MODE	157	JTAG Boundary Scan MODE [5V-tolerant, internal pull-up]
GPIO_6/JTAG_CLK	158	JTAG Boundary Scan CLK [5V-tolerant, internal pull-up]
GPIO_5/JTAG_TDI	159	JTAG Boundary Scan TDI [5V-tolerant, internal pull-up]
GPIO_4/JTAG_TDO	160	JTAG Boundary Scan TDO [5V-tolerant, internal pull-up]
GPIO_3/JTAG_RESET	163	JTAG Boundary Scan Reset [5V-tolerant, internal pull-up]
GPIO_2	164	No alternative functions. [5V-tolerant, internal pull-down]
GPIO_49	165	No alternative functions [Open drain 5V-tolerant]
GPIO_48	166	No alternative functions [Open drain, 5V-tolerant]
GPIO_22/INT1	211	Interrupt Input 1 and also shared with Interrupt Out [5V-tolerant, internal pull-down]
GPIO_23/INT0	214	Interrupt Input 0 [5V-tolerant, internal pull-down]
GPIO_0/DDC_SCL_0	230	Two_Wire Slave (DDC2B) clock input. [Schmitt trigger, 5V-tolerant]
GPIO_1/DDC_SDA_0	231	Two_Wire Slave (DDC2B) data i/o. [Schmitt trigger, 5V-tolerant]
GPO_8/PWM2/BOOT[6]	243	PWM2 output; shared with BOOT[6] input. [5V-tolerant, internal pull-down]
GPO_9/PWM3/BOOT[7]	244	PWM3 output, shared with BOOT[7] input [5V-tolerant, internal pull-down]
GPO_0	69	No alternative functions. [5V-tolerant, internal pull-down]
GPO_1	70	No alternative functions. [5V-tolerant, internal pull-down]
GPO_2	71	No alternative functions. [5V-tolerant, internal pull-down]
GPO_3	72	No alternative functions. [5V-tolerant, internal pull-down]
GPO_4	74	No alternative functions. [5V-tolerant, internal pull-down]
GPO_5	75	No alternative functions. [5V-tolerant, internal pull-down]
GPO_6	77	No alternative functions. [5V-tolerant, internal pull-down]
GPO_7	126	No alternative functions. [5V-tolerant, internal pull-down]
ITU601_4/GPIO_36	2	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_3/GPIO_35	3	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_2/GPIO_34	4	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]

Free Datasheet http://www.datasheet4u.com/

ITU601_1/GPIO_33	5	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_0/GPIO_32	6	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_15/GPIO_47	239	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_14/GPIO_46	240	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_13/GPIO_45	248	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_12/GPIO_44	249	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_11/GPIO_43	250	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_10/GPIO_42	251	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_9/GPIO_41	252	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_8/GPIO_40	253	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_7/GPIO_39	254	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_6/GPIO_38	255	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]
ITU601_5/GPIO_37	256	ITUR-BT601 YUV4:2:2 input. [5V-tolerant, internal pull-down]

4.28.7 Pulse Width Modulation (PWM)

Many of today's LCD back light inverters require both a PWM input and variable DC voltage to minimize flickering (due to the interference between panel timing and inverter's AC timing), and adjust brightness.

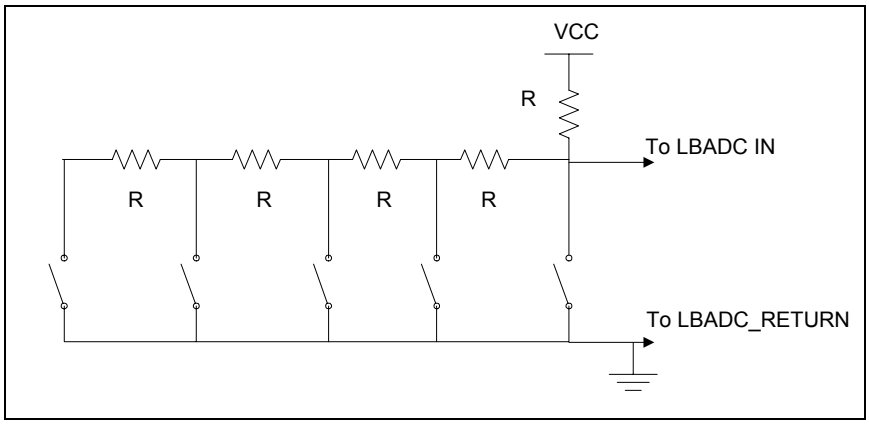
There are four pins available for PWM outputs: PWM0, PWM1, PWM2 and PWM3. The duty cycle of these signals is programmable. They may be connected to an external RC integrator to generate a variable DC voltage for a LCD back light inverter. Panel HSYNC is used as the clock for a counter generating this output signal.

PWM0 has an additional option for 10-bit duty cycle control.

4.28.8 Low-Bandwidth ADC (LBADC)

A general-purpose ADC is integrated to allow for functions such as keypad scanning or for monitoring system temperature or voltage sensors. The ADC has 8 bits of resolution, and can perform a conversion in 13 LBADC clock periods. The LBADC sampling clock can either be TCLK, TCLK/2 or TCLK/4. The maximum sampling clock frequency for 8-bit resolution is 14MHz. An analog multiplexer selects one of three analog input pins as the input to the ADC.

Figure 28: Typical Keypad Function



Free Datasheet http://www.datasheet4u.com/

4.28.9 Low Power State

This device provides a low power state in which the clocks to selected parts of the chip may be disabled. In addition, the OCM_CLK may be reduced (by a factor of up to 510) so that the OCM itself consumes less power.

4.29 Electrostatic Discharge (ESD)

Integrated ESD diodes protect the device during handling. External on-board ESD diodes are required on the analog RGB inputs, DVI inputs, and DDC inputs for protection against electrical overstress (EOS).

Free Datasheet http://www.datasheet4u.com/

5 Electrical Specifications

5.1 Preliminary DC Characteristics

Table 25: Absolute Maximum Ratings

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
3.3V Supply Voltages (1,2)	$V_{VDD\_3.3}$	-0.3		3.4	V
1.8V Supply Voltages (1.2)	$V_{VDD\_1.8}$	-0.3		1.85	V
Input Voltage (5V tolerant inputs) (1,2)	$V_{IN5Vtol}$	-0.3		5.5	V
Input Voltage (non 5V tolerant inputs) (1,2)	V_{IN}	-0.3		3.6	V
Electrostatic Discharge	V_{ESD}			±2.0	kV
Latch-up	I_{LA}			±100	mA
Ambient Operating Temperature	T_A	0		70	°C
Storage Temperature	T_{STG}	-40		150	°C
Operating Junction Temp.	T_J	0		125	°C
Thermal Resistance (Junction to Air) Natural Convection Heat slug incorporated. gm5862H/5822H on 4-layer PCB	θ_{JA_4L}			14.7	°C/W
Thermal Resistance (Junction to Case) Convection Heat slug incorporated. gm5862H/5822H on 4-layer PCB	θ_{JC_4L}			5.9	°C/W
Soldering Temperature	T_{SOL}			250±5	°C

NOTE (1): All voltages are measured with respect to GND.
NOTE (2): Absolute maximum voltage ranges are for transient voltage excursions.

Table 26: DC Characteristics

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
POWER					
Power Consumption @ 193.25 MHz (gm5862H)	P_{WUXGA}			2.5	W
Power Consumption @ 146.25 MHz (gm5822H)	P_{WSXGA+}			2.1	W
Power Consumption @ Low Power Mode (1)	P_{LP}		<100		mW
3.3V Supply Voltages (VDDA and RVDD)	$V_{VDD\_3.3}$	3.2	3.3	3.4	V
1.8V Supply Voltages (VDD and CVDD)	$V_{VDD\_1.8}$	1.75	1.8	1.85	V
Supply Current @ CLK =193.25 MHz • 1.8V digital supply (2) • 3.3V digital supply (4) • 3.3V analog supply (5)	I $I_{VDD\_1.8}$ $I_{VDD\_3.3}$ $I_{VDDA\_3.3}$		 600 110 280		mA
Supply Current @ Low Power Mode	I_{LP}		<30		mA
INPUTS					
High Voltage	V_{IH}	2.0		V_{DD}	V
Low Voltage	V_{IL}	GND		0.8	V
High Current (V_{IN} = 5.0 V)	I_{IH}	-25		25	µA
Low Current (V_{IN} = 0.8 V)	I_{IL}	-25		25	µA
Capacitance (V_{IN} = 2.4 V)	C_{IN}			8	pF
OUTPUTS					
High Voltage (I_{OH} = 7 mA)	V_{OH}	2.4		V_{DD}	V
Low Voltage (I_{OL} = -7 mA)	V_{OL}	GND		0.4	V
Tri-State Leakage Current	I_{OZ}	-25		25	µA

NOTE (1): Low power figures result from setting the ADC, DVI, and clock power down bits so that only the micro-controller is running.
NOTE (2): Includes all CVDD_1.8, VDD_RPLL_1.8, VDD_DVI_1.8 and VDD1_ADC_1,8 pins.
NOTE (3): Includes all RVDD_3.3 pins.
NOTE (4): Includes pins AVDD_LV_3.3, AVDD_OUT_LV_3.3, VDDA_DVI_3.3, VDDA_ADC, AVDD_RPLL_3.3 and LBADC_VDD_3.3.
NOTE (5): Maximum current figures are provided for the purposes of selecting a power supply circuit.

Free Datasheet http://www.datasheet4u.com/

5.2 Preliminary AC Characteristics

All timings are measured relative to a 1.5V logic-switching threshold, under normal operating conditions, and with loading capacitance C_L = 16pF for all outputs.

Table 27: Maximum Speed of Operation

Clock Domain	Max Speed of Operation
Main Input Clock (TCLK)	25 MHz (14.3MHz recommended)
DVI Differential Input Clock (DVI_CLK)	165 MHz
ADC Clock (SCLK)	205 MHz
Input Clock (IP_CLK)	195 MHz
Reference Clock (RCLK)	220MHz (200MHz recommended)
On-Chip Microcontroller Clock (OCM_CLK)	100 MHz
Display Clock (DCLK)	165 MHz

Figure 29: Timing Diagram for ITU656 Video Port

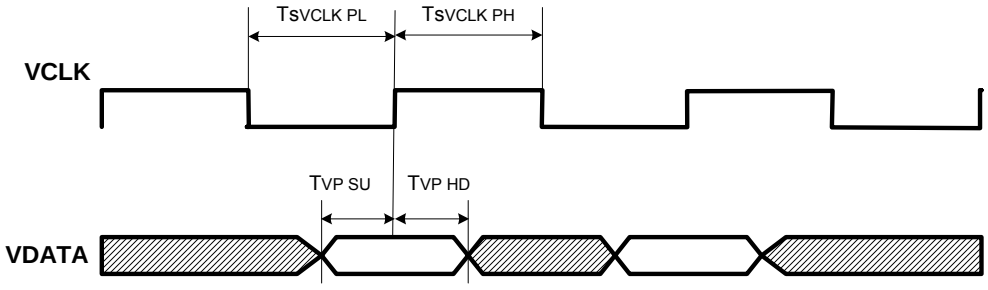


Table 28: Input Timing for ITU656 Video Port

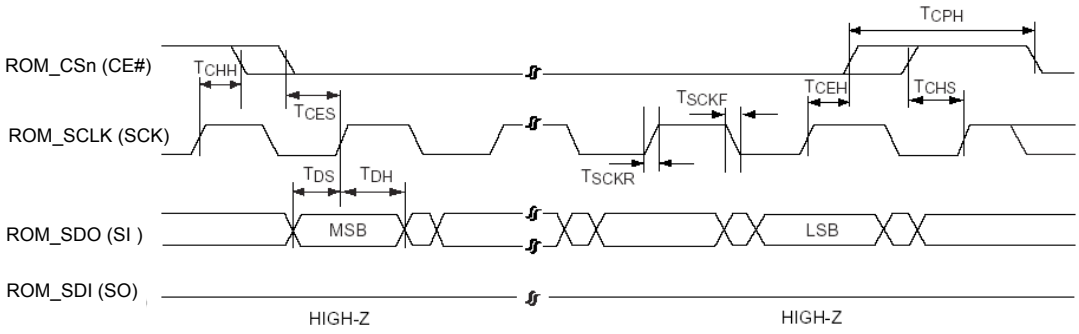
Symbol	Parameter	Min	Max	Units
T_{VP_SU}	Setup time for data signals valid before VCLK edge. VCLK edge is programmable to be either rising or falling.	2		nsec
T_{VP_HD}	Hold time for data/control signals to remain valid after VCLK edge.	1		nsec
T_{VCLK_PH}	VCLK high pulse width period	3		nsec
T_{VCLK_PL}	VCLK low pulse width period	3		nsec
F_{VCLK}	VCLK maximum operating frequency.		28	Mhz

Free Datasheet http://www.datasheet4u.com/

Table 29: SPI Interface Timing, VDD = 2.7~3.6V

Symbol	Parameter	Min	Max	Units
F_{CLK}	Serial Clock frequency		50	MHZ
T_{SCKH}	Serial Clock High Time	5		ns
T_{SCKL}	Serial Clock Low Time	5		ns
T_{SCKR}	Serial Clock Rise Time		5	ns
T_{SCKF}	Serial Clock Fall Time		5	ns
T_{CES}	CE# active Setup time	10		ns
T_{CEH}	CE# active Hold time	10		ns
T_{CHS}	CE# Not active Setup time	10		ns
T_{CHH}	CE# Not active Hold time	10		ns
T_{CPH}	CE# High time	100		ns
T_{CHZ}	CE# High to High-Z output		20	ns
T_{CLZ}	SCK Low to Low-Z Output	0		ns
T_{DS}	Data In Setup Time	5		ns
T_{DH}	Data In Hold Time	5		ns
T_{OH}	Output Hold from SCK change	0		ns
T_V	Output Valid from SCK		20	ns
T_{SE}	Sector Erase		25	ms
T_{BE}	Block Erase		25	ms
T_{SCE}	Chip Erase		100	ms
T_{BP}	Byte Program		20	ms

Figure 30: Serial Interface SPI ROM Timing Diagrams



Free Datasheet http://www.datasheet4u.com/

Figure 31: Serial Interface SPI ROM Timing Diagrams

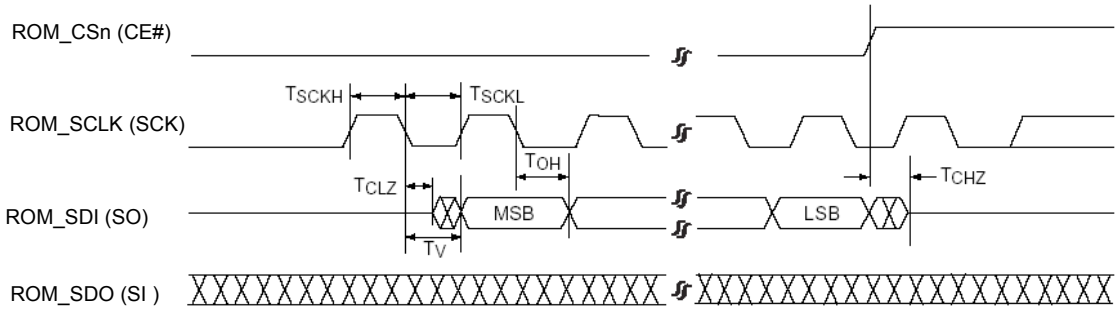


Table 30: External Memory Interface Timing and Adjustments

OUT_TIMING	Min (MCLK)	Typical (MCLK)	Max (MCLK)
Propagation delay from MCLK to DQ* (output)	1/16	¼	3/4
Propagation delay from MCLK to A*	1/16	¼	3/4
Propagation delay from MCLK to RAS#	1/16	¼	3/4
Propagation delay from MCLK to CAS#	1/16	¼	3/4
Propagation delay from MCLK to WE#	1/16	¼	3/4
Propagation delay from MCLK to BA	1/16	¼	3/4

Note: This table lists the amount of adjustment in unit of MCLK that can be made to the framestore output propagation delays, in order to improve setup margin of DRAM write operations at the expense of Hold margin on write operations and setup margin on read operations.

Free Datasheet http://www.datasheet4u.com/

Figure 32: LVDS Transmitter Switching Characteristics

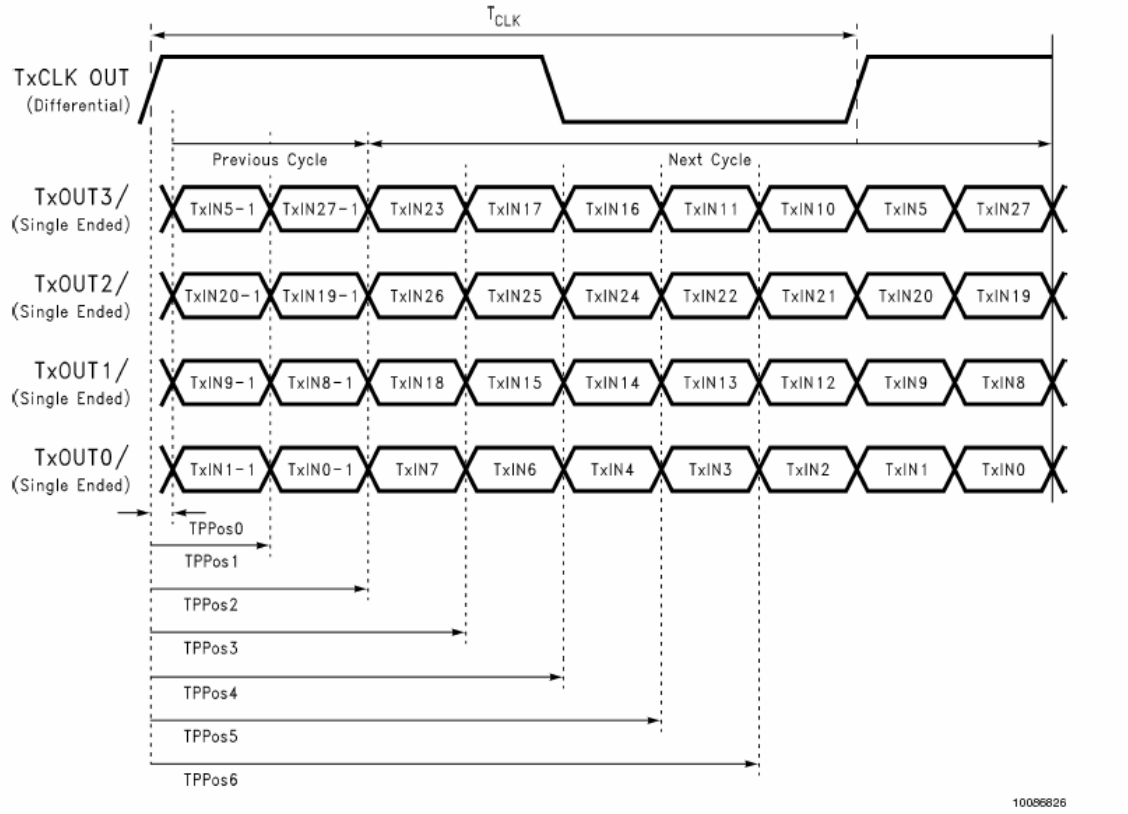


Table 31: LVDS Even Channels 0 to 3(1)

Symbol	Parameters	E_CH0 ~ E_CH3	Min	Typical	Max	Units
TPPos0	T/X output pulse position for bit 0	F= 65 Mhz	-0.3	0	0.3	ns
TPPos1	T/X output pulse position for bit 1		1.9	2.2	2.5	ns
TPPos2	T/X output pulse position for bit 2		4.1	4.4	4.7	ns
TPPos3	T/X output pulse position for bit 3		6.3	6.6	6.9	ns
TPPos4	T/X output pulse position for bit 4		8.5	8.8	9.1	ns
TPPos5	T/X output pulse position for bit 5		10.7	11.0	11.3	ns
TPPos6	T/X output pulse position for bit 6		12.9	13.2	13.5	ns

Table 32: LVDS Odd Channels 0 to 3(1)

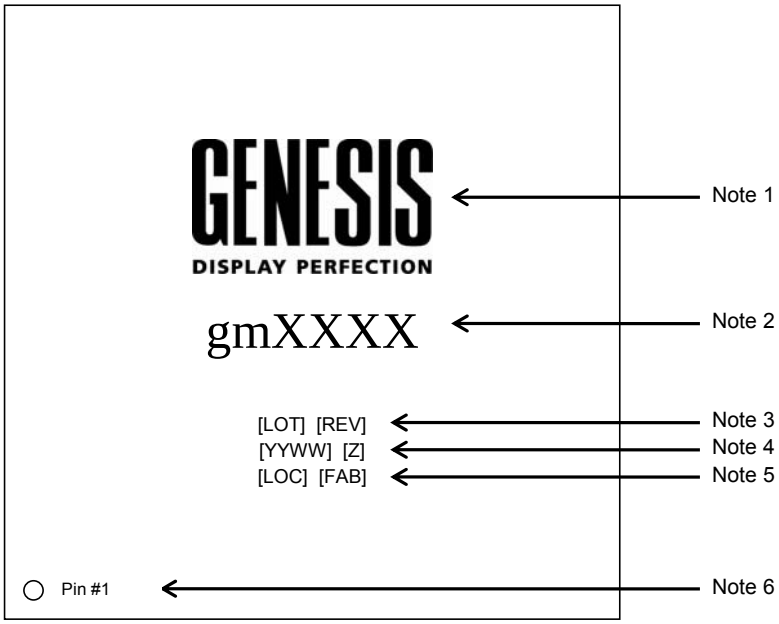
Symbol	Parameters	O_CH0 ~ O_CH3	Min	Typical	Max	Units
TPPos0	T/X output pulse position for bit 0	F= 65 Mhz	-0.3	0	0.3	ns
TPPos1	T/X output pulse position for bit 1		1.9	2.2	2.5	ns
TPPos2	T/X output pulse position for bit 2		4.1	4.4	4.7	ns
TPPos3	T/X output pulse position for bit 3		6.3	6.6	6.9	ns
TPPos4	T/X output pulse position for bit 4		8.5	8.8	9.1	ns
TPPos5	T/X output pulse position for bit 5		10.7	11.0	11.3	ns
TPPos6	T/X output pulse position for bit 6		12.9	13.2	13.5	ns

NOTE: There is +/- 200 ps variation for the measurements for even and odd channels in reference to clock.

Free Datasheet http://www.datasheet4u.com/

6 Branding Information

Figure 33: Branding Diagram



Note 1: Genesis Logo
Must be prominently displayed

Note 2: Part Number
Font must be 2-3 sizes bigger than rest of text
gm – Genesis Microchip
FLI – Faroudja Laboratories (Genesis part that incorporates Faroudja technology)
XXXX – Alphanumeric part number

Note 3: Lot Code
[LOT] – Alphanumeric characters designation for lot number
[REV] – Two letter designation for mask ID revision

Note 4: Assembly Code
[YYWW] – YY = year; WW = workweek; when package is molded or sealed
[Z] – Assembly company

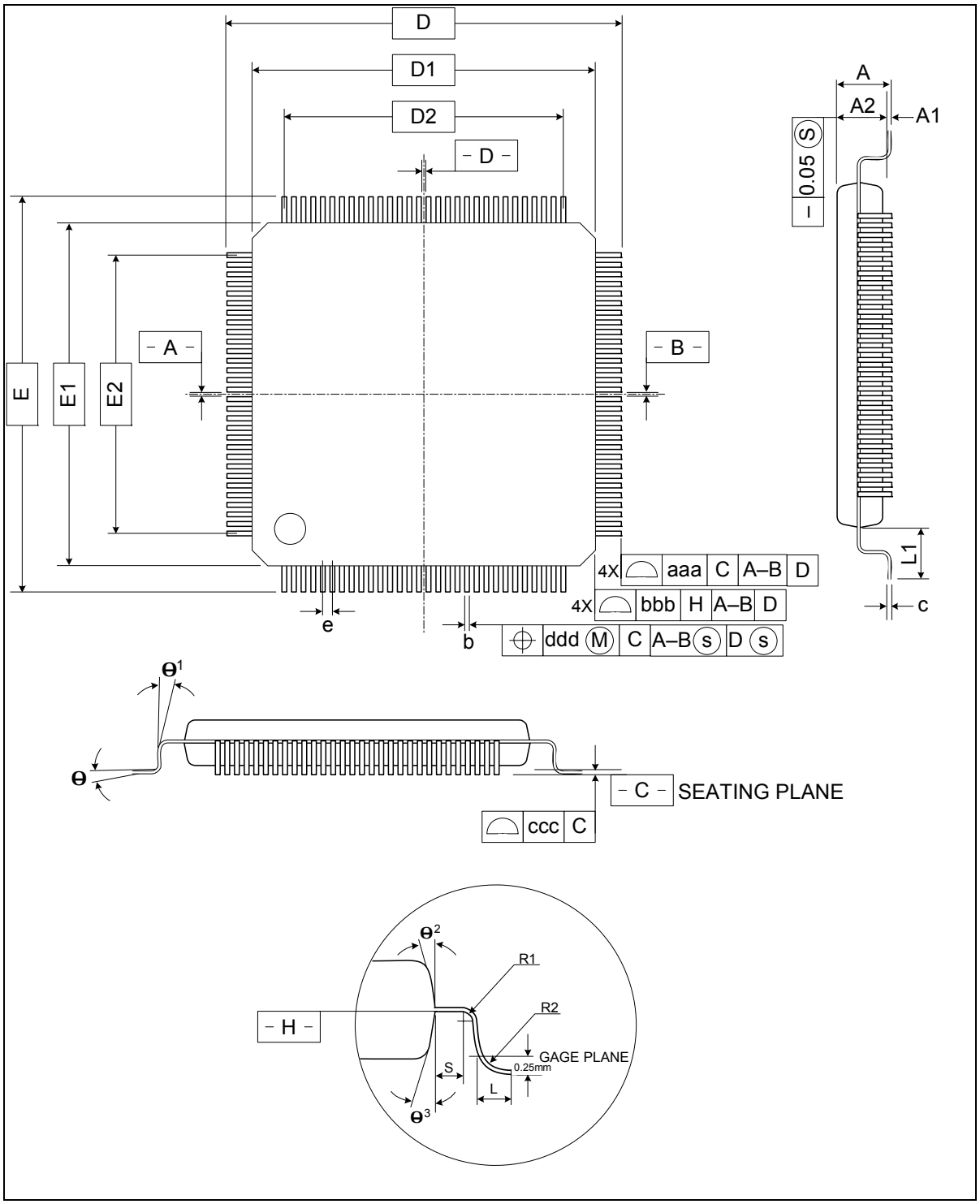
Note 5: Fab Location Code
[LOC] – Country of origin
[FAB] – Fab

Note 6: Pin #1 location identifier

Free Datasheet http://www.datasheet4u.com/

7 Mechanical Specifications

Figure 34: 256-pin PQFP Mechanical Drawing



Free Datasheet http://www.datasheet4u.com/

Table 33: Package Dimensions

SYMBOL	MILLIMETER			INCH		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	4.10	—	—	0.161
A1	0.25	—	—	0.010	—	—
A2	3.20	3.32	3.60	0.126	0.131	0.142
D	30.60 BSC.			1.205 BSC.		
D1	28.00 BSC.			1.102 BSC.		
E	30.60 BSC.			1.205 BSC.		
E1	28.00 BSC.			1.102 BSC.		
R2	0.08	—	0.25	0.003	—	0.010
R1	0.08	—	—	0.003	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ^1	0°	—	—	0°	—	—
θ^2	8° REF			8° REF		
θ^3	8° REF			8° REF		
c	0.09	0.15	0.20	0.004	0.006	0.008
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.30 REF			0.051 REF		
S	0.20	—	—	0.008	—	—
b	0.13	0.16	0.23	0.005	0.006	0.009
e	0.40 BSC.			0.016 BSC.		
D2	25.20			0.992		
E2	25.20			0.992		
TOLERANCES OF FORM AND POSITION						
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	—	0.08	—	—	0.003	—
ddd	—	0.07	—	—	0.003	—

NOTES:

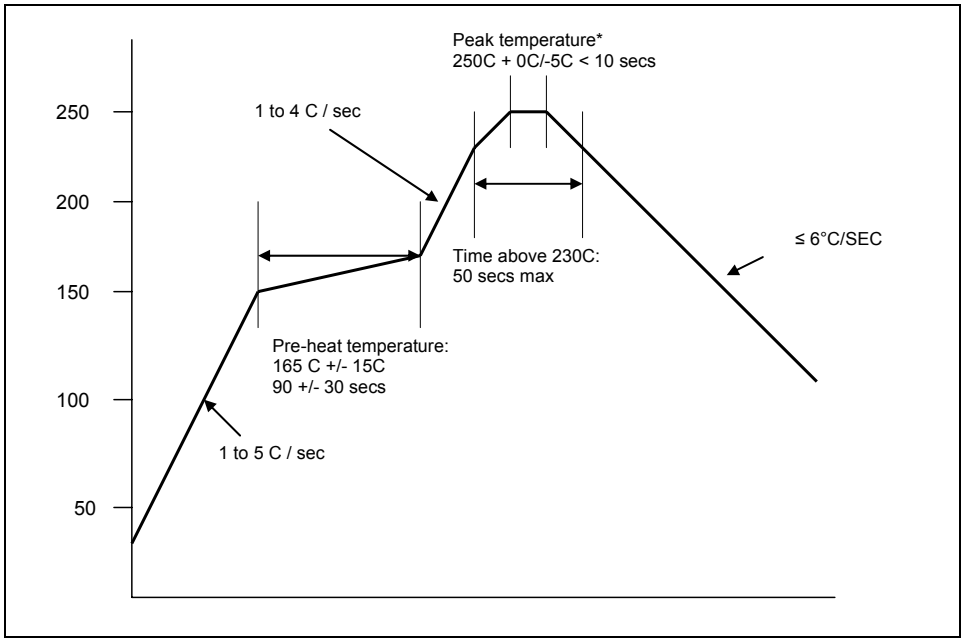
- DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08mm.
- THE TOP PACKAGE BODY SIZE MAY BE SMALLER THAN THE BOTTOM PACKAGE BODY SIZE.

Free Datasheet http://www.datasheet4u.com/

8 Solder Profiles

The following is the recommended solder reflow profile for Genesis Microchip lead-free QFP devices.

Figure 35: Lead-Free QFP Solder Reflow Profile



Free Datasheet http://www.datasheet4u.com/